THE SNS RING LLRF CONTROL SYSTEM

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Abstract

The low-level RF control system for the SNS Ring differs considerably from that for the Linac. To accommodate requirements for higher data throughput and improved performance the system is based on a PCI interfaced Digital Signal Processor (DSP). In accordance with SNS standards, a VME-based PowerPC© is used, but advantage is taken of the on-board PMC slot which houses a Bittware© Hammerhead© PMC card with four AD-21162 DSPs. The EPICS system handles system configuration and data traffic while the DSP performs the low-level RF controls. Protocol and software to support both the PowerPC and the DSP have been developed. This paper presents the system design and initial testing experience.

INTRODUCTION

The SNS accumulator ring contains a single bunch of 1 GeV protons, accumulated over more than 1000 turns, circulating with a period of about 0.95μs per turn. Successive cycles of proton accumulations and extractions occur at 60 Hz under the control of the timing system.

The SNS Ring LLRF System regulates the phase and amplitude of the RF gap voltage in order to maintain a smooth bunch with minimum peak current and a sufficient beam free gap to accommodate the extraction kicker rise time.

Since beam load increases each turn, the Ring LLRF system must adjust the gap volts accordingly to compensate. Predefined turn-by-turn functions of gap voltage in-phase (I) and quadrature (Q) are downloaded to support expected beam accumulation profiles.

SNS supports up to eight different beam modes, each of which may have an independent beam accumulation profile. The beam mode for each cycle is broadcast by the Real Time Data Link (RTDL) system as "flavor ID" in advance of the start of the cycle. The Ring LLRF system uses the beam mode information for selecting appropriate gap voltage functions for each cycle.

To meet all these requirements, we designed and implemented the high-performance, feature-rich SNS Ring LLRF control system.

SYSTEM OVERVIEW

There are four Ring LLRF cavities. Each of them has individual control electronics.

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Hardware Platform

The hardware platform includes the VME-based PPC603 CPU (MVME2100), the SNS standard timing board (V124S) to generate timing gate on specified event, the SNS standard utility board (V108S) to receive event and RTDL information, A custom VME carrier board with DSP link (communication) ports, a field programmable gate array (FPGA), and sites for daughter cards supporting ADCs and DACs.

The heart of Ring LLRF control system is the Bittware Hammerhead-PMC+ (HHPMC) card attached to MVME2100 on PMC slot. It features four ADSP-21160 SHARC DSPs which provides a total of 1920 MFLOPS of processing power. It includes the high performance SharcFIN ASIC to bridge the PCI bus and the local DSP cluster bus. The HHPMC has 256MB onboard SDRAM. It also supports up to eight 80Mbytes/s link ports.

Figure 1: Bittware Hammerhead-PMC+ (HHPMC).

Software Architecture

The SNS Host Interface Library (SNS_HIL) was developed to manage the resources of the HHPMC from MVME2100 running the vxWorks operating system. The MVME2100 is able to easily communicate with all the DSPs and to directly access HHPMC onboard devices such as SDRAM.

The communication and data exchange protocol between the MVME2100 and the DSPs were carefully defined. The SharcFIN ASIC provides eight single-byte-wide mailboxes accessible via the PCI bus which generate PCI-to-DSP interrupts. The SharcFIN provides two four-byte-wide mailboxes, accessible via a DSP, which generate DSP-to-PCI interrupts. These mailboxes are used for timing information and handshaking. The HHPMC onboard SDRAM is accessible from PCI bus, so it is used as shared memory between PowerPC and DSPs. DSP 1 is defined as the communication master. It handles all transactions with the MVME2100 and coordinates the roles of the other three functional DSPs.

Those three DSPs are responsible for I&Q feedback loop, turn-by-turn feed forward correction and dynamic Power RF (HPRF) system with cavity under control.

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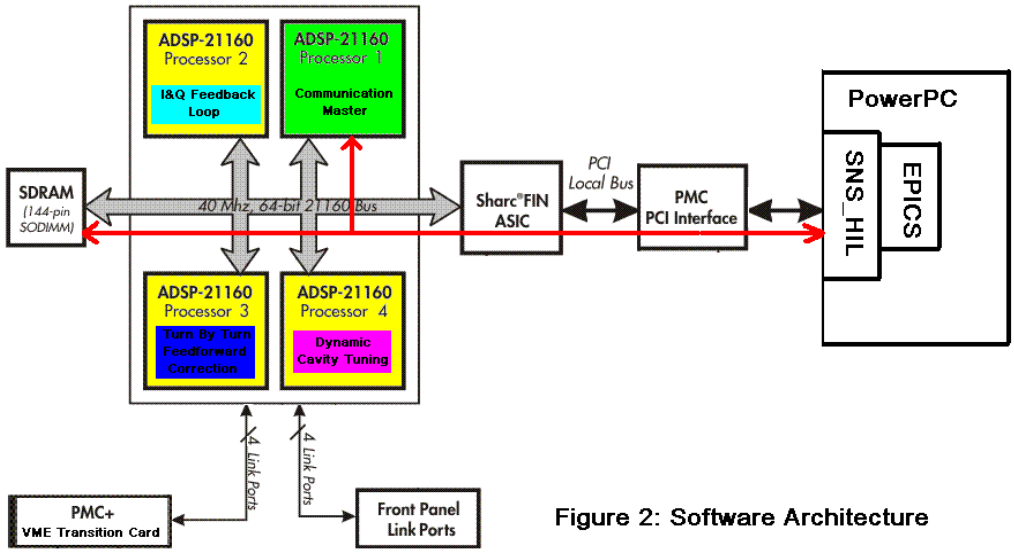

Figure 2: Software Architecture

and DACs on daughter cards via link ports on their carrier cards. Those ADCs and DACs are interfaced via the High cavity tuning, respectively. They communicate with ADCs

Adhering to the SNS control standard, the SNS Ring LLRF control system is EPICS-based. EPICS drivers and device support were developed on top of the SNS_HIL to provide user interface through standard Channel Access protocol.

CONTROL SYSTEM FUNCTIONALITIES

The SNS Ring LLRF control system has six major functions. They are implemented within either an interrupt service routine (ISR) or one of the two operation tasks depending on "direction" of communication, either to the DSP or from the DSP.

Deliver Timing Information

The CYCLE_START event and "flavor ID" are critical timing information for the Ring LLRF system. The CYCLE_START event indicates the beginning of a new 60Hz beam cycle. The "flavor ID" is necessary for the DSP to prepare the correct function tables and control parameters.

The SNS standard timing board can output a trigger to the VME carrier card to trigger ADCs and DACs upon a certain event. However, the DSPs do not have the capability to decode timing information. Therefore, the MVME2100 must deliver timing information to DSP 1.

Since the SNS event is encoded as a single byte, three of the eight PCI-to-DSP mailboxes are used to send CYCLE_START, INJECTION and EXTRACTION events. Two PCI-to-DSP mailboxes are reserved for future use. One PCI-to-DSP mailbox is used to send DSP 1 the "flavor ID" which comes from the RTDL link, and one PCI-to-DSP mailbox is used to notify DSP 1 that new cycle number from RTDL link is available. Before notifying DSP 1 of the new cycle number, the MVME2100 broadcasts the cycle number to all 4 DSPs' internal memory directly. The cycle number is transferred via shared memory, rather than via a mailbox because the cycle number ranges from 0 to 599, which is too large to be fit in single-byte-wide mailbox.

The timing information delivery happens in the ISR for SNS utility board. This introduces less than 150 μs delay.

Download Function Tables

Each function table is a list of pairs of I&Q values corresponding to the different beam loading profiles. Each function table may contain up to 4095 turns of data. Each valid function table ends with a signature "0xFEEDBACC". This is an efficient way to tell DSP whether the memory of function table has been initialized.

For each "flavor ID", there are eight different functions. Since there are eight different "flavor ID" and three functional DSPs, there are a total of 192 functions tables per cavity. All these function tables are stored in HHPMC onboard SDRAM. After the DSP receives the "flavor ID" for upcoming cycle, the DSP will load the proper function tables into DSP internal memory.

Each functional DSP has a swap area in onboard SDRAM for downloading new function tables. The swap area includes the memory block to hold the incoming function table plus a few words to store the "flavor ID" and "function number" to which this function table applies. There is also a "ownership flag" in the swap area which supports mutual exclusion between the DSP and the MVME2100.

New function tables are stored in a text files using a simple ASCII format. The files are maintained in predefined directories available to the MVME2100 via NFS server. An EPICS stringout record is used to send the file name to control system. The control system uses a dedicated task to copy the file from NFS to a local ramDisk to avoid deadlock of scan task and operation task. After the file is successfully copied, a message is sent to operation task.

The operation task then checks the ownership of swap area. If the MVME2100 holds the ownership, the operation task will parse function table file in the ramDisk then start DMA to download function table to swap area

of the appropriate DSP. After DMA successfully finishes, the operation task will turn ownership flag to DSP and use one PCI-to-DSP mailbox to tell DSP 1 that a new function table is already in the swap area. The destination DSP number in indicated in the mailbox. After the DSP finishes moving new function table out of swap area to permanent memory, DSP 1 will turn back ownership flag to the MVME2100 and then use DSP-to-PCI mailbox to notify the MVME2100.

Using text file to store the function table provides a lot of flexibility in managing the function table. Using the EPICS stringout record to download function table provided an effective work-around for some EPICS/CA limitations and provided a straightforward implementation of "bumpless reboot". PCI DMA provides about 50MB/s throughput and dramatically boosts up the system performance.

Download Control Parameters

Control parameters are the scalar values used to setup DSPs and the cavity. The control parameters for SNS Ring LLRF could be either 32-bit integer or 32-bit float values. They are all stored in HHPMC onboard SDRAM.

Up to 255 control parameters are supported per "flavor ID" per functional DSP, for a total of 6120 control parameters. To avoid having to implement an excessive number of EPICS records we divide all parameters to two categories: static and dynamic.

Static control parameters are almost never changed after they are loaded into SDRAM. Generally their values are not very interesting to users. The technique for supporting these control parameters is substantially similar to the technique used to download function tables. For each "flavor ID" of each DSP, up to 127 static control parameters can be stored in a simple text file using a simple ASCII format. The file also ends with a signature "0xFEEDBACC" to indicate valid status. The entire file of static control parameters are DMAed into HHPMC onboard SDRAM upon user's request. Because the operation of each control parameter is atomic, there is no need for an ownership flag or interrupt handshaking.

By comparison, dynamic control parameters changed fairly frequently and may need to be monitored or plotted as they change. Dynamic control parameters are implemented using individual EPICS records, and use conventional memory access techniques to read/write. The number of such dynamic records is intentionally limited to conserve system load.

Upload History Data

History data consists of interesting waveforms reported by a DSP, typically indicating system performance. For each cycle, three functional DSPs are allowed to generate 30 waveforms with 4096 points per waveform. A single large circular buffer in HHPMC onboard SDRAM is used to hold all these waveforms for hundreds of cycles.

In each DSP, a report area is defined to hold the ownership flag, an index of history data in circular buffer and the corresponding "flavor ID".

Each time one of the functional DSPs reports history data, it checks ownership first. Until it has the ownership, it fills and freezes the report area and turns ownership to the MVME2100 then notifies DSP 1 that history data is ready. After DSP 1 receives all notifications from the functional DSPs, it notifies the MVME2100 via a DSP-to-PCI mailbox. The MVME2100 will DMA history data to its local memory then report the waveforms via EPICS waveform records. Then it turns back the ownership flag to DSP. The ownership flag implements flow control for the history data.

Uploading history data could be as fast as 100MBytes/s. But this will put system into unstable situation because other PCI devices such as the Ethernet chip also need bandwidth to DMA data. It became necessary to intentionally throttle back the DMA to avoid undesirable side-effects. With throttling, the history data DMA is about 50Mbytes/s. In the best situation, the MVME2100 can upload history data at about 20Hz.

DSP Management

Users are able to reset all DSPs via a button. Users can also reload DSP program for any DSP during runtime without any cold reboot. The control system also monitors the heartbeat of each DSP to ensure they are running properly, and to generate an alarm if they are not.

Slow Feedback

All turn by turn fast feedback loops are handled by the functional DSPs. There is also a need for slow feedback that does not require turn by turn response and is not very sensitive to delay. To offload the DSP, the EPICS SNL is used to implement some slow feedback loops. History data is used as input to these feedback loops, and the outputs are written to corresponding control parameters.

There is a dedicated control parameter PV for each "flavor ID", but this is not true for history data. To maintain synchronization between history data and the beam mode in effect when the history data was collected, a special history data waveform record was implemented with 4095 data points instead of 4096 with the corresponding "flavor ID" stored in the last location. This allows feedback loops to associate history data with the appropriate output control parameter.

CONCLUSION

The SNS Ring LLRF control system is a high data throughout, high performance, feature-rich system. Functionality is divided between the MVME2100 and the DSPs according to their strengths. It has been smoothly integrated into the EPICS control system. It meets the design requirement and has been used successfully to test the ring cavities.

REFERENCES

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