# FILLING PATTERN MEASUREMENT IN THE LNLS STORAGE RING

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*Abstract*

The storage ring filling pattern affects the performance of the machine in several ways. A bunch charge meter has been developed in order to perform bunch-by-bunch charge measurement and to record the storage ring filling pattern. This instrument separates the electric pulse produced by the selected bunch from the RF signal obtained from a button pick-up. A fast switch based on a double balanced mixer (DBM) was developed to strip off all but one bunch pulse at each revolution period. A 12-bit ADC with a FIFO buffer card acquires the bunch signals. A PECL timing card performs the bunch selection. The bunch charge meter is connected to the LNLS control system through a DSP processor board, which controls the instrument through an FPGA interfacing board. The DSP software provides digital filtering. Some implementation details, performance data and operational results are presented.

## INTRODUCTION

The LNLS 93-meter long 1.37-GeV electron storage ring can be filled with up to 148 bunches. The bucket spacing is 2.1 ns, and a 500-MeV booster synchrotron is the injector for the main ring. The storage ring is filled in a nearly uniform way by a system which automatically controls the phase between the booster and the storage ring, ejecting bunches to fill different buckets at each injection cycle. This system provides uniform filling as long as the LINAC beam energy stays constant along the accumulation. The bunch charge meter is supposed to be very useful for several purposes, for example: recording the filling pattern of the users' runs, machine studies about the correlations between filling patterns and instabilities, bunch lifetime measurements, etc…

## SYSTEM DESCRIPTION

The instrument which contains the bunch charge meter has another RF front-end, the "bunch cleaner", which performs bunch cleaning in the booster injector (also reported in these proceedings). Figure 3 shows the block diagram of the bunch charge meter.

### *Back-end processor*

The back-end processor is composed of a DSP C6711' evaluation board and a card based on an FPGA (XILINX model XC2S50E). This FPGA card was implemented in a four-layer PCB and it works integrating the DSP to the internal devices, namely: acquisition board, timing card, programmable attenuator and the serial communication board of the LNLS control system.

The DSP accesses the FPGA through its expansion connector. The DSP software implements digital filtering and manages the communication between the instrument and the LNLS control system [1].

### *RF front-end*

The beam signal is obtained through one button of an RF button pick-up (8.1-mm diameter). We observed that in our case using an RF combiner to sum the four signals from the pick-up is not an advantageous approach due to the RF reflections caused by the large number of connections.

This signal is applied to a programmable attenuator (Weinschel Corporation, 4206-63) and after that, it is driven to the fast switch, which separates the signal related to one electron bunch. The amplitude of the signal obtained from the button pick-up can reach several volts (peak) according to the beam current and filling pattern. It is necessary to attenuate the beam signal in order to bring it to the useful range of the fast switch.

The fast switch consists of a DBM (Minicircuits model rms-30) and a fast pulse generator (500 ps FWHM) designed on the same circuit board. Figure 1 shows the fast switch circuit.

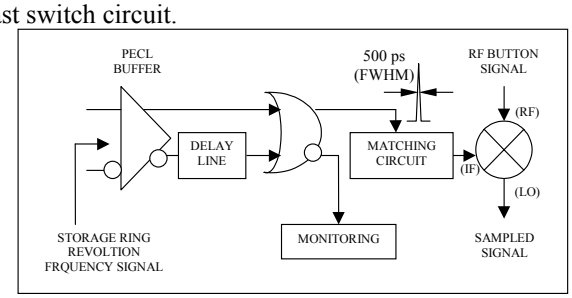


Figure 1 – Fast switch circuit.

The fast pulse is obtained through a simple PECL digital circuit by the delay introduced in one trace of a differential transmission line. When this pulse is applied to the IF input, the DBM captures the RF signal. The digital circuit is coupled with the DBM by a simple passive circuit composed of voltage dividers and matching RF capacitors. Besides RF matching, proper attenuation of the digital pulse is crucial to minimize IF-LO crosstalk.

The signal from the fast switch is analogically treated in order to allow the analog-to-digital conversion. The block diagram of the circuit that performs this treatment is shown in figure 2.

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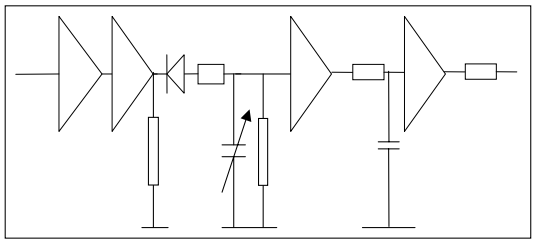

Figure 2 – Block diagram of the pulse treatment circuit.

In figure 2, the first two amplifiers are MAR-6 MMIC Minicircuits. A detector diode (Agilent Technologies, HSMS-8202) and high-frequency trimmers (Voltronics Corp. and Temex Electronics Inc.) compose the detector circuit. Afterwards the signal is amplified by a current feedback Op. Amp. and filtered. The last device is a VCA Op. Amp. (Texas Instruments, VCA610), whose gain is adjusted by the DSP through a 16-bit DAC.

Table 1: Preliminary results of the 12-bit ADC board characterization tests

| | |
|---|---|
| SNR (Signal-to-Noise Ratio) | 65.1 dB |
| SINAD (SIgnal-to-Noise And Distortion ratio) | 65 dB |
| THD (Total Harmonic Distortion) | 85.8 dB |
| ENOB (Effective Number Of Bits) | 10.5 bits |

The processor reads the data in the FIFO buffers through a digital bus (LVTTL level, 50 ways 10 centimeters flat-cable).

### *Timing card*

The fast switch and the ADC module are triggered by the timing card, which is a homemade PECL programmable divider. The output signals are generated through the division of the RF signal, 476.066 MHz, by

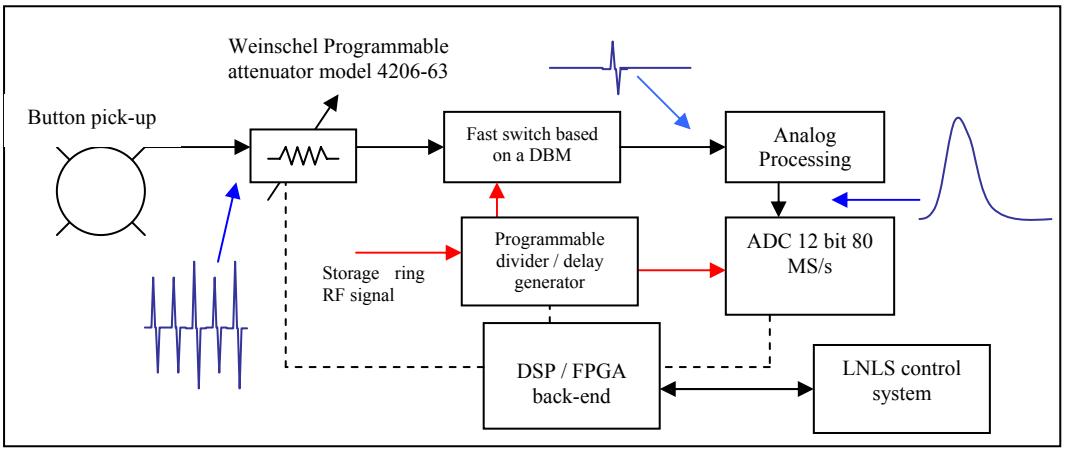


Figure 3: Block diagram of the bunch charge meter

The flexibility given by the large range of input attenuation (63 dB) and by the VCA is enough to perform filling pattern measurements in both multi-bunch and single-bunch modes.

### *Acquisition board*

The signal after switching and analog processing has a smoothed shape and its frequency is the same as the storage ring revolution one (3.21 MHz). A 12-bit ADC board, based on the AD9432 (Analog Devices) with a FIFO buffer, was developed in order to digitize this signal.

The ADC module has 50 Ω differential input, 33 MHz analog bandwidth and maximum conversion rate of 80 MS/s (AC coupling, ECL level). We use two 8-Kbyte, 9-bit FIFO buffers (IDT, IDT72V05), but the module was designed to accept buffers with different capacities by changing them. The circuit was implemented in a four-layer PCB and several precautions [2] related to mixed-signal designs were taken in order to achieve good performance. Some results of the preliminary characterization [3] are shown in Table 1.

the storage ring harmonic number, 148, however any number between 2 and 255 can be used to divide the RF signal. This card has also a programmable delay generator with 20 ps resolution and rms jitter smaller than 5 ps. The relative phase between the two output signals can be adjusted, as well as the phase difference of these two signals to the RF signal.

The timing card was also implemented in a four-layer PCB and high speed digital routing techniques [4] were taken in order to assure signal integrity.

## MEASUREMENT PROCESS

Once the bunch charge meter is on, the acquisition board acquires the beam signal without interruptions. The back-end processor controls the FIFO buffers. When the data is not required, the FIFO buffers are disabled.

Through the control system, the operator can set the desired filtering parameters, which make the acquisition slower or faster. The measurement cycle starts with the optimization of the acquisition parameters, namely: input attenuation, gain of the analog processing stage and fine phase adjusts between the fast switch and the ADC. The acquisition rate is 3.21 MHz and every complete bunch

acquisition fills the entire FIFO buffers (8 Kbytes). Once these buffers are full, which takes about 2.5 ms, the back-end processor reads these data, resets the FIFOs and changes the timing adjusts in order to measure a neighbor bunch. After acquiring the data from the 148 bunches, the filling pattern (or the average of each acquisition) is transferred to the control system.

## PRACTICAL DETAILS

As we expected the process is very sensitive to timing variations. Figure 4 shows how the sampled data changes when the fine timing of the fast switch is adjusted. In this situation the ADC timing adjust was fixed.

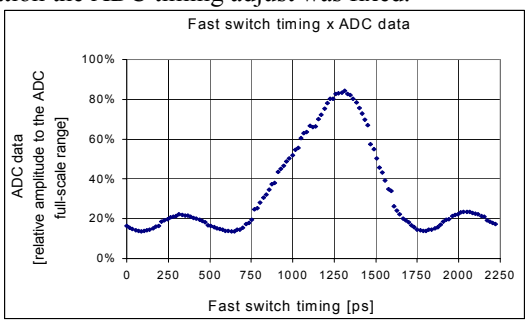


Figure 4 – Sensitivity of the ADC sampling to the timing adjusts of the fast switch.

During the testing period we observed that the variance of the measurements of the high charge bunches were bigger than the low charge bunches. By analyzing all the data (not the average result) it was possible to see a sinusoidal oscillation, which had the same frequency of the synchrotron oscillations. In some cases the amplitude of the sinusoidal oscillations observed was higher than 10% of the ADC full-scale range. The mechanism that produces this coupling is not completely understood. Figure 5 shows an 8-ksample acquisition of the signal from a 2-mA bunch. Figure 6 shows the result of one experiment in which the synchrotron frequency was measured by utilizing both a spectrum analyzer and the bunch charge meter (FFT).

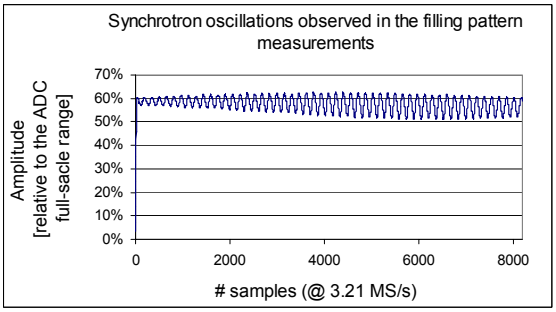


Figure 5 – 8-ksample acquisition of a signal of a 2 mA bunch.

The synchrotron oscillations observed in the bunch signals decrease the resolution of the filling pattern measurement. In order to minimize this effect the back-end processor resamples the data, in other words, the back-end processor reads a number of positions in the buffer, waits a number of clock cycles and reads it again until reaching 8 ksamples. With this procedure a resolution better than 1% was achieved in a 3-second measurement.

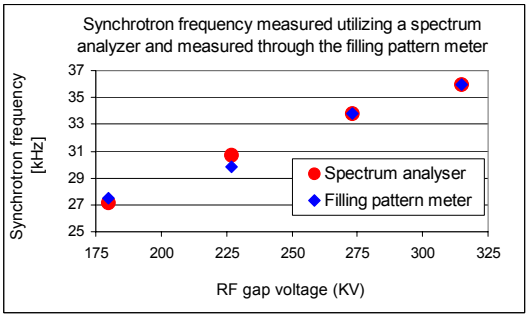


Figure 6 – Synchrotron frequency measured by utilizing a spectrum analyzer and the bunch charge meter (FFT).

A typical filling pattern of the storage ring is shown in figure 7.

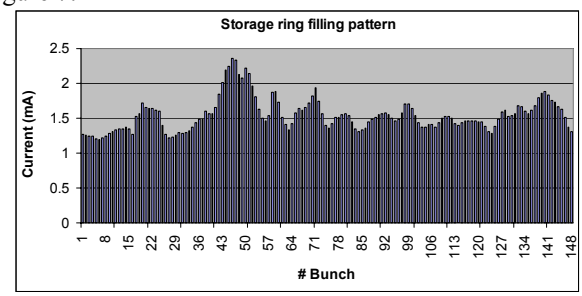


Figure 7 – Typical filling pattern of the storage ring.

We also implemented the bunch charge meter by utilizing a digitizing oscilloscope (Hewlett Packard, model 54750A) and, a measurement with similar resolution takes about 3 minutes due to the low acquisition rate.

## CONCLUSIONS

The bunch charge meter has been developed and integrated to the LNLS control system. A resolution better than 1% was achieved in a 3-second measurement. The system will be calibrated by utilizing a single-bunch beam through the data obtained from both the storage ring DCCT and the HP 54750A oscilloscope.

## REFERENCES

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[3] S.R. Marques, H.J. Onisto, “Chaves rápidas e módulos eletrônicos para aquisição de sinais rápidos no LNLS”, internal communication.

[4] Motorola, Inc. 1996, “High Performance ECL Data” DL140/D REV 4.