HIGH SPEED EPICS DATA ACQUISITION AND PROCESSING ON ONE VME BOARD*

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Abstract

A custom VME board is being designed at the Los Alamos Neutron Science Center (LANSCE) for high-speed signal acquisition and processing. While it is desirable to design around the EPICS / VME platform, it can be difficult to process high-speed signals with long record lengths. The relatively slow data path between the IOC and the general-purpose computer makes real time computations impossible. Commercial VME processor boards can be used, but the data must still flow over the VME backplane in lieu of other traffic. This custom board is designed to overcome this problem by acquiring and processing the signal in one place, with the processed result presented at the VME interface instead of the raw data. The board consists of multiple front-end signal conditioners / digitizer cards plugged into the foundation 6U VME board with an embedded digital signal processor (DSP). The DSP is programmed in C to process the raw signal any way the user wants before writing results into a VME register map. The present front-end conditioner / digitizer cards are being designed with the LANSCE low momentum detector in mind, but other variations on this card could be developed. The architecture is flexible enough to deploy in many accelerator applications.

INTRODUCTION

Powerful, low cost digital signal processors (DSPs) and field programmable gate arrays (FPGAs) have made it feasible to design a single hardware platform from which many accelerator instruments may be launched. Since these devices are reconfigurable / reprogrammable, the same circuit board that is used with a low momentum detector [1] today can be redeployed as part of another diagnostic in the future.

It has been recognized that the application of a single VME board to various accelerator applications might require conflicting analog front-end specifications. To solve this problem, the board has been designed to accept up to eight analog and mixed signal front-end plug in cards. These cards have analog amplifiers, filters, analog to digital converters (ADCs), and perhaps other unanticipated circuitry for future instrument applications.

ARCHITECTURE

The platform was designed to work with the EPICS control system as it exists at LANSCE [2]. In this case, the LANSCE control room operators and scientists are faced with controlling the accelerator through EPICS displays that update at a 1 Hz to 10 Hz sample rate. At the same time an effective DSP-based accelerator instrument must sample information at rates in the tens of MHz. This bandwidth gap is compensated for with processing capability on the VME board so that high-speed data from an instrument can be reduced in hardware and presented to EPICS as a low bandwidth result. This allows an instrument to have a real-time control room display that looks "alive".

Otherwise, digitized data would have to be transferred from front-end digitizers to a commercial processor in the VME crate or over the network to a general-purpose computer in the control room. Neither of these options is desirable because these techniques require processing of data offline in batches and would not result in real-time update of displays.

VME Board

The VME board is a 6U size module that accepts up to eight custom analog / mixed signal front-end cards. A dedicated ALTERA 20K100E FPGA and a 64Kx18 FIFO support individual front-end cards. These blocks of front-end hardware are linked by a common bus to an Analog Devices ADSP-21161N floating point DSP. Another FPGA that contains a VME interface links this board wide bus to the VME bus. A 25 MHz clock is distributed board-wide and then multiplied by phase locked loops in the DSP and FPGAs. An architectural block diagram appears in figure 1.
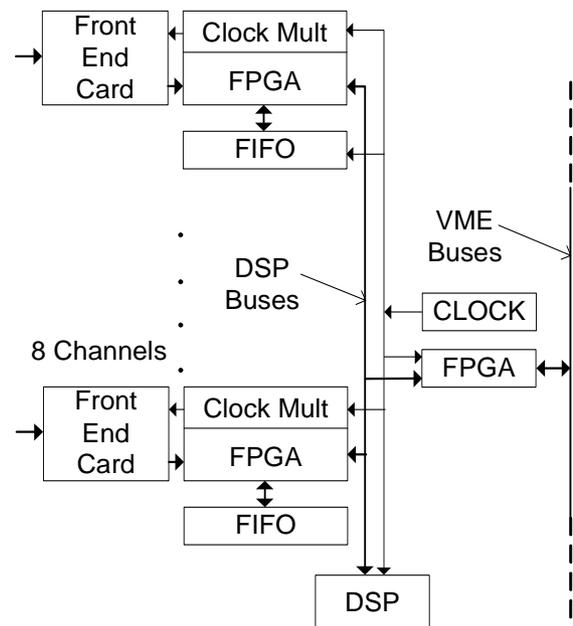
Figure 1: VME board architecture.

There are 28 bits of configurable I/O between the front-end card and the FPGA. The FPGA can boost the board wide clock up to 200 MHz for use within the FPGA and front-end card electronics. There is a clock output from the FPGA to the front-end card for use as an encode signal for an ADC and other digital hardware.

The embedded DSP operates at a core frequency of 100 MHz. The processor can execute between 1 and 4 floating-point instructions in a single 10 ns cycle.

The VME interface is implemented in an Altera 20K30E FPGA. This FPGA is less than 10% utilized with the VME interface hardware and may be used as a reconfigurable hardware coprocessor for the DSP.

Not shown in figure 1 is a board wide hardware trigger from the front panel.

Front-End Cards

Two types of front-end cards have been designed. The *fast front-end card* is capable of digitizing at rates between 50 MHz and 200 MHz using a 10-bit Analog Devices AD9410 ADC. A two-stage amplifier and 2 pole anti alias filter condition the signal before it is digitized. The analog section of the card has shown a fairly flat response up to 40 MHz on the test bench with its over all gain set to 20. The card accepts a clock from the VME board to set its digitization rate. In order to achieve this speed, it needs two digital output buses, each running at half the full sample rate. The user has the freedom to adjust the amplifier gain, filter cutoff frequency, and ADC conversion rate to suit a particular application.
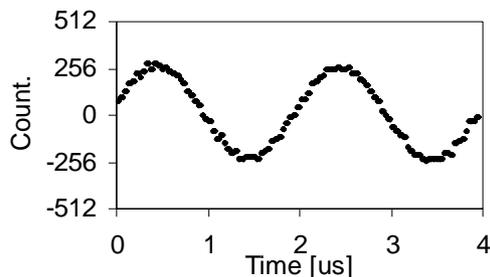
Figure 2: Digitized (measured) test waveform.

The fast front-end card has been prototyped in the lab and tested end-to-end using a waveform generator to supply an input signal and a logic analyzer to acquire the digital data at the back end. The measured data captured with a logic analyzer is shown in figure 2. Here the card was configured with a gain of 40 and a 10 MHz filter cutoff frequency. The ADC was clocked at 50 MHz and a 10 mV, 500 KHz input signal was applied. The figure shows a clearly reconstructed digital version of the input signal. Noise is less than 1 mV.

A second *medium speed* front-end card can digitize at speeds up to 10 MHz with 14 bits and has a programmable amplifier that conditions the signal before it reaches the ADC. The gain can be set with the programmable I/O between the VME board and this front-end card.

APPLICATIONS

The linear accelerator at LANSCE supports several experimental areas at the same time. It does this by multiplexing beam pulses intended for different destinations. Diagnostic instruments are often required to de-multiplex beam data depending on the destination for each beam pulse. The beam pulse destination is locally referred to as its *flavor* [3]. This board supports timed and flavored data with board wide hardware and software triggers from the LANSCE master timing system.

Low Momentum Detector

The platform is first being applied to the LANSCE Low Momentum Detector. This is a diagnostic used during tuning to identify low momentum tails in the linear accelerator. This is done by examining the output of a multi-wire proportional chamber placed at a high dispersion point near a bending magnet. Fast pulses are produced on each of these wires when beam is incident on them. These pulses have to be processed into a spectrum of beam current vs. momentum for display in the LANSCE control room.

When integrated, the pulses are proportional to the number of protons incident on each wire. Integrals then must be averaged over time to convert results in Coulomb units into beam current in Amperes.

Scientists in the control room will want to see an EPICS display with a real-time spectrum of beam current vs. beam momentum as they tune the accelerator. They will use this "live" picture as feedback when they manually adjust accelerator controls in an attempt to remove unwanted beam components. Occasionally they may want to see the beam structure by viewing a waveform record containing the raw digitized data.

This VME board is applied to the low momentum detector problem by assigning a fast front-end card to each of the wires in the detector so that pulses can be digitized at 50 MHz. The digital data is integrated at the full sample rate in the dedicated FPGA and then averaged in the DSP to compute the measured beam current in each wire of the detector. The FIFO memory retains the last 64K samples that have been digitized. Normal processing may be suspended to transfer the FIFO contents to an EPICS display. An architectural block diagram showing this specific configuration appears in figure 3.

The FPGA associated with each front-end card is configured with two digital integrators, one for each output bus of the AD9410 ADC. Analysis with Matlab / SIMULINK using real input data has shown that a 20-bit result bus is sufficiently wide for this application.

When operated at capacity, the LANSCE accelerator has a 120 Hz beam pulse repetition rate. This means that results may be transferred out of the digital integrators at this rate, effectively reducing the bandwidth of the data stream from 50 MHz to 120 Hz without discarding any information.

120 Hz, however, is still out of band for EPICS and the data must be averaged over time anyway to convert from Coulombs to Amperes. The DSP collects these results at
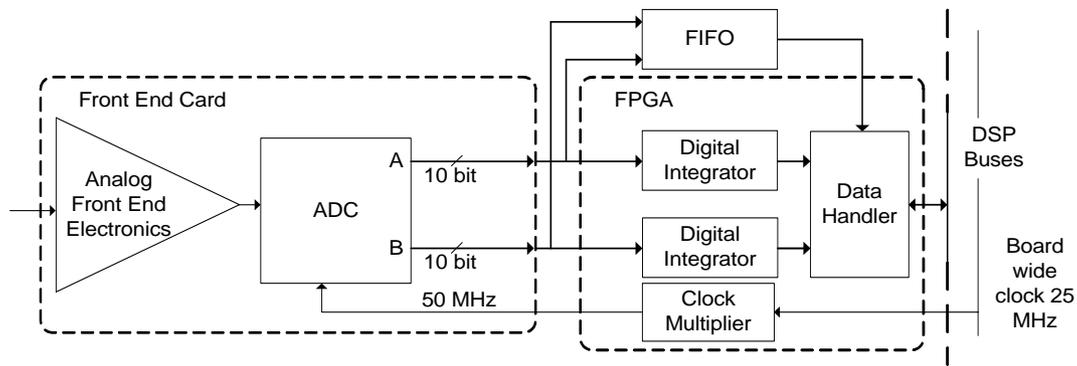
Figure 3: Application specific configuration of the FPGA with the fast front-end card.

120 Hz, computes averages for each wire, and low pass filters the result to further reduce the bandwidth to less than the EPICS update rate.

Control room operators will also need to see current spikes on their displays that may occur with durations too short to be observed with even the fastest EPICS update rate. The DSP will be programmed to detect these spikes in real-time and hold them long enough to be effectively reported through EPICS.

In figure 3, a data handler is shown designed into the FPGA. This is an interface between the front-end electronics and the DSP. It orchestrates the flow of data between the ADC, FIFO, integrators, and the DSP bus.

HARP

A new Isotope Production Facility (IPF) is being commissioned at LANSCE. The transport line to the IPF will require beam position diagnostics. A HARP is a diagnostic used to determine the beam centroid that uses horizontal and vertical wires in the beam.

For the HARP, configuration and programming of this VME board will be similar to the low momentum detector application. In this case, the DSP may also be programmed to partially compute the beam centroid before with the final result is computed by software running in the IOC.

Beam Loss Monitoring

Beam loss monitoring generally involves threshold discrimination and then counting pulses [4]. Count totals are averaged over time to produce a beam loss rate at various locations in the accelerator. One of the front-end cards that have already been designed may be immediately applied to threshold detection. Counting can be done on the associated FPGA. In this case the threshold could be adjusted automatically under the control of the DSP. Additionally, a new front-end card could be developed to convert the raw analog pulses directly into the digital domain without an ADC.

Beam Position Monitoring

The floating point DSP used on this board lends itself to the Δ / Σ type computation common in beam position monitoring (BPM) applications. Depending on the nature of the BPM, one of the existing front-end cards could be used, or an RF front-end card could be developed [5].

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