A MULTIWIRE PROPORTIONAL CHAMBER SYSTEM FOR MONITORING LOW MOMENTUM BEAM IN ACCELERATORS*

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Abstract

A diagnostic is being developed at the Los Alamos Neutron Science Center (LANSCE) for the purpose of identifying low momentum beam tails in the linear accelerator. These tails must be eliminated in order to maintain the transverse and longitudinal beam size. Instead of the currently used phosphor camera system, this instrument consists of a Multi Wire Proportional Chamber (MWPC) front end coupled to an EPICS compliant VME-based electronics package. Low momentum tails are detected with a resolution of 5 mm in the MWPC at a high dispersion point near a bending magnet. While phosphor is typically not sensitive in the nano amp range, the MWPC is sensitive down to about a pico amp. The electronics package will process the signals from each of the MWPC wires to generate an array of beam currents at each of the lower energies. The electronics will have a wideband analog front end, active anti alias filter, and high-speed analog to digital converter for each wire. Data from multiple wires will be processed with an embedded digital signal processor and results placed in a set of VME registers. An EPICS application will assemble the data from these VME registers into a display of beam current vs. beam energy (momentum) in the LANSCE control room. This display will update at least once per second, but will be a representation of the real time signal processing results from the electronics package.

INTRODUCTION
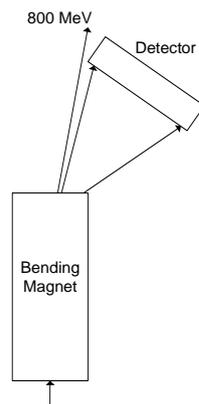
Beam from the linear accelerator is transported to

Figure 1: Position of detector with respect to bending magnet.

several different experimental areas by a set of bending

magnets in the LANSCE switchyard.

Optimally, beam entering the switchyard should be at 800 MeV when the accelerator is properly tuned. Before accelerator tuning is complete, there are often unwanted beam components at energies below 800 MeV that need to be removed. These low energy components are bent in a radius that is too tight to allow them to continue to the experimental areas and fall out and hit a beam stop. The lower the energy, the tighter the bending radius is. The low momentum detector is placed between a bending magnet and a beam stop so it can measure the magnitude spectrum of beam currents over a range of unwanted low energies.

IONIZATION CHAMBER

The chamber is constructed using ¼" G-10 fiberglass for its frames. It has an active area of 300 sq. cm. (50 cm x 6 cm). There is one frame with wires (64 gold plated tungsten of diameter 20 micron) stretched at 5 mm spacing and two frames with 1 mil aluminum foil on either side of the signal frame for high voltage. The whole assembly is enclosed in an aluminum box with 1 mil aluminum windows covering the active area of the detector. The gas is a mixture of argon-methane (90-10). The signal wires (twisted pair) are connected to a vacuum tight connector attached to the box. The signals from each wire indicate a particular energy beam tail that has to be minimized to achieve an optimum tune for the accelerator. The signals from the wires are fast enough to identify the loss across the macro-pulse of the beam.

SIGNAL

Data is taken from each detector wire to construct a spectrum of beam currents over a range of beam energies from 350 MeV to 750 MeV. Each wire corresponds to a particular unwanted energy component. The wire's relationship to that energy depends on its position in the detector. A sketch of the detector appears in figure 2 [1].

When protons are incident on one of these wires, a current is produced according to equation 1.

Figure 2: Detector

$$I = \frac{N \cdot \Delta E \cdot 1.6 \times 10^{-19}}{I_P} \qquad (1)$$

Where I is the current produced in amperes and N is the number of protons per second that are associated with the wire. ΔE is the energy lost in the detector and has been calculated to be 15 eV through a LANDAU simulation [2]. Ip is 12 eV, the ionization potential of argon and 1.6 x 10^{-19} is the charge of a proton. When 10^6 protons are incident on a wire, a current of 0.2 pA is produced which is amplified due to the effect of the ionization chamber by 10^9 [3]. The result is a current of about 0.2 mA, which is readily measurable.

Figure 3 shows part of a typical signal produced in one of these wires when terminated into 50Ω. The electronics package must integrate this signal over time so that the beam current incident on the wire can be computed.
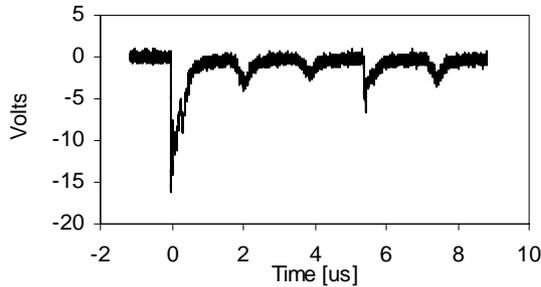
Figure 3: First 8 μs of raw signal from a single detector wire.

This signal is typically 625 μs long, corresponding to the length of the LANSCE beam gate. However, gates as long as 1 ms must be supported. Beam gates occur at a maximum rate of 120 Hz at LANSCE, which means that the electronics package has (1/120Hz – 1 ms) = 7.3 ms to recover from a beam gate.

BANDWIDTH

In figure 4, a frequency analysis of the raw signal reveals three prominent peaks at 559 KHz, 1.1 MHz, and 1.47 MHz.

The electronics must then be sufficiently fast to capture this information. The analog front end has a bandwidth that has been limited to 10 MHz using a 2-pole anti-aliasing filter. The output of that filter is sampled at 50 MHz.

Another bandwidth consideration is that of the EPICS control system in which this instrument will be used. Operators in the LANSCE control room will see their EPICS-based displays update at frequencies between 1 and 10 Hz. This instrument must bridge the bandwidth gap between the 50 MHz data collection and the relatively slow update rate of the control room displays without losing data. It must also do this in real time, meaning the displays in the control room must look "alive" all the time

so that control room operators are comfortable using the instrument [4].

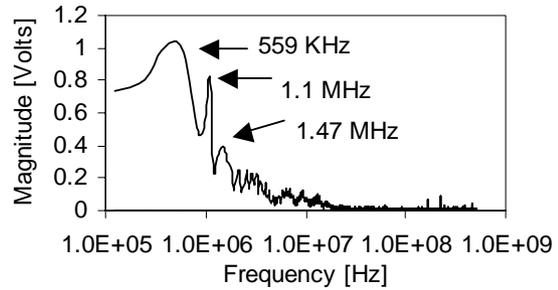Figure 4. Frequency components of input signal.

ARCHITECTURE

Data that is sampled at 50 MHz at the front end of the instrument is processed in two stages so that a useful, low bandwidth result can be presented to the EPICS control system. At each stage the signal is processed in a way that reduces its bandwidth without discarding information about the signal.

Each wire in the detector has a dedicated section of electronics called the "front-end" associated with it. In the front-end, data is processed by analog and digital hardware to compute an integral at the full sample rate of 50 MHz. However, the signal that is being operated on lasts for less than 1 ms and has a repetition rate of 120 Hz. This means that processed results can flow out of the front end at 120 Hz, which is at a much slower rate than the 50 MHz input data.
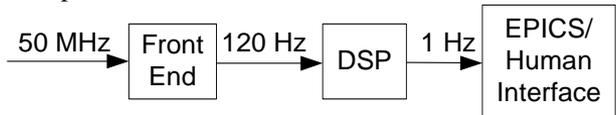
Figure 5. Data processing stages.

The 120 Hz signal is processed further in a DSP before it is presented to EPICS. When the signal is processed in the first stage, a result in Volt-second units is computed. That result has to be converted into charge in Coulombs and then averaged over time for a beam current result in Amperes. The averaging operation reduces the bandwidth of the signal to less than 1 Hz. EPICS can then properly handle this in real-time. A block diagram showing the data flow through the two bandwidth-limiting stages appears in figure 5.

ELECTRONICS

The electronics package consists of a 6U VME board coupled with mixed signal front-end boards suited to the low momentum detector application. The front-end electronics is the mixed signal front-end card and its associated dedicated hardware. There are eight front-ends on each 6U VME card. Since this instrument needs to support 64 wires with 64 front-ends, eight VME cards are required.

Each board has an embedded floating-point digital signal processor (DSP) and a VME interface, which is implemented in a field programmable gate array (FPGA). This FPGA contains only the VME interface, but since just a fraction of its resources are utilized, it could be configured as a hardware coprocessor to the DSP for applications with another type of instrument. The eight front-ends, the DSP, and the VME interface are connected to each other with board wide data, address, and control buses. A block diagram of the VME board architecture is shown in figure 6.
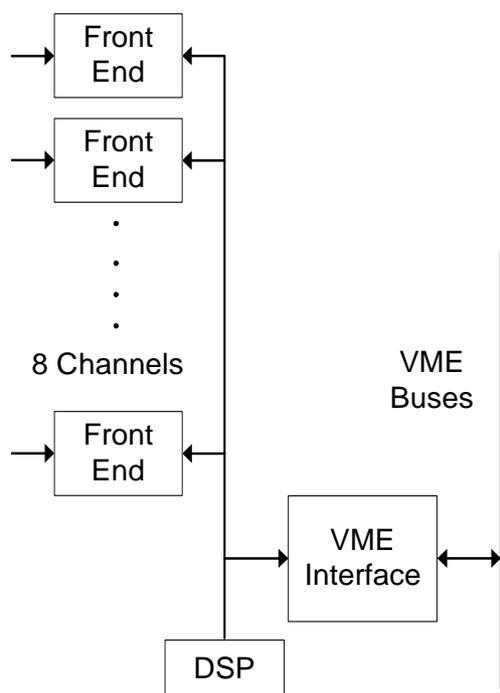

Figure 6. VME board architecture block diagram.

Front End Card

A block diagram depicting the relationship between the front-end card and the VME board is shown in figure 7. The signal from each wire is processed first by the section labeled "analog FE". This is the analog front end, consisting of a two-stage amplifier and a low pass anti-alias filter. The front-end card has on board a 10-bit analog to digital converter (ADC) that is configured to sample at 50 MHz, but can run at speeds up to 200 MHz for other applications [5].

VME Board

The digital hardware for the front end is implemented on the VME board. The underlying VME board accepts eight front-end cards and provides processing support using dedicated FPGAs and one board wide DSP. This board also has first-in-first-out (FIFO) memories to buffer high-speed data so that the raw waveform can be transferred from this instrument to a display in the control room if required.

Although the FPGA dedicated to each front-end is currently configured to be a fixed-point integrator, it may be configured differently for other applications. The digital integrator processes data from the ADC in real time. The integrator can handle signals up to 0.8 µV-seconds while the measured worst case integral from a real signal is about 0.3 µV-seconds.

OPERATOR INTERFACE

Result data from this instrument will be in the form of a magnitude spectrum graph of beam current vs. beam momentum. The graph will show how many protons / second are incident on each of the detector wires. The graph will update at up to 10 Hz, for a "live" look. Data transfer from the VME card to the operator's computer screen will be fast because only 64 processed results need to be sent, but not any raw data.
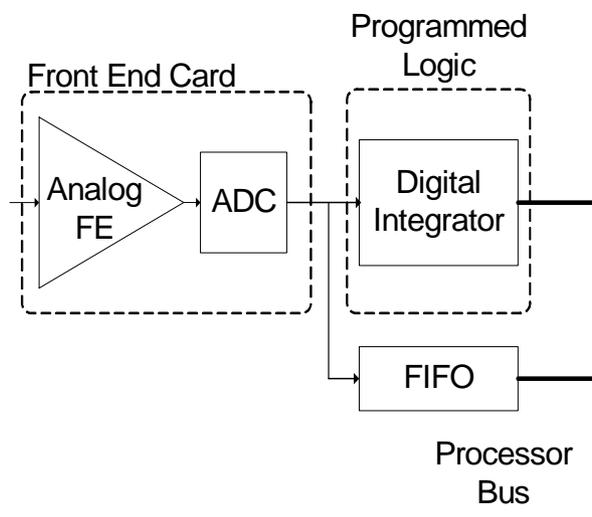

Figure 7. Block diagram of front-end electronics.

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[3] T. Ferbel, "Frontiers in Physics", Addison-Wesley, Reading MA, 1987.
[4] Mark McMillen, Los Alamos National Laboratory, private communication.
[5] R. Merl, F. Gallegos, C. Pillai, F. Shelley, "High Speed Epics Data Acquisition And Processing On One VME Board", PAC 2003, Portland OR, May 2003.