THE LOW LEVEL RF SYSTEM FOR 100MV PROTON LINAC OF KOMAC*

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Abstract

At the 100MeV proton linac of the KOMAC(Korea Multi-Purpose Accelerator Complex), the low level RF system provides field control for the entire KOMAC proton linac, including an RFQ and a DTL1 at 350MHz as well as 7 DTL cavities at 700MHz. In addition to field control, it provides cavity resonance control, and incorporates the personnel and machine protection functions. An accelerator electric field stability of ± 1% in amplitude and ± 1° in phase is required for the RF system. In order to accomplish these requirements, a digital feedback control technique is adopted for flexibility of the feedback and feed forward algorithm implementation.

In this paper, the detailed description of the low level RF system will be described .

1 INTRODUCTION

The KOMAC accelerator has been designed to accelerator a 20mA cw proton/H- with the final energy 1GeV CW super-conductive linear acclerator. As the 2nd phase of the project, we are developing cw accelerating structure up to 20MeV, and operate the accelerator in 10% duty pulse mode. After the initial operation, we will challenge the cw operation of the linear accelerator. The 20MeV proton accelerator is constructing in the KTF(KOMAC Test Facility), and will be commissioned in 2005. After the commissioning, KTF will provide the proton beam for the many industrial applications. With the technologies developed in KTF, the 2nd phase accelerator of 100MeV final energy will be constructed in 2010. The final goal of this phase is 100MeV proton accelerator.

In the 100MeV proton linear accelerator(LINAC) for KTF, the RF source will power two accelerator cavities (an RFQ, a DTL1) operated at a frequency of 350MHz, and five cavities(DTL2) operated at a frequency of 700MHz.

The low level RF(LLRF) system for 100MeV proton linear accelerator provides field control including an RFQ and a DTL at 350MHz as well as 7 DTL cavities at 700MHz. In addition to field control, it provides cavity resonance control, and incorporates the personnel and machine protection functions. An accelerator electric field stability of ± 1% in amplitude and ± 1° in phase is required for the RF system. In order to accomplish these requirements, we will employ digital feedback control technique adopting flexibility of the feedback and feed-forward algorithm implementation.

2 MASTER OSCILLATOR & RF GENERATOR

Figure 1 shows the block diagram of the master oscillator and RF generator included clock. The 10MHz RF reference is distributed to 9 low level RF systems. As shown in the figure, the electrical RF reference signal (10MHz, sine) generated by a master oscillator (external reference oscillator) is divided into 18 way by divider and amplified individually.

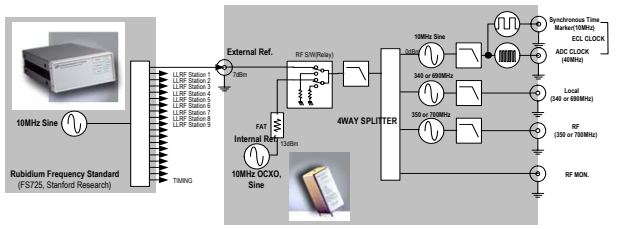

Fig. 1. A block diagram of the master oscillator and RF generator included 40MH ECL clock for 100MeV linear accelerator

In order to maintain the correct accelerating field of RF source within an amplitude error of ±1%, and a phase error of ±1°, a digital feedback and feed-forward control system with high intelligence is required. Therefore, the RF reference signal, which is distributed to all of the RF stations included klystrons, should be more highly stable.

	Internal(LLRF)	External (Master Oscillator)
Model No./Mfg's name	SC10/SRS	FS725/SRS
Output Frquency	10MHz Sine	10MHz Sine
Phase Noise(SSB)	< -120dBc(10Hz) < -150dBc(100Hz) < -155dBc/Hz(1kHz)	< -120dBc(10Hz) < -140dBc(100Hz) < -150dBc/Hz(1kHz)
Stability	< ± 0.002ppm	< ± 0.00005ppm
Operating Temp.	0 to +50°C	+10 to +40°C
Freq. Tuning	±3Hz	±0.02Hz(0 to 5VDC)
Spurious		< -100dBc(100KHz BW)
Harmonics		< -60dBc

Table 1. The characteristics of the internal RF reference and external RF reference

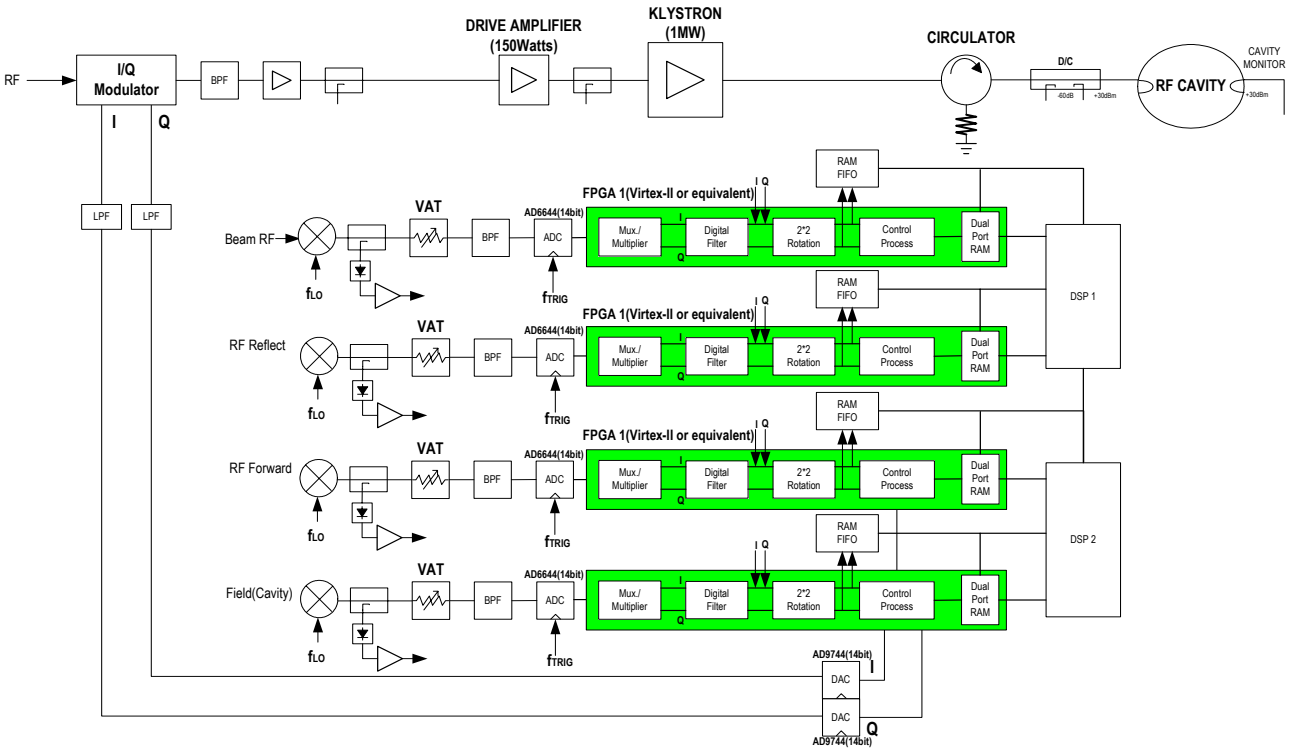

Fig. 2. A block diagram of the digital feedback hardware

Our goal for the RF reference is at within ±0.1° for the phase stability. The characteristics of the internal RF reference and external RF reference are shown in table1. One stabilized coaxial line provides the RF reference for each RF stations (RFQ, DTL1, DTL2). The LLRF system was designed to make use of a 350MHz(or 700MHz) RF, 340MHz(or 690MHz) LO, 40MHz ECL clock, 10MHz synchronization. The accelerator source RF(klystron driving signal) of 350MHz or 700MHz is generated by a VCO with PLL synchronizing with the distributed 10MHz reference at each local station.

3 DIGITAL FEEDBACK HARDWARE

For the 100MeV proton LINAC of the KOMAC, the error of the accelerating field must be within ± 1° in phase and ± 1% in amplitude. To stabilize the amplitude and phase of the field in the accelerator cavity, a digital feedback and feed-forward technique is used in the LLRF system. Figure 2. shows a block diagram of the digital feedback hardware in the LLRF. This system controls I/Q components of the RF signal as shown in Fig. 2. The feedback and feed-forward control is performed by a combination of FPGAs(Field Programmable Gate Array) for fast and simple then feed to the appropriate carrier RF signal prior to amplification by the klystron. As shown in Figure 2., the RF signals from the cavity field probe, forward power, and reflected power are down-converted to 10MHz IF and sampled at 40MS/s by individual 14bit ADCs with 40MHz ECL clock in order to produce quadrature I, Q, -I, -Q samples. These are then properly updated at 20MS/s by two multipliers, and filtered. Once filtered, they are compared to set-point tables and control algorithms are performed to control an RF vector(I/Q) modulator.

	XCV1000E (Virtex-E)	XC2V1000 (Virtex-II)	XC2VP30 (Virtex-IIPro)
System Gate	1.57M	1M	
Logic Gate	331,776		30,816 Logic Cells
CLB Array	64×96	40×32	
CLB Slice		5120	13,696
CLB Max. Distributed RAM Kbits	393	160	428
Multiplier Blocks		40	136(18×18Bit)
SelectRAM Blocks Max. RAM(Kbit s)	393	720	2,448
Features	*fast high density *high flexible select I/O *0.18um 6layer metal process	*selectRAM memory hierarchy *Select I/O-ultra *PCI/XPCI compliant *0.15um 8layer metal process 0.1um high speed transistor	*high performance platform *selectRAM memory hierarchy *power pC RISC block *Select I/O-ultra *PCI/XPCI compliant *0.13um 9layer copper process 90nmm high speed transistor

Table 2. Xilinx FPGA's comparison

The digital feedback hardware relies on FPGA(Field Programmable Gate Array) and digital signal processors optimised for real-time signal processing. Table 2. shows the Xilinx FPGA's comparison. The digital feedback hardware performs feedback and feed-forward algorithms on the field signal, resulting in control in phase and quadrature(I/Q) outputs, which are processing and DSPs(Digital Signal Process) for slow and complicate

processing. A windows OS system will be used as an integrated development environment in order to make it easy for us to develop the software of FPGAs, DSPs and a CPU host.

4 CONTROL & INTERFACE

The control parameters are set through the EPICS(Experimental Physics Interface Control System) interface allows the operator to set up the LLRF system, in a variety ways. Registers on the module provide access to all manners of control – set points, thresholds, mode selection, controller type, etc, and the DSPs provide the direct interface to the control register and hardware. A network host computer connects the fast signal processing chip to outside world via Ethernet. Timing and interlocks are routed through an FPGA. Fig. 3. shows the interface of the RF station for the RFQ, DTL1, DTL2.

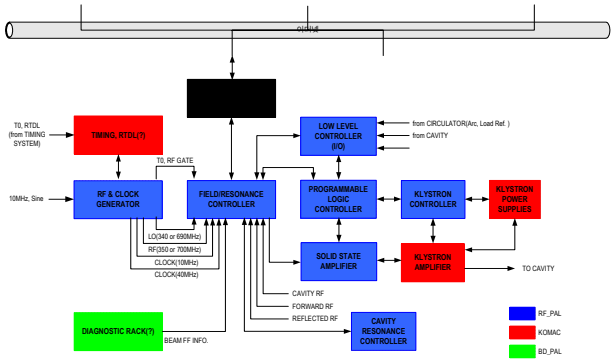

Fig. 3. The interface of the RF station for the RFQ, DTL1, DTL2.

5 SUMMARY

Recent technology in System on Chip(SoC) has enable to develop high-density FPGA devices that suited to the needs of high performance real-time signal processing. With the addition of embedded processor cores and powerful IO interface they provide a valuable combination of high performance and configurability. The 100MeV proton LINAC for KOMAC requires an RF stability of ± 1% in amplitude and ± 1° in phase. In order to satisfy these requirements, a completely digital feedback system to provide flexibility in the control algorithm, precise calibration of the vector sum, and extensive diagnostics and exception handling capabilities is required.

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