R&D WORKS ON 1MHZ POWER MODULATOR FOR INDUCTION SYNCHROTRON

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Abstract

A proof of principle experiment of an Induction Synchrotron [1,2] is scheduled in 2003 at the KEK 12GeV-PS. Proton bunches are accelerated with a 10kV of rectangular shaped induction voltage. An accelerating system consists of four induction cavities capable of individually generating a 2.5kV of output voltage. Each cavity is driven by a solid-state power modulator, which is operated at a revolution frequency of 600-800 kHz. The modulator circuit consists of MOS-FETs as switching element.

Uniformity in the voltage waveform is crucial for the stable acceleration. Ringing in the voltage waveform caused by coupling of self-inductance of circuit and output capacitance of MOS-FETs deteriorates the uniformity. With the help of circuit analysis and simulation, method of minimizing the self-inductance has been developed. Ratio of numbers of MOS-FETs in series and in parallel which defines the total output capacitance is also important to design the power modulator circuit.

Power loss in MOS-FET is also important for stable operation of the power modulator. By the circuit analysis, it is also found that the output capacitance contributes to the power loss.

1 INTRODUCTION

A novel concept of a proton synchrotron [1], referred to as an Induction Synchrotron, was proposed by K.Takayama and J.Kishiro. The Induction Synchrotron employs two types of induction cavities and power modulators [2]; one is for acceleration and the other is for the confinement of proton beams. This functional separation between beam handling and acceleration enables us to increase the beam intensity by utilizing the longitudinal phase space efficiently with an induction barrier voltage and an induction acceleration voltage.

One of the key devices of the Induction Synchrotron is a power modulator which generates a rectangular shaped voltage at a magnetic core loaded induction cavity with the same repetition rate as the revolution frequency of proton beams of up to 1 MHz.

The induction power modulator consists of four switches by MOS-FETs and composing a full bridge circuit as in DC-AC converter. The circuit of the induction power modulator and its trigger sequence is shown in Fig.1. In sequence 1) and 3) the voltage is induced at the magnetic core with non-zero value of dI/dt. In sequence 2) and 4) the primary current with dI/dt nearly equal to zero flows to the magnetic core without inducing a secondly voltage. Following those sequences from 1) to 4), a bipolar pulse voltage with the same amplitude is generated at the magnetic core.

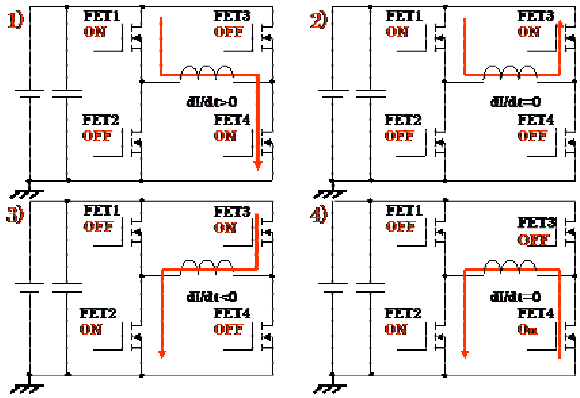

Fig. 1 : Circuit of the Induction Power Modulator and its trigger sequence

This report describes recent progress in the development of induction power modulator.

2 SPICE CIRCUIT MODEL

In a Spice model of the induction power modulator, drain current dependence on drain to source voltage of MOS-FET is characterized by Shichman-Hodges model. In this model, drain current is characterized by following two equations.

$$Id = \frac{kW}{L}\{(Vgs - Vt)Vds - \frac{Vds^2}{2}\} \qquad (1)$$

for linear region in which drain current has almost linear dependence on drain to source voltage. And

$$Id = \frac{kW}{2L}(Vgs - Vt)^2(1 + \lambda Vds) \qquad (2)$$

for saturation region in which drain current is square dependence on gate voltage. Here L is the channel length. W is the channel width. Vt is the gate threshold voltage. K is transconductance parameter. Lambda is channel length modulation. Parasitic capacitance, caused by P-N junction between p-substrate and n+ drain, is modelled by

capacitance inserted between drain and source. Spice calculation result for drain current characterization is plotted in Fig. 2. Although an error between measured and calculated results was up to 46% for lower gate voltage of around threshold voltage, we had good agreement of the order of few % with higher gate voltage of up to 15 [V]. Here the threshold voltage for modelled MOS-FET was 3.85V.

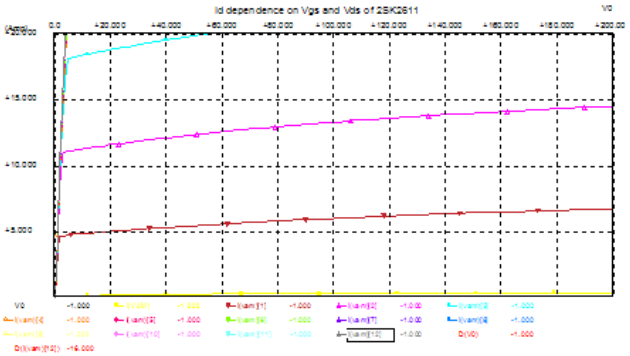

Fig. 2 : Calculated drain current dependence of modelled MOS-FET

Self-inductance of power modulator circuit should exist. For simplicity, it was inserted at typical four points as in Fig. 3.

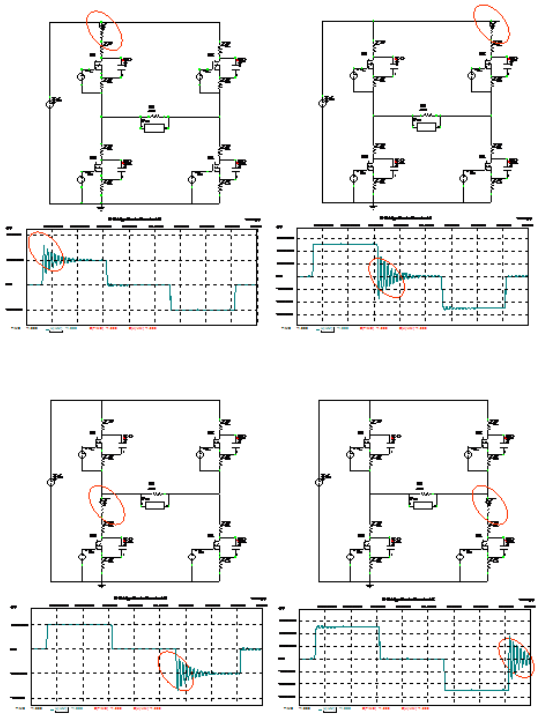

Fig. 3 : Spice model of the induction power modulator

From this calculation, it was found that the resonant coupling occurred by the output capacitance of MOS-FET and by the self-inductance of modulator circuit. As the resonant frequency is expressed by following equation, both output capacitance and self-inductance should be minimized.

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{3}$$

Total amount of output capacitance is determined by number of MOS-FETs in series and in parallel. So, to design the induction power modulator, proper choice of number of MOS-FETs in series and in parallel should be made to avoid output voltage deterioration by resonant coupling. Total amount of output capacitance is calculated as low as 25 [pF] with 7 series and 1 parallel MOS-FETs.

Numerical treatment of self-inductance is also important to design the induction power modulator. To do this, we modelled a wiring pattern of circuit as rectangular shaped wiring with its height of a [m], width of b [m] and radii of wire of r [m]. The self-inductance of this rectangular wiring is calculated as in the following equation.

$$L = \frac{\mu}{\pi}\{-a\log(a+\sqrt{a^2+b^2}) - b\log(b+\sqrt{a^2+b^2}) + (a+b)\log(\frac{2ab}{r}) + 2\sqrt{a^2+b^2} - \frac{7}{4}(a+b)\} \tag{4}$$

It is found that, by proper choice of those parameters, self-inductance of the power modulator is minimized. For a=1 [mm], b=1 [m] and r=3 [mm], calculated self-inductance is as low as 92 [nH].

With above numerically calculated parasitic elements, output voltage was simulated as in Fig. 4.

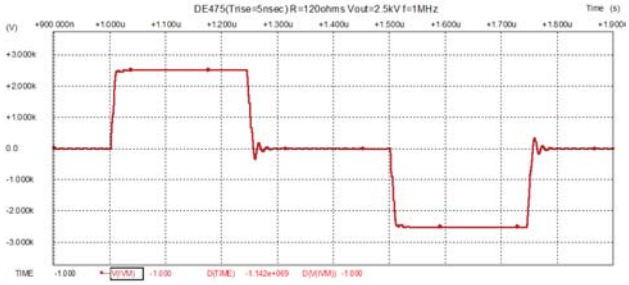

Fig. 4 : Simulated output wave form of the induction power modulator

3 THERMAL DESIGN

Stable operation of semiconductor devices requires accurate estimation of power loss and proper cooling system. By the help of Spice simulation, power loss at each of the MOS-FET was calculated as in Fig. 5.

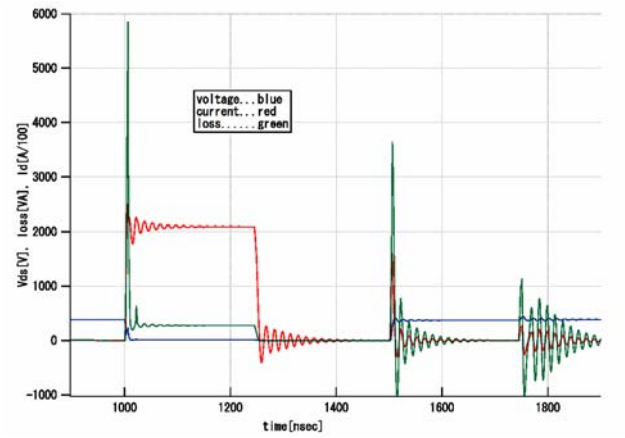

Fig. 5 : Calculated power loss at MOS-FET

As power loss is defined by following equation, it is calculated as 55 [W] for each MOS-FET.

$$P[W] = \frac{1}{T}\int_0^T V(t) \times I(t) dt \qquad (5)$$

Calculation is done with resistor load of 120 [Ω] which corresponds to an impedance of an induction cavity. We have decided to employ the indirect water cooling system for the induction power modulator after above calculation. Characteristic values of the induction power modulator are listed in table 1.

Table 1:Design values and characteristics of the Induction Power Modulator

DC Power Supply	50[kW]
Output Voltage	2.5 [kV]
Peak Output Current	821[A]
Duty of Pulse	50 [%]
Power Loss at MOS-FET	55[W]
Cooling of MOS-FET	Indirect water cooling
# of MOS-FETs in Series	7
# of MOS-FETs in Parallel	1

4 OPERATION RESULTS

The induction power modulator loaded with induction cavity was successfully operated in burst mode operation for test purpose. Repetition frequency was 500 [KHz]. Output voltage measured as gap voltage was 2.0 [kV] as in Fig. 6.

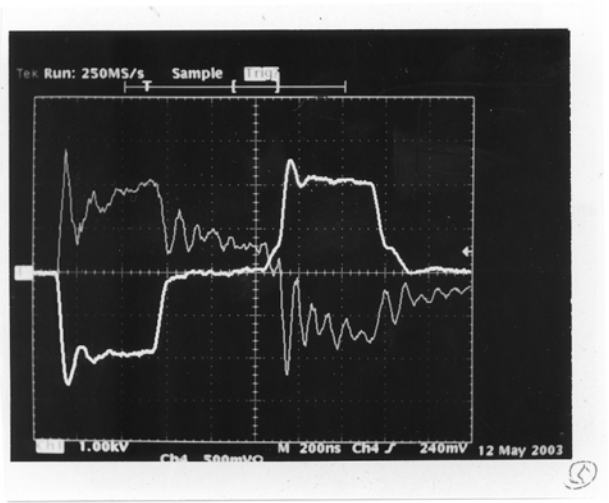

Fig. 6 : 500kHz burst-mode operation loaded with induction cavity.

5 CONCLUSIONS

An induction power modulator has been developed and successfully operated with induction cavity load in burst mode. A repetition rate of 500 [kHz] with 500 [nsec] of bipolar pulses was achieved. The output voltage measured at cavity gap was 2.0 [kV].

6 ACKNOWLEDGEMENTS

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7 REFERENCES

[1]K. Takayama and J. Kishiro, “Induction synchrotron”, Nucl. Inst. and Meth. A451/1, 304-317(2000)

[2]J.Kishiro, K.Takayama, E.Nakamura, K.Horioka, M.Watanabe, A.Tokuchi, and S.Naitoh, “Rappidly switched accelerating devices for Induction synchrotrons”, in Proceedings of EPAC2000, 1966-1968(2000).