UPGRADING THE ORBIT FEEDBACK SYSTEM IN THE TAIWAN LIGHT SOURCE

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Abstract

The global orbit feedback system plays a crucial role in the operation of the Taiwan Light Source (TLS). Various issues must be addressed to achieve maximize performance. The orbit feedback system was upgraded recently to meet increasing demand. Based upon operational experience during the last few years, a new system was designed to provide an environment for easy maintenance, real-time monitoring of performance, and trouble-shooting of the feedback loop. Highly robust and flexible controllers are now also supported. A general-purpose CPU real-time operation system has replaced the former DSP boards to reduce the resources required and provide a superior software development environment. Performance analysis tools were also developed to monitor system performance. Highly integrated Commercial Off-The Shelf products (COTS) were used to support various beam studies and evaluation of the performance of the system. The implementation of these systems is discussed herein.

INTRODUCTION

An orbit feedback system is used to eliminate orbit variation due to various sources of perturbations. Efforts to increase the stability of the orbit began in 1995, by the orbit feedback system. This orbit feedback system has been incorporated with insertion devices, including an undulator (U5 and U9) and an elliptical polarized undulator (EPU5.6). Orbit drift is suppressed and a low frequency oscillation is achieved. The orbit feedback system in the storage ring of the SRRC is being upgraded to improve its performance. This effort includes increasing the feedback bandwidth, increasing the sampling rate, compensating for the eddy current effect of the vacuum chamber with the filter, and improving the performance and robustness of the control rules. This report summarizes the status of the development of the orbit feedback in the NSRRC.

OLD ORBIT FEEDBACK SYSTEM

The old digital orbit feedback system [1,2] is a two-crate feedback system. One crate is for data acquisition; the other crate is for digital signal processing includes of controller, filters, calculates the response matrix a. The feedback controller is based on a PID algorithm. Digital filtering techniques were used to remove noise fro the reading of the position of the electron beam, to compensate for the eddy current effect of the vacuum chamber, and to increase the bandwidth of the orbit feedback loop. The infrastructure of the digital orbit feedback system consists of an orbit acquisition system, gigabit fiber links, digital signal processing hardware/software, and high-precision digital-to-analog converters.

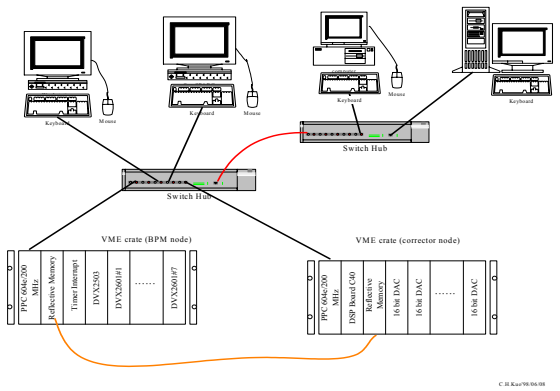

Figure 1: Original hardware environment of the orbit feedback system.

Hardware structure

The old system consists of two VME crates. One is the orbit server VME crate, others is the corrector and computation VME crate. Within the corrector and computation server, a VME bus to ISA bus adapter is used to provide PC and VME crate communication. Figure 1 shows the hardware configuration of the corrector node and the orbit node in the NSRRC. The low layer is a VME crate system that includes a PowerPC 604e CPU board and I/O interface cards. The CPU board includes a PowerPC microprocessor, 32 mega-bytes of on-board memory, an RS-232, PMC sites and Ethernet ports. The front-end devices are connected to this system via interfaces for analog I/O, digital I/O, and so on. A PowerPC-based server system is used as the TFTP file server for downloads of the OS and to mount the disk of the network file server (NFS). All application programs are stored on the disk on the server. These programs are developed and debugged at the client node to relieve the loading on the server. Embedded in the single board computer of the VME bus, the real-time multi-tasking kernel provides satisfactory performance, reliability and a rich set of system services. A new device can be easily created merely by modifying the device table file, by editing it on line. The system can automatically boot and

execute various applications in every VME node in the same operating system environment. The system timing was improved to one millisecond using a VME interrupt. The bus adapter is fit into slot 1 of the VME crate, to be as a system controller. All programs were developed and debugged on a PC and downloaded to the DSP board. The DSP board, carrying a TMS320C40 module, handled all signal processing, and included a digital low pass filter (LPF) and PID controller.

UPGRADE ISSUES

The existing orbit feedback system was a C'4x DSP based system. The DSP module was installed in the corrector control VME crate. The host computer of the corrector node handled interrupt requests and generated two trigger events that were sent to DSP. One was for vertical orbit feedback; other was for horizontal orbit feedback. The system was nearly ten years old and outdated in terms of performance, features and integration.

The demand of orbit feedback system have increased dramatically during the last decade. More BPM signals and correctors are required in the feedback loops. In particular, several insertion devices had to be able to be moved at the same time. A simple look-up table correction scheme doe not suffice for this dynamic request. The orbit feedback system had to be upgraded for several reasons, to improve the maintainability and stability of the system. The DSP board of the original feedback system is embedded in the corrector control VME crate, which situation is inconvenient for developing a feedback system. The impact of machine operation and research on the control algorithm development was a problem. Secondly, the system was implemented in 1995 with a slow DSP board; the functionality of the feedback loop was therefore limited. Not enough computing power was available to meet the increasing demand of the increasing number of BPMs and correctors. The control algorithm implement was also limited due to the computing power. In the new implementation, the feedback calculation will be performed on a separate VME crate. The feedback controller is decoupled to the feedback node processor from corrector node. The upgraded system includes three VME crates – the BPM node, the corrector node and the feedback node, as shown in the figure 5. These three nodes are connected by reflective memory. Several of the fiber link reflective memory cards are tied together by one dedicated reflective hub that simplifies the routing of the fiber link. The corrector node handles the power-supply control. The existing DSP systems have migrated to PowerPC 7410 (G4) architectures for greater performance, ease of use, and access to opening standards. The PowerPC handles feedback control, the calculation of the control algorithm and the conversion of the orbit information signal to the corrective action of the corrector. The correction value results are sent to the corrector node with fiber link. In the same time, the synchrotron event is broadcasted from BPM node and sends to corrector node and feedback node with fiber link.

The processor of feedback node handles more multi-input and multi-output controller loops in each mill-second period. Although the new-generation DSPs, such as TMS320C6201 or TMS320C6701 from Texas Instruments, can meet this request, maintenance is problematic and parts are expensive. The general-purpose CPU with a real-time OS also met our specification of feedback control, but isn't the disadvantage of DSP. The more important issue is that save time in the developing the upgrade.

The PowerPC is belong to a kind of general purpose CPU that is based on Motorola's AltiVec technology, specifically on the fourth-generation MPC74xx. Digital signal processing applications are beginning to migrate from a traditional DSP environment to a RISC environment, Motorola has been increasing the processing power of the PowerPC, to increase the speed and flexibility of an already impressive portfolio of DSPs, such as by introducing new parts from the C6000 family of Texas Instruments. Table 1 presents some of the processors available from Texas Instruments and Motorola that can be used to meet upgrade requirements in the future.

Table 1: List of processors for orbit feedback.

Manufacturer	Processor	Part Number
Texas Instruments	C6415	TMS320C6415
Texas Instruments	C6203	TMS320C6203
Texas Instruments	C6701	TMS320C6701
Motorola	7410	MPC7410

Table 2: Speed and benchmarks of DSP and PowerPC. The 7410 can perform up to 16 parallel integer calculations on 8-bit data per cycle, so the MIPS number: is 16 multiplied by 500 MHz to 8000 MIPS. Some 7410 instructions involve 8 calculations per cycle.

	C6415	C6203	C6701	7410
Clock(MHz)	600	300	167	500
Instruction Cycle (ns)	1.67	3.33	6	2
Instruction Per Cycle	1~8	1~8	1~8	1~3
Peak MIPS	4800	2400	1336	917[1]
Floating-Point Operations Per Cycle	-	-	1~6	4[2]
Peak MFLOPS	-	-	1000	2000

A first view of the performance of the processor can be obtained by comparing clock speeds and peak processing power, as shown in Table 2. Both DSP and the PowerPC solution can meet the requirements of orbit feedback. However, the PowerPC was chosen since it is to be compatible with the existing control system.

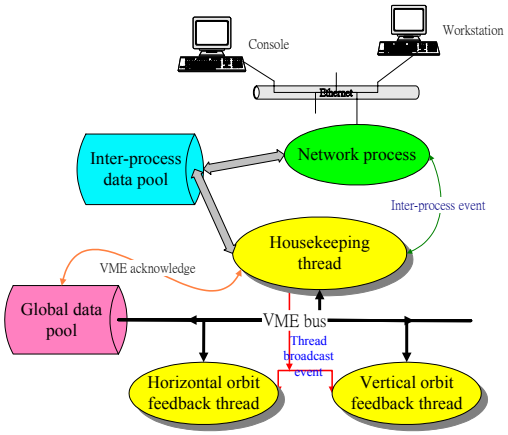

Figure 2: Relationship between software processes.

SOFTWARE TASK MANAGEMENT

The main tasks of the software in the feedback node include housekeeping, horizontal orbit control and vertical orbit control thread process. The housekeeping thread handles the transportation of control parameters; the VME interrupts acknowledge and thread broadcast events. Two orbit control threads handle global data access, digital filtering and the PID controller. The control parameters include the PID coefficient, the filter coefficient, feedback on/off and other special applications. The network process receives these parameters and saves them to the inter-process data pool from the console over the Ethernet. The inter-process data pool supports data exchange between different tasks. The global data pool handles data exchange between different VME crates and different threads. The housekeeping thread broadcasts an event to other threads when the interrupt is acknowledged from the VME bus. Two orbit feedback threads are always waiting until such an event is received. The threads are synchronized at the same time to prevent two the feedback controls of plane in the data access specifically.

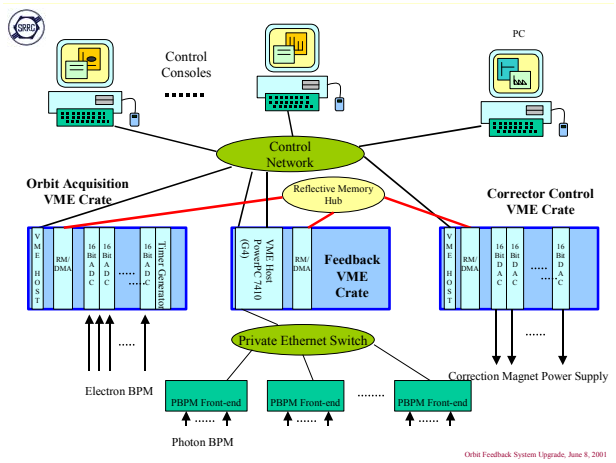

Figure. 3: Hardware structure of the orbit feedback system.

CURRENT STATUS

The new hardware structure is based on the old system. The feedback loop is divided into a VME crate separate from the original corrector node. The sub-components of the feedback node were tested successfully. These components support VME interrupt requests, VME bus access, signal processing and the controller loop. Figure 2 presents the new system block diagram. The system process rate is close to 1KHz, with two-planes orbit feedback. Figure 3 shows details the process timing. The signal in line 1 is close to 1 millisecond, which is the sampling rate of the system. Two feedback loops are processed timing simultaneously as shown in line 2 of figure 3, take 70 microseconds in two planes. This period time includes filtering, PID calculation and 60 BPM readings and 36 corrector settings. The multi-thread technique is applied to the feedback control. The latency time in the line2 of figure 3 is 50 microseconds due to bus arbitration of CPU. The threads technique keeps from processes are interfered each other. Optimization of the orbit feedback system is ongoing.

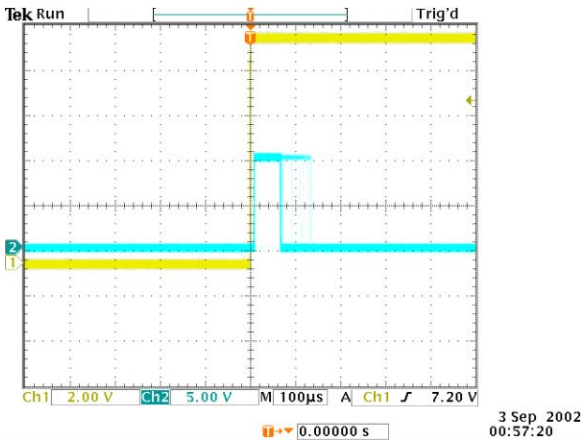

Figure 4: Timing measurement.

REFERENCES

[1] C. H. Kuo, et al., "Local Feedback Experiment in the Taiwan Light Source", Proceedings of 1997 IEEE Particle Accelerator Conference, Vancouver, 1997.

[2] C. H. Kuo, et al., "Digital Global Orbit Feedback System Developing in SRRC", Proceedings of 1997 IEEE Particle Accelerator Conference, Vancouver, 1997.