RF CONTROL SYSTEMS FOR THE TRIUMF ISAC RF STRUCTURES

K.Fong, M. Laverty, S. Fang, TRIUMF, Vancouver, BC, Canada

Abstract

The ISAC RF system consists of a radio frequency quadrupole accelerator, five drift tube LINACs, six bunchers, two choppers, and a bunch rotator. An additional buncher will be added in the near future. They run at frequencies ranging from 5.89 to 106.08 MHz, and have cavity Q values ranging from 400 to in excess of 5000. All have to run synchronously and be individually amplitude and phase regulated. A novel system that provides closed-loop amplitude, phase, and tuning control for each cavity using a single feedback circuit is employed. This system, as well as the frequency synthesis and distribution system, is described in this paper.

1 INTRODUCTION

An earlier version of the basic RF control system for the RFQ was documented in a previous paper[1]. It also shares some elements with the prototype design for the prebuncher[2]. Since that time, the frequency distribution system has been added, the DTL linacs have been commissioned, and the bunchers and choppers brought online. As well, a number of basic design changes involving both hardware and software have been introduced, some of which have been retrofitted to the prebuncher and RFQ control systems.

2 FREQUENCY DISTRIBUTION SYSTEM

A block diagram of this system is shown in Figure 1.

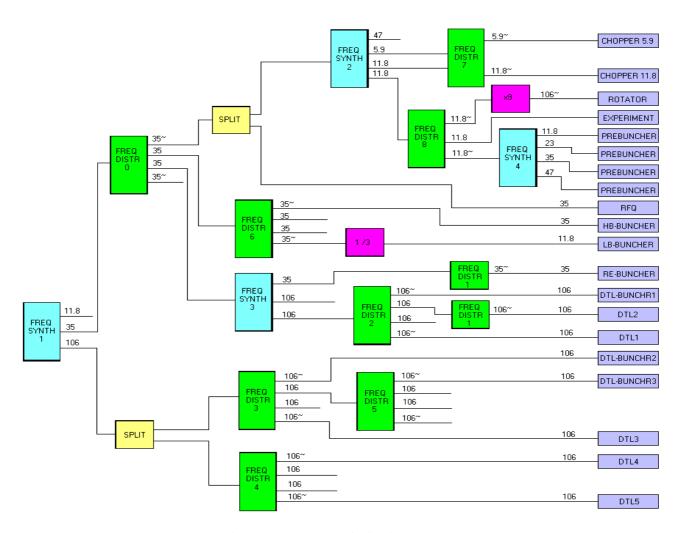


Figure 1 – Frequency Distribution System

Each of the blocks in this system corresponds to a VXI module with the exception of the coaxial splitters. Frequency synthesizer 1 uses a 10 MHz crystal reference oscillator which is multiplied to 80 MHz. A direct digital synthesizer uses this reference to provide the 35 MHz principle frequency for the RFQ with a resolution of 6 Hz, as well as a third harmonic. Since this is the first accelerator in the system, its reference frequency is used as the base for all of the other derivative frequencies. The remaining frequency synthesizer modules use various combinations of harmonic generation for multiplication, and digital or phase-lock-loop dividers for frequency division.

The frequency distribution modules provide buffered, as well as software adjustable phase shifted outputs, for one or two input frequencies. An I/Q modulator is used to provide both amplitude and phase control. The latter provides phase shift over a range of 800 degrees in approximately 0.1 degree steps.

3 RF CONTROL SYSTEM

A block diagram of the overall system is shown in

Figure 2, while Figure 3 shows the RF controls in more detail

A typical RF control system consists of a desktop PC, a VXI slot zero control module, and two custom modules housed in a VXI mainframe. The VXI mainframe provides a clean environment for the two modules which handle analog signals. One of these provides the RF modulation and demodulation function, while the second performs digital signal processing of the demodulator signal. Feedback loop regulation, requiring high signal bandwidth, is performed on-board using Motorola digital signal processors. Supervisory tasks, which require low signal bandwidth but relatively complex decision logic, are performed with the desktop PC. Communication between the PC and the VXI mainframe is done via a FireWire (IEEE 1394) interface. A control system typically consists of 4 loops: a phase-locked loop for phase stabilization, an in-phase and a quadrature-phase regulating loop for RF amplitude/phase regulation, and a cavity tuning loop for proper impedance matching to the RF amplifiers.

Up to 4 independent RF systems can be controlled by a single control PC and associated VXI mainframe.

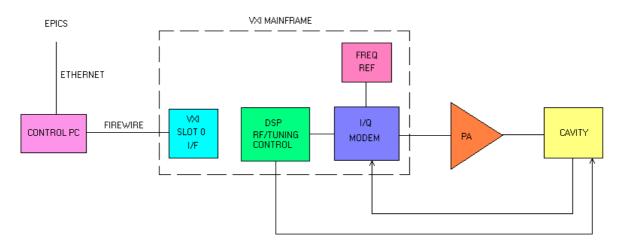


Figure 2 – System Block Diagram

4 CAVITY TUNING SYSTEM

The cavities are tuned by a grounded capacitive plate extending inside the cavity. The plate is moved in or out by a leadscrew connected to a stepping motor. The cavity tuning system make uses of the fact that the RF phase around the I/Q loop at resonance is an integer multiple of 360 degrees. At resonance, the Q input to the feedback controller is zero and the Q modulation is zero. As the cavity detunes, the detuning is manifested as the presence of signal at the Q input when the Q loop is opened, or the presence of Q modulation when the loop is closed. The weighted sum of the input and the output of the Q PID is used as the error signal for the tuner controller.

5 SYSTEM SOFTWARE

There are two distinct software designs incorporated in this system. One is the low level feedback control firmware for the DSP. In order to be able to achieve the highest processing speed this software is hand coded in assembler. It performs open and closed loop regulation, output limiting, as well as exchanges of status information with the supervisory processor. The supervisory processor performs the tasks of automatic power up sequencing, local status display, and communication with the remote EPICS-based master control system. Since each VXI mainframe can house up to four RF control systems, the supervisory processor can have up to five tasks running that are related to RF control. These

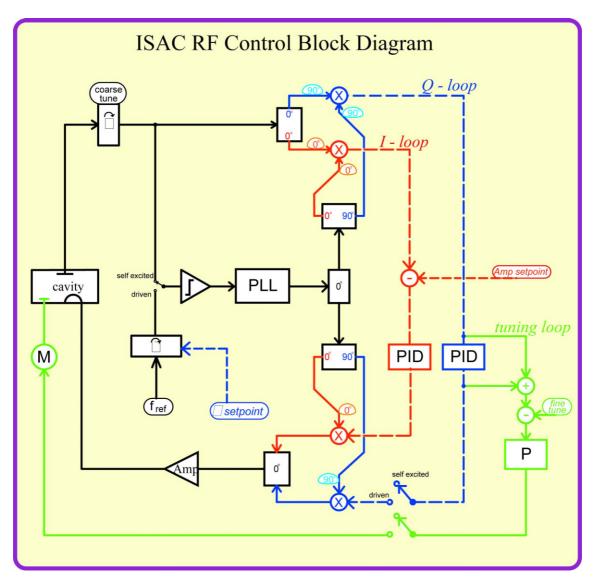


Figure 3 – RF Control Block Diagram

include a separate task for each control system, and a task to control the tuning status and phase shifts to these four systems. All the tasks are written using 32 bits C++ with Windows API's. Inter-task communication was originally performed using dynamic data exchange, but process instability forced the abandonment of this method, and the more stable method of UDP/IP packets is now used. Communication with remote control also uses UDP/IP for parameters that are to be updated frequently, such as setpoint slewing. TCP/IP is used for controls that are accessed less frequently, such as ON/OFF switching.

6 CONCLUSION

The system as described in this paper has been constructed, tested, and commissioned. The commissioning experience is the subject of another paper at this conference [3]. One potential problem with the frequency distribution system that was noted owes its

source to the use of the 35 MHz RFQ frequency as the base reference throughout the system. Since subharmonics of this frequency are used in multiple places, the potential exists for these to be locked to different cycles of the 35 MHz reference. It is planned to replace the 35 MHz with its lowest subharmonic in the future to eliminate this difficulty.

7 REFERENCES

- [1] M. Laverty, K. Fong, S. Fang, "Design and Testing of the ISAC RFQ Control System", Proceedings of the 1999 Particle Accelerator Conference, New York, March 1999, pp. 890-2.
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- [3] K. Fong, S. Fang, M. Laverty, J. Lu, R.L. Poirier, "Commissioning of the TRIUMF ISAC RF System", this proceeding.