ISBN: 978-3-95450-223-3 ISSN: 2673-7000 doi:10.18429/JACoW-NAPAC2019-WEPLM03

THE LLRF CONTROL DESIGN AND VALIDATION AT FRIB*

S. Zhao†, W. Chang, S.H. Kim, H. Maniar, D.G. Morris, P.N. Ostroumov, J.T. Popielarski, H.T. Ren, N.R. Usher[1], Facility for Rare Isotope Beams, Michigan State University, East Lansing, MI, USA
[1] also at Ionetix Corporation, Lansing, MI, USA

Abstract

One of the challenges in designing the low level radio frequency (LLRF) controllers for the Facility for Rare Isotope Beams (FRIB) is the various types of cavities, which include 5 different frequencies ranging from 40.25 MHz to 322 MHz, and 4 different types of tuners. In this paper, the design strategy taken to achieve flexibility and low cost and the choices made to accommodate the varieties will be discussed. The approach also allowed easy adaptation to major design changes such as replacing two cryo-modules with two newly designed room temperature bunchers and the addition of high-voltage bias to suppress multi-pacting in half-wave resonators (HWRs). With the successful completion of the third accelerator readiness review (ARR03) commissioning in early 2019, most of the design has been validated in the real accelerator system, leaving only HWRs which are constantly undergoing tests in cryo-module bunker. The integrated spark detector design for HWRs will also be tested in the near future.

INTRODUCTION

The Facility for Rare Isotope Beams (FRIB) is a scientific user facility for nuclear physics research being built at Michigan State University (MSU). The folded linear accelerator (LINAC) at FRIB consists of a front end (FE), three linear segments (LS1/2/3) and two folding segments (FS1/2). Four types of superconducting radio-frequency (SRF) cavities spread out in the linear and folding segments, namely β=0.041 and β=0.085 quarter-wave resonators (QWR041/085) and β=0.29 and β=0.53 half-wave resonators (HWR29/53). Most of the room temperature (RT) cavities including the multi-harmonic buncher (MHB), radio-frequency quadruple (RFQ) and medium energy beam transport (MEBT) buncher are in the FE, with the exception of multi-gap buncher (MGB) in FS1 [1]. Table 1 summarizes different types of cavities in the FRIB LINAC.

As shown in the table, the various types of cavities run at five different frequencies from 40.25 MHz to 322 MHz and have four different tuner types. Designing a low level radio frequency (LLRF) controller to support all those cavity types is a challenging task.

LLRF DESIGN

As stated earlier, the FRIB LLRF design has to be flexible to support various cavity types. The flexibility also means that the design should be able to accommodate possible design changes in a later stage. For any engineering design, cost is also a major factor to be considered. Time wise, it is critical to integrate the LLRF controller with other systems as early as possible to identify potential issues and fix them in the next iteration.

Table 1: FRIB Cavity Types

System	Area	Frequency (MHz)	Type	Tuner
MHB F1	FE	40.25	RT	N/A
MHB F2	FE	80.5	RT	N/A
MHB F3	FE	120.75	RT	N/A
RFQ	FE	80.5	RT	temperature
MEBT	FE	80.5	RT	2-phase stepper
QWR	LS1 FS1	80.5	SC	2-phase stepper
MGB	FS1	161	RT	5-phase stepper
HWR	LS2/3 FS2	322	SC	pneumatic

Hardware

FRIB General Purpose Digital Board A common digital board based on the Xilinx Spartan-6 field programmable gate array (FPGA) was designed at FRIB to serve different applications including LLRF, beam position monitor (BPM) and machine protection system (MPS). The cost of the FRIB General Purpose Digital Board (FGPDB) is reduced due to the combined high volume. For the LLRF application, some unused and expensive parts are not populated to further reduce the cost. The FGPDB is compatible with the μTCA standard and can be used either in a μTCA crate (BPM case) or in a chassis (LLRF and MPS cases). The FGPDB has 512 MB onboard double data rate memory which can be used for waveform storage.

RF Board Trying to reduce the temperature dependency of some RF devices, e.g. mixers and local oscillator, the FRIB LLRF control adopts direct-sampling / under-sampling approach, which means that the analog-to-digital converter (ADC) samples the RF signal directly without mixing it to an intermediate frequency at a frequency lower than the Nyquist frequency of the signal. This makes sharing the same RF input chain across all five frequencies possible, and allows the ADC to use the same sampling frequency which greatly simplifies the board design. Non-In-Phase/Quadrature (non-IQ) sampling is also adopted to reduce the effect of harmonics.

No mixer is used in the RF output chain as well. The digital-to-analog converter (DAC) generates four points (I, Q, −I, −Q) per waveform. The band-pass filters pick up the fundamental or higher harmonics of interest. By carefully choosing the parts to be footprint compatible, three variations of the RF board were designed to have the same

* Work supported by the U.S. Department of Energy Office of Science under Cooperative Agreement DE-SC0000661
† Email address: zhaos@frib.msu.edu

Content from this work may be used under the terms of the CC BY 3.0 licence (© 2019). Any distribution of this work must maintain attribution to the author(s), title of the work, publisher, and DOI

ISBN: 978-3-95450-223-3 ISSN: 2673-7000 doi:10.18429/JACoW-NAPAC2019-WEPLM03

Content from this work may be used under the terms of the CC BY 3.0 licence (© 2019). Any distribution of this work must maintain attribution to the author(s), title of the work, publisher, and DOI

board layout. With only one DAC, each variant supports two frequencies, i.e. 80.5/322 MHz, 40.25/120.75 MHz and 161/241.5 MHz, by using two RF switches (see Fig. 1). The RF switches are tied to external interlock input to shut off RF immediately.

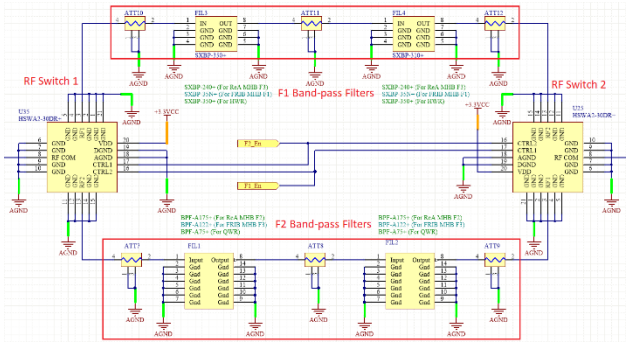

Figure 1: RF output chain to support two frequencies.

Additionally, four analog input, four analog output, five digital input and five digital output channels are included on the RF board to accommodate unexpected changes.

Tuner Board Two types of tuner boards of the same form factor are designed. The stepper tuner board can drive the 2-phase stepper motor with micro-stepping capability for QWRs and MEBT bunchers. An RS-422/485 interface is reserved on this board and later is used to communicate with an external 5-phase stepper driver module for the MGB. The analog tuner board generates voltage signals to either control the pneumatic valves for the HWRs or send the tuner error information to the RFQ water skid controllers.

Figure 2 shows a complete FRIB LLRF controller.

Figure 2: FRIB LLRF controller. 1. Power supply; 2. Tuner board; 3. RF board; 4. FGPDB; 5. Front panel and board.

Firmware/Software

An embedded system design approach based on the Microblaze 32-bit soft core processor is adopted at FRIB to allow proper firmware / software partitioning. The software running in the Microblaze handles less time critical functions, such as device initialization, tuner control, fan speed control, serial console, build-in test functions, waveform read-out, firmware updates, etc. Software functions can be changed much easier and faster without recompiling/testing the firmware which takes hours rather than minutes.

Functions that need fast processing and high reliability, e.g. the RF digitization and synthesis, interlocks, RF feedback control, pulsing and waveform storage, are implemented in the firmware as a customized intellectual property (IP) core. For standard bus functions such as Serial Peripheral Interface (SPI) and Inter-Integrated Circuit (I^2C), the Xilinx provided IP cores are used.

FRIB LLRF controller implements digital self-excited loop (SEL) mode, which allows cavities to be driven at an offset frequency to the reference frequency. This makes cavity turn on very easy and is an essential part of the auto-start process (e.g. during RFQ warm-up period).

For RF feedback control, FRIB uses the same active disturbance rejection control algorithm as the 3 MeV/u re-accelerator (ReA3) [2], but it is implemented directly in the firmware [3] rather than software and is running at a much higher rate (1 MHz vs. 50 kHz).

Comprehensive external and internal interlocks to protect the cavities, amplifiers, and other equipment are implemented in FRIB LLRF controller. The controller takes external inputs from programmable logic controller, amplifier and fast protection system to shut off RF drive if vacuum, temperature, etc. are abnormal, or the amplifier has a fault. Besides external interlocks, the LLRF controller also generates internal fault conditions including the following: cavity field low (for low multi-pacting), cavity field high (for quenching or field emission), reverse power high (for amplifier protection or sparking), forward power high (for amplifier and cavity protection), and cold cathode gauge monitor (for fundamental power coupler protection).

FRIB LLRF also supports pulse operation. An internal pulsing function is available with user settable frequency, duty, ramp time, and pulse low/high set-points. The pulser can also be synchronized to external sources, e.g. digital input and global timing system.

LLRF VALIDATION

The LLRF controller prototype design was done quite ahead of the cavity and cryomodule production to take every opportunity to validate and refine the design.

In early 2015, a batch of 9 LLRF controllers (version 1) were built and started to serve firmware development, SRF cavity certification testing, fundamental power coupler (FPC) conditioning and cryomodule bunker tests.

Based on the issues and problems found during various tests, the production LLRF controller design (version 2) was finished in late 2016. The mass production started in early 2017 and 378 LLRF controllers (including spares) were built by the end of 2017.

For any firmware changes, the LLRF undergoes bench test to verify critical functions such as interlocks, network communication etc., followed by tests with a real cavity in the cryomodule test bunker before they are rolled out to production. In the following we highlight a few tests that helped us to validate the LLRF design.

ISBN: 978-3-95450-223-3 ISSN: 2673-7000 doi:10.18429/JACoW-NAPAC2019-WEPLM03

Integrated Test

During the integrated test for the HWR53 in Feb. 2016, the cavity frequency control with the pneumatic tuner was not good due to the lack of experience with the nonlinear behavior of the valve characteristic. After consulting with experts at the Argonne National Laboratory (ANL) [4], a procedure has been developed to calibrate the valve open/close voltages for the pneumatic tuner.

Bunker Test

In 2015, the QWR prototype cryomodule was built and tested in the ReA6 bunker [5]. The stepper driver chip overheating problem was discovered during the 24-hour cavity locking test, after which a newer version of the stepper tuner board with improved thermal management was designed.

During the second HWR cryomodule testing in April 2016, the phase control performance was found to be much worse than previous tests. A study was carried out and the finding is that the reference clock frequency is too low (10.0625 MHz vs. 80.5 MHz used previously). Immediately, the FRIB reference clock design was changed to use 80.5 MHz reference.

After testing the first few HWR cryomodules, it was determined that high voltage bias is necessary to suppress multipacting in the FPC. The spare analog input/output channels are used to monitor the bias voltage and enable the high voltage power supply. Additional interlocks were added to inhibit RF when bias voltage is not present.

Accelerator Readiness Review (ARR)

FRIB implemented a phased-ARR process to support commissioning [6]. So far three ARRs have been completed and the forth one is scheduled in early 2020.

ARR01 Front end commissioning started in June 2017 and the mainly focus was on the RFQ [7]. Fast interlock response is required to reduce the risk of damage to the cavity due to spark at high power level. To prevent undesired latching anode power supply fault, the LLRF firmware was updated to inhibit the synchronization pulses in the anode power supply for >800 ns when the RF drive is turned off.

ARR02/03 The QWRs were commissioned during this period. Due to the large number of cavities (104 in total), improving the operation efficiency is high priority. An auto-start procedure was developed to automate cavity turn-on sequence (see Fig. 3).

REA3 LLRF UPGRADE

The LLRF controller for the ReA3 at the National Superconducting Cyclotron Laboratory, now part of FRIB, was designed in 2007 and adopts the Nuclear Instrumentation Module (NIM) crate design with a much older FPGA chip (Xilinx Spartan 3E) which was too crowded to support any new firmware changes. In September 2017, five of the fifteen LLRF controllers for the ReA3 SRF cavities were replaced by the FRIB type LLRF controllers to demonstrate compatibility and new features. After almost a year of validation, by September 2018, all LLRF controllers for ReA3 were upgraded, including the three for the ReA3 MHB F1/F2 and RFQ. By sharing the same hardware/firmware/software as FRIB, the upgrade has made the maintenance effort much less.

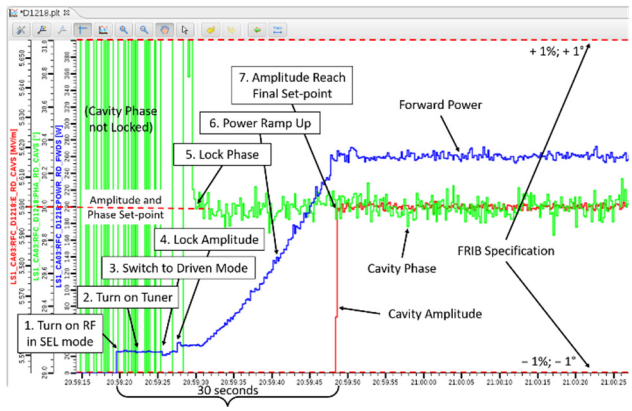

Figure 3: Example of automated turn-on of QWR during ARR3 commissioning.

SUMMARY

Flexibility and low cost are the core to the FRIB LLRF design strategy, based on which the detailed design was carried out. It was demonstrated through various level of testing that the design meets all the requirements. In the case when system level design changes are necessary, the FRIB LLRF design is very agile and can quickly fulfill the new requirement. The upcoming ARR04 is a very critical step in terms of the LLRF validation. After the HWR cryomodule commissioning, the LLRF design will be fully validated for all system types.

REFERENCES

[1] D. G. Morris *et al.*, "RF System for FRIB Accelerator", in *Proc. IPAC'18*, Vancouver, Canada, Apr.-May 2018, pp. 1765-1770. doi:10.18429/JACoW-IPAC2018-WEXGBF3

[2] J. Vincent *et al.*, "On active disturbance rejection based control design for superconducting RF cavities," *Nucl. Instrum. Methods Phys. Res., Sect. A*, vol. 643, no. 1, pp. 11-16, 2011.

[3] S. Zhao *et al.*, "Fixed-point Implementation of Active Disturbance Rejection Control for Superconducting Radio Frequency Cavities," in proc. *2010 American Control Conference*, Washington D.C., June-July 2010, pp. 2693-2698.

[4] G. Zinkann, E. Clifft, and S. I. Sharamentov, "An Improved Pneumatic Frequency Control for Superconducting Cavities", in *Proc. PAC'05*, Knoxville, TN, USA, May 2005, paper WPAT082, pp. 4090-4092.

[5] H. Ao *et al.*, "FRIB Driver Linac Integration to be Ready for Phased Beam Commissioning," presented at NAPAC'19, Lansing, MI, Sept. 2019, paper WEPLH09, this conference.

[6] J. Wei *et al.*, "The FRIB SC-LINAC: Installation and Phased Commissioning," presented at SRF'19, Dresden, Germany, Jul. 2019, paper MOFAA3.

[7] H. T. Ren *et al.*, "Commissioning of the FRIB RFQ", in *Proc. IPAC'18*, Vancouver, Canada, Apr.-May 2018, pp. 1090-1093. doi:10.18429/JACoW-IPAC2018-TUPAL039

Content from this work may be used under the terms of the CC BY 3.0 licence (© 2019). Any distribution of this work must maintain attribution to the author(s), title of the work, publisher, and DOI