FPGA Control of Coherent Pulse Stacking

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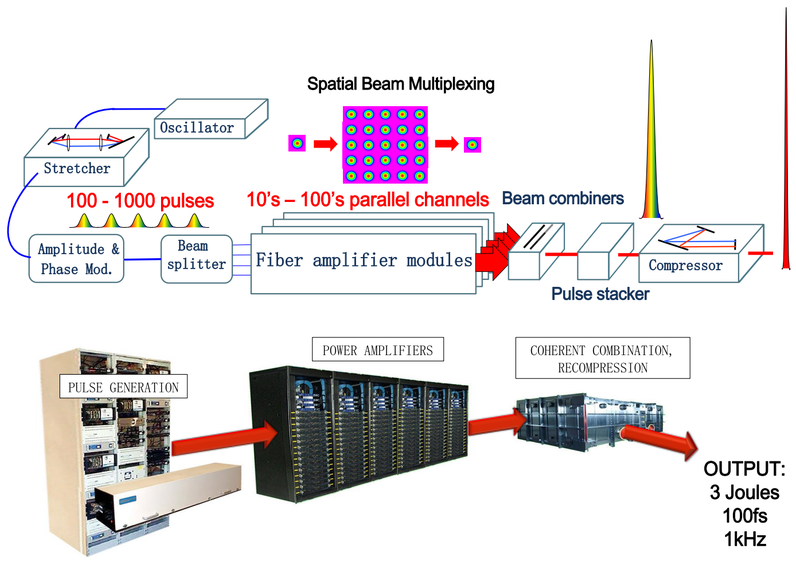
Abstract

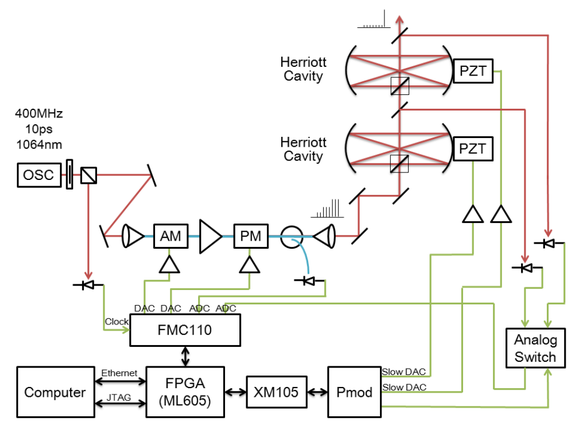
Coherent pulse stacking (CPS) is a new time-domain coherent addition technique that stacks several optical pulses into a single output pulse, enabling high pulse energy from fiber lasers. Due to advantages of precise timing and fast processing, we use an FPGA to process digital signals and do feedback control so as to realize stacking-cavity stabilization. We develop a hardware and firmware design platform to support the coherent pulse stacking application. A firmware bias control module stabilizes the amplitude modulator at the minimum of its transfer function. A cavity control module ensures that each optical cavity is kept at a certain individually-prescribed and stable round-trip phase with 2.5 deg rms phase error.

Introduction



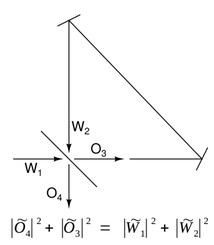
- High laser pulse energy is achieved at low repetition rate currently.
- CPS combines high average power and high repetition rate.
- Joule-kHz CPS system will revolutionize LPAs and FELs.

Principle of Coherent Pulse Stacking



$$\begin{bmatrix}\widetilde{O}_4\\ \widetilde{O}_3\end{bmatrix}=\begin{bmatrix}r & it\\ it & r\end{bmatrix}\begin{bmatrix}\widetilde{W}_1\\ \widetilde{W}_2\end{bmatrix}\Rightarrow\begin{cases}\widetilde{O}_4 = r\,\widetilde{W}_1 + it\,\widetilde{W}_2\\ \widetilde{O}_3 = it\,\widetilde{W}_1 + r\,\widetilde{W}_2\end{cases}\Rightarrow \frac{\widetilde{O}_4}{\widetilde{W}_1}=\frac{r-\widetilde{\alpha}\,z^{-1}}{1-r\,\widetilde{\alpha}\,z^{-1}}$$

$$\widetilde{W}_2 = z^{-1}\cdot\widetilde{\alpha}\cdot\widetilde{O}_3 = z^{-1}\cdot 1e^{j\varphi}\cdot\widetilde{O}_3$$



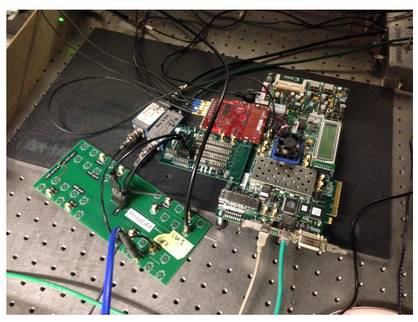
z-transform

$$H(z)=\frac{Y(z)}{X(z)}=\frac{r-\widetilde{\alpha}\,z^{-1}}{1-r\,\widetilde{\alpha}\,z^{-1}}$$

$$|\widetilde{O}_4|^2+|\widetilde{O}_3|^2=|\widetilde{W}_1|^2+|\widetilde{W}_2|^2$$

- Optical beam is coupled into a polarization-maintaining single-mode fiber.
- AM tailors the pulse burst, followed by PM imprinting the required phase.
- The first pulses of burst enter the cavity and interfere destructively, storing energy inside cavity.
- The final pulse interferes constructively with intra-cavity pulses, extracting energy into one pulse.
- Z-Transform is employed in algorithm for the implementation of FPGA.

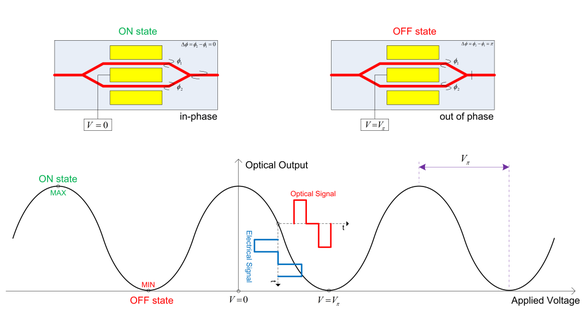
Hardware and Firmware Infrastructure

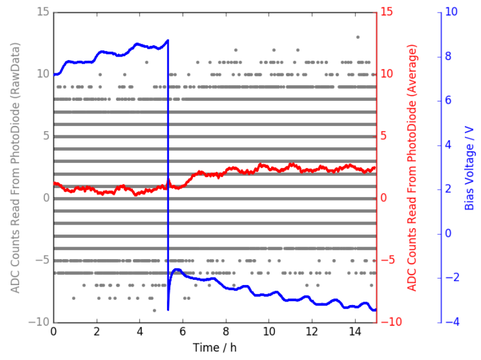


Hardware:
- ML605 + FMC110 + XM105
- 2-CH 12-bit A/D & 2-CH 16-bit D/A & 400Msps
- kHz Feedback Control Repetition Rate

Firmware:
- Bottom Layer: Hardware-Dependent Drivers
- Intermediate Layer: Data Communication Layer (UDP)
- Top Layer: Project Specific DSP
  - bias_ctrl.v
  - cavity_ctrl.v

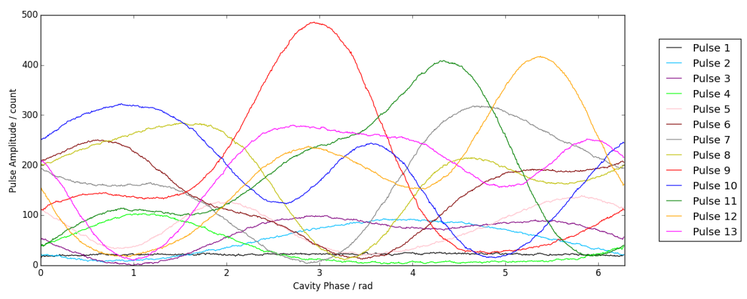
Bias Control

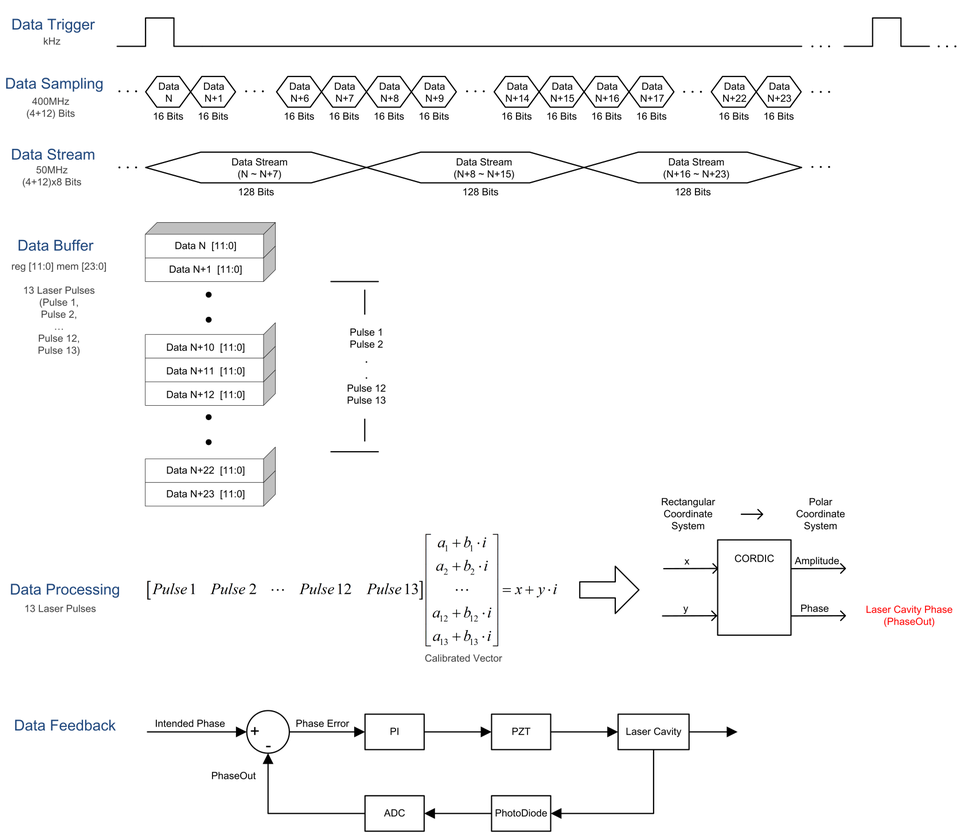




- Algorithm: Output two ± voltages. If transmission unequal, move bias to equalize.
- Bias control module stabilizes the amplitude modulator at the minimum of its transfer function.
- Zero bias point drifts due to temperature.
- Extinction ratio of the modulator is 28 dB which suits the bias control requirement.
- Bias control module operates at kHz rate on FPGA.

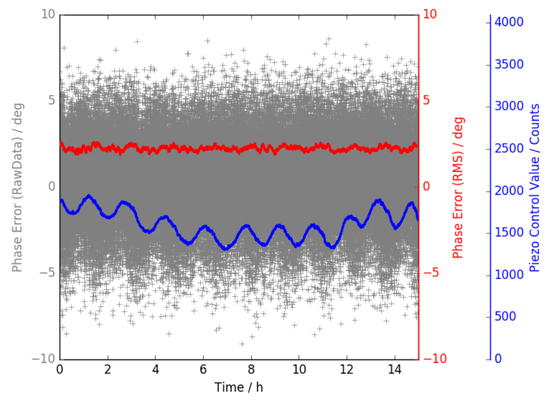
Cavity Control

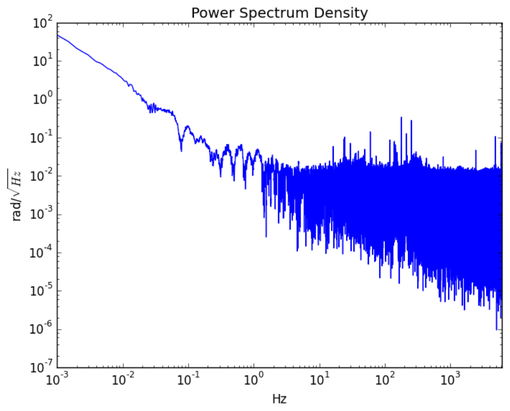


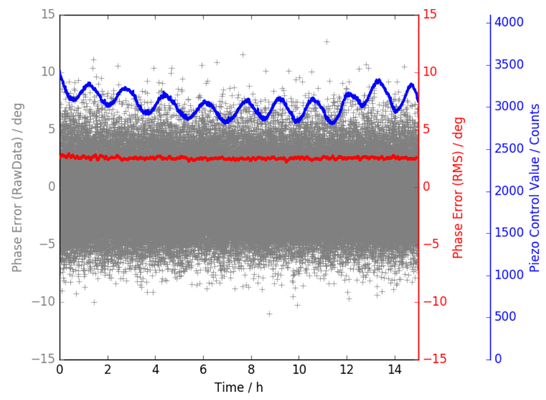


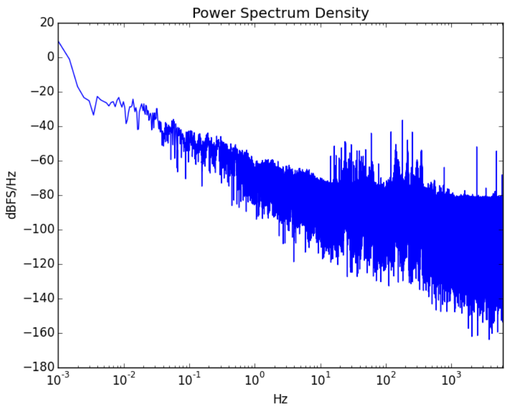
- Lock the cavity phase at the desired angle to realize coherent pulse stacking.
- Cavity control module programs the slow DAC and drives the PZT to stabilize the optical cavity.
- Three clock domain: sampling clock domain (400MHz), processing clock domain (50MHz), feedback clock domain (kHz).

Experiment Results









- Stabilize cavities at target phase with 2.3° (1st cavity) and 2.5° (2nd cavity) rms phase error.
- This level of phase stability ensures an intensity enhancement factor of 7.4 with 13-pulse input.
- The actuated mirror resonance is the bandwidth limit.
- Resonant frequencies (170∼400Hz for different mirrors) are OK for now.