FERMILAB CRYOMODULE TEST STAND RF INTERLOCK SYSTEM

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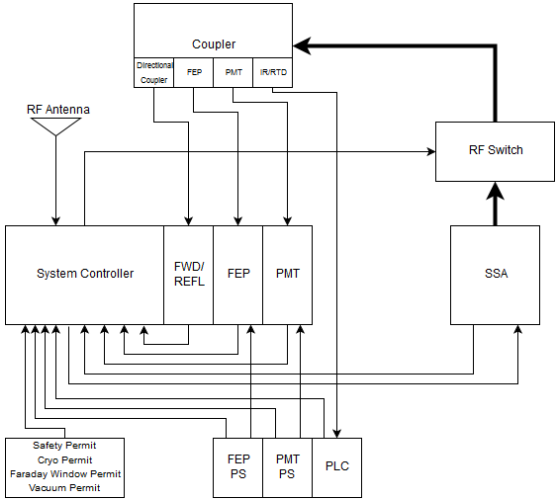
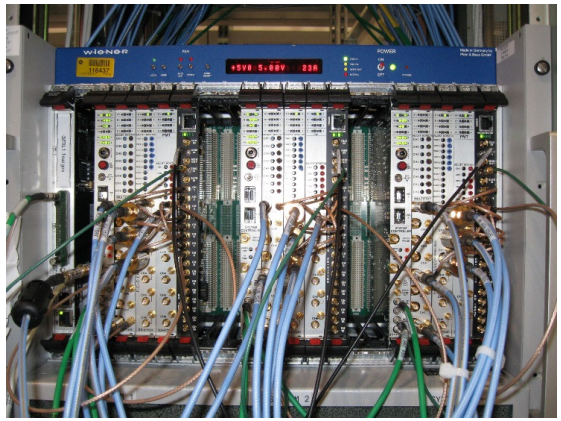
An interlock system has been designed for the Fermilab Cryo-module Test Stand (CMTS), a test bed for the cryo-modules to be used in the upcoming Linac Coherent Light Source 2 (LCLS-II) project at SLAC. The interlock system features 8 independent subsystems, one per superconducting RF cavity and solid state amplifier (SSA) pair. Each system monitors several devices to detect fault conditions such as arcing in the waveguides or quenching of the SRF system. Additionally each system can detect fault conditions by monitoring the RF power seen at the cavity coupler through a directional coupler. In the event of a fault condition, each system is capable of removing RF signal to the amplifier (via a fast RF switch) as well as turning off the SSA. Additionally, each input signal is available for remote viewing and recording via a Fermilab designed digitizer board and MVME 5500 processor.



The above block diagram details the permits that are summed by each System Controller card



3 full systems of interlocks in a VME crate

The above image shows three full RF interlock systems installed in a VME crate. The boards (in order) are:

MVME 5500 – retrieves status signals and data from all system boards

System Controller – sums permit signals, monitors RF antenna

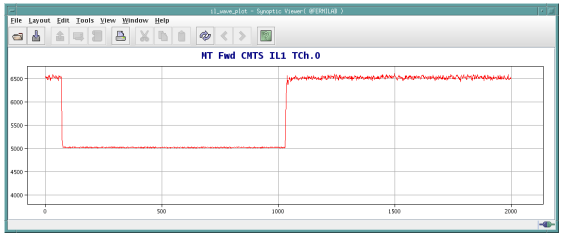
FWD/REFL – monitors RF power from directional coupler

FEP – monitors a field emission probe for voltage drop indicating stray ions

PMT – monitors a photomultiplier tube, looks for light from arcing

Digitizer – allows remote viewing of interlock board signals, digitizes signals at up to 80 MHz

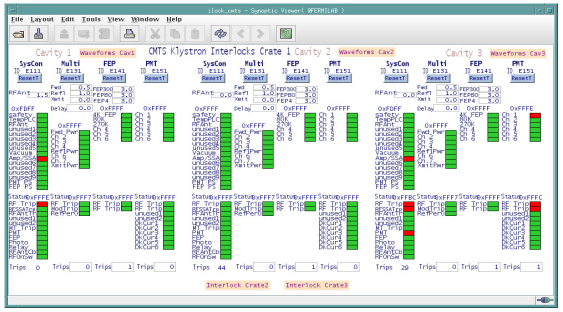
Relay-Latch – latches auxiliary inputs to be fanned out to each system (not shown in above photo)



Digitizer output in pulsed mode. Lower value equates to higher input power, showing that the entire pulse is visible.

Usage and Remote Viewing

The interlock boards were designed in order to be run remotely. Each board has an analog trim-pot set trip limit as well as a DAC set trip limit. All boards report their status via the MVME 5500, and trips can be reset remotely. Below is the display used for a single VME crate (three full systems).



RF Interlock remote display of trip limits and status, with the three systems in various permit states

The digitizer boards were designed to have two running modes: pulsed and CW.

During the pulsed mode the digitizer receives external triggers to synchronize data acquisition, with a variable sampling rate to accommodate long pulses. The number of samples is also variable. This is seen below to the left.

During CW mode the digitizer runs continuously, reporting data at 720 Hz. A circular buffer is used to keep a set amount of data (sampling rate and number of points also variable) that are only reported when a trip occurs. Below is an example of this mode, where FEP activity that caused a trip is captured and plotted.

FEP activity causing a trip condition