BEAM INTENSITY MONITORING SYSTEM FOR THE PIP-II INJECTOR TEST ACCELERATOR*

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Abstract

The PIP-II injector test accelerator is an integrated systems test for the front-end of a proposed CW-compatible, pulsed H^- superconducting RF linac. This linac is part of Fermilab's Proton Improvement Plan II (PIP-II) upgrade. This injector test accelerator will help minimize the technical risk elements for PIP-II and validate the concept of the front-end. Major goals of the injector accelerator are to test a CW RFQ and H^- source, a bunch-by-bunch MEBT beam chopper and stable beam acceleration through low-energy superconducting cavities. Operation and characterization of this injector places stringent demands on the types and performance of the accelerator beam diagnostics. This paper discusses the beam intensity monitor systems as well as early commissioning measurements of beam transport through the Medium-Energy Beam Transport (MEBT) beamline.

INTRODUCTION

The beam intensity, or number of charged particles in the beam, has to be monitored and must be kept within predetermined safety and operational envelopes. To ensure that, beam intensity monitors with magnetically-coupled toroidal pickups are used as a non-interceptive method to measure the total transferred intensity in the PIP-II H^- linac. The beam intensity monitor system consists of the toroid assembly, the signal conditioning circuit as well as the data acquisition electronics (see Fig. 1). The toroid pickup is inserted around the beam tube with a ceramic insulator.

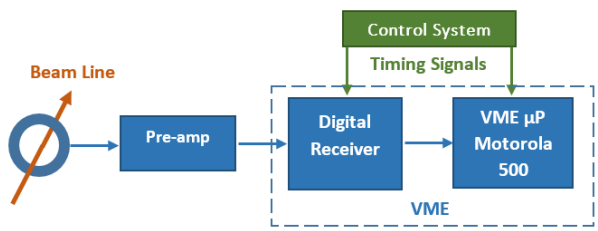

Figure 1: Toroid-based beam intensity monitor system.

A low-pass filter / gain stage follows. An in-house designed digitizer module is used for data acquisition and digital signal processing. The digitizer is a 6U VME module and has 8 analog input channels with selectable AC or DC coupling. On-board ADC chips are capable of a sampling rate up to 125MS/s. A programmable clock distribution circuit offers flexible timing configurations. Other elements on the board are the Cyclone III FPGA chip for signal processing, and 192 MB of DDR2 memory for data buffering (see Fig. 2). A Motorola 5500 VME microprocessor is used for data buffering and communication with Fermilab's Accelerator Controls System (ACNet).

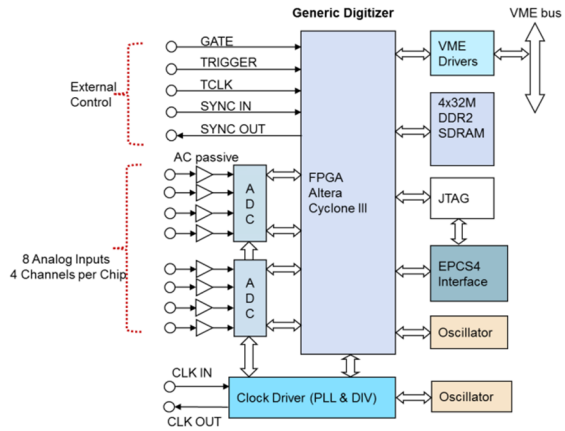

Figure 2: 8-channel 125 MS/s VME digitizer.

TOROID SYSTEM

At PIP-II beam intensity is detected using several magnetically-coupled toroidal pickups along the transport line, to provide a non-destructive method to measure the total transferred intensity.

- The first part of the monitor is the beam pickup, i.e. the toroid, including its mechanical assembly, ceramic gap, shielding, etc., as part of the beam line within the tunnel enclosure. A ceramic insulator provides an electric break in the metallic vacuum chamber. The toroid couples to the magnetic field components of the beam, i.e. detects the beam intensity. The support and shielding structure provides a well-defined path of low impedance for the wall currents.
- Following the pickup are the preamp and digital electronics which are discussed in following sections.

The toroidal pickup follows the basic transformer theory. Passing through the center of the toroid, the beam forms a single-turn primary coil of the transformer. An N-turn secondary coil is wound around the core, and the induced voltage is measured across a load resistor which terminates the secondary winding.

The toroidal pickups installed at PIP-II have a limited bandwidth substantially lower than the RF beam spectrum. As a result, most of the bunch time structure, i.e. bunch-by-bunch information, is lost. Thus the waveform of the toroid signal reflects the "envelope" of the beam pulse (Fig. 3). Using both *Ohm*'s law and transformer relationships, the amplitude of macro-pulse is linear with

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the respect to the beam current within the bandwidth of the toroid. Furthermore, this relationship can be written in terms of the pickup's sensitivity or transfer impedance:

$$Z_{\text{toroid}}(\omega) = \frac{V_{\text{out}}(\omega)}{I_{\text{beam}}(\omega)} \quad (1)$$

A preamplifier is added to provide additional gain to increase the toroid signal. The amplitude of the toroid signal at the digitizer input is a linear function of the pickup's sensitivity and the preamplifier gain.

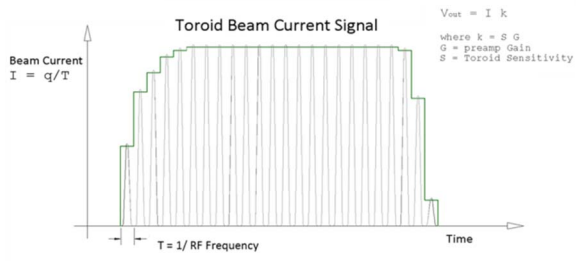

Figure 3: Processing the envelope of the toroid's beam current signal.

After acquiring the toroid signal, the electronics' primary function is to integrate the macro-pulse envelope signal to provide total beam intensity, and / or average beam current. The total beam intensity, or number of particles per beam pulse N can be calculated from Q_{total}, divided by the charge per particle e=1.602e-19 as:

$$\text{Total Beam Intensity, } N = \frac{Q_{\text{rotal}}}{e} \approx \frac{T}{k\,e}\sum_{n=0}^{M} v_n \quad (2)$$

The average current of the transferred beam pulse can be computed as:

$$\text{Beam Current, } I_{\text{AVG}} = \frac{Q_{\text{rotal}}}{\text{PW}} \approx \frac{T}{k\,\text{PW}}\sum_{n=0}^{M} v_n \quad (3)$$

where PW is the width of the measured beam macro-pulse.

Although the toroid's output is AC-coupled, therefore has no DC response, additional digital filtering and / or algorithms, e.g. baseline correction, may be needed to improve signal-to-noise ratio, linearity and accuracy of the reported, calibrated beam intensity.

THE DIGITIZER

Used for both data acquisition and digital signal processing, the 125MS/s digitizer is implemented on an in-house designed 6U VME board. Figure 2 shows the simplified diagram of the digitizer board.

There are eight analog input channels; each can be configured for either AC or DC coupling. The full scale input range, in either configuration, is +/- 1.15V. The DC coupled input, which is used for this application, has two stage pre-amps from Analog Devices, with an effective bandwidth of roughly 500 MHz at unity gain. These provide differential inputs centered at DC level.

The digitizer is equipped with a clock distribution circuit which can reference to the on-board oscillator or external clock source. A clock driver chip, programmable through the FPGA, provides a flexible clock source for different applications. Input signals are sampled by two ADS6445 analog-to-digital converters (ADC) which can sample at a rate of up to 125 MS/s.

An Altera Cyclone III FPGA chip is used for hardware configuration and on-board data processing. The FPGA algorithms provide smart timing schemes with external trigger, gate and sync inputs.

There are also 192 MB of DDR2 SDRAM for data buffering.

SINGAL PROCESSING ON FPGA

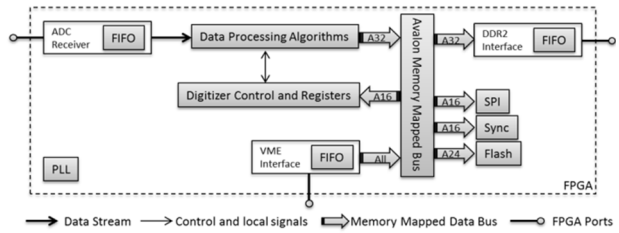

Figure 4: Simplified data flow.

The FPGA's code can be divided into two sections. One supports the basic infrastructure required for any general application: an ADC interface, a VME bus driver, a memory interface, a serial port interface and a timing signal decoder. The other supports application specific algorithms including the intensity calculation.

The connection between these design blocks was developed using the Qsys tool provided by *Altera*, the FPGA manufacturer. The above block diagram gives a simplified view of data flow between the various design blocks. The actual interfaces between the blocks follow guidelines of the Avalon Memory Mapped data bus and the Avalon Streaming data interface (Fig. 4).

Timing Schema

There are three clock domains in the firmware design. The ADC data processing is clocked at the same rate as the sampling frequency. General control blocks and the data bus operate at a separate clock rate from an on-board oscillator. The DDR2 memory interface is clocked at higher rate than the sampling frequency for improved data buffering performance.

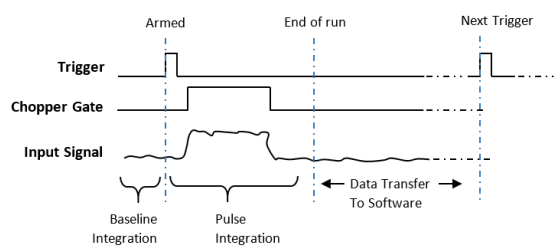

Figure 5: Timing Diagram for data processing.

To synchronize these clock domains, an external trigger is used. Data processing algorithms are synchronized by an external trigger in sync with beam events. When the processing is finished, the digitizer returns to its default state and waits for the next sync pulse (Fig. 5).

Waveform data from all eight channels are processed in parallel. For each channel the sampled raw data are converted from serial to parallel and then packaged into 16-bit samples.

Beam Intensity Measurements

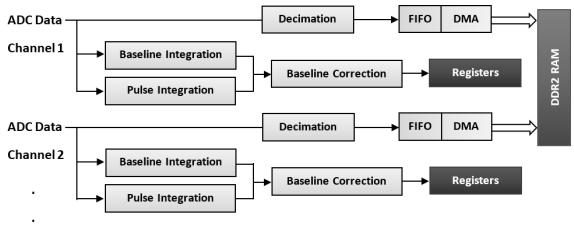

Figure 6: Simplified data path for the digitizer.

The beam intensity monitor provides total beam intensity and calculated average current to ACNET. Beam intensity is calculated by integration of the ADC samples. The raw data samples are integrated within programmable windows in time. The average beam current is then evaluated as a result of the beam intensity calculations and the calculated pulse width based on edge detection or an external gate signal.

Furthermore, the acquired toroid data is corrected for the baseline-shift of the input data and saved to memory for waveform readout by the control system applications. Data decimation can be applied as an option (Fig. 6).

Trapezoidal Integrator To balance accuracy and complexity, the integrator uses the trapezoidal integration algorithm (Fig. 7):

$$Int \approx \sum_{k=1}^{8192}\left(\frac{s_k + s_{k+1}}{2}\right) = \sum_{k=1}^{8192} s_k + \frac{s_{8193}}{2} - \frac{s_1}{2} \qquad (4)$$

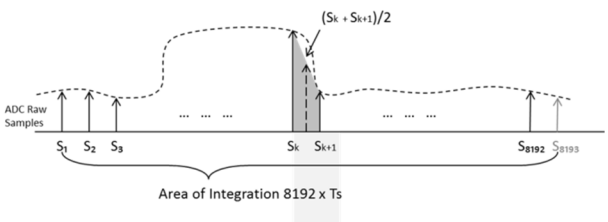

Figure 7: Trapezoidal integration.

Baseline Correction A trigger event marks the beginning of the beam pulse. Integration of the baseline is performed on data buffered in an on-chip memory. Following the baseline measurement the integration of the actual beam pulse starts. The size of the baseline integration window is limited by the size of the memory, whereas the pulse window is dynamic, determined by the intended pulse width. The integration results are then adjusted according the difference in window sizes. The difference of the two integrations produces the baseline corrected beam pulse intensity.

Edge Detection An optional edge detecting procedure helps to detect the width of the pulse. Pulse width combined with intensity calculation gives us averaged pulse current. A buffer keeps track of the variation of the baseline. When ADC samples exceed the recorded baseline level by a predetermined threshold, rising edge of the pulse is detected. The trailing edge of the pulse is detected when the signal drops below a predetermined threshold. Having the two edges determined, the width of the beam pulse is calculated (Fig. 8). As an alternative to edge detection, a TTL gate from the beam chopper is used to provide the pulse width.

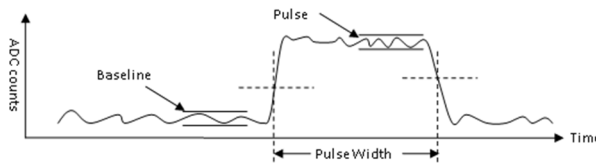

Figure 8: Edge detection of the beam pulse.

RESULTS AND CONCLUSIONS

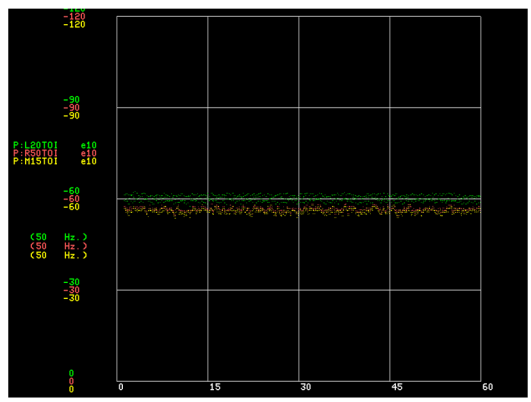

Figure 9: Intensity reading of three toroids.

A toroid-based beam intensity measurement system for the linac at PIP-II uses an in-house developed digital signal processing schema. Preliminary measurement results are in-line with other instrumentation devices in the beam line, with absolute accuracy of 2-3% (see Fig. 9). Our goal is to achieve 1% absolute accuracy. Additional signal conditioning and calibration process may be needed.

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