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HIGH EFFICIENCY, HIGH POWER, RESONANT CAVITY AMPLIFIER FOR PIP-II

Rebecca Simpson, David Cope, Marcel. P.J. Gaudreau, Erik Johnson, Michael Kempkes, Nigel Stuart, Diversified Technologies, Inc., Bedford, MA, USA

Abstract

An advanced high-power, high power density, solid state power amplifier (SSPA) was developed to replace legacy Vacuum Electron Devices (VEDs). Diversified Technologies, Inc. (DTI) developed and integrated a resonant-cavity combiner with solid state amplifiers for the Proton Improvement Plan-II (PIP-II) at Fermilab. The architecture combines the power of N-many (up to 100+) RF power transistors into a single resonant cavity that are surface-mounted and -cooled. The system is designed so that failure of individual transistors has negligible performance impact. Due to the electrical and mechanical simplicity, maintenance and logistics are simplified leading to reduced capital and operating costs.

DTI demonstrated the basic feasibility of a 50-100 kW class amplifier resonant cavity combiner system at 650 MHz. A single-cavity system reached 15 kW at 66% power-added efficiency with ten of 12 slots filled, on only one of two cavity faces. The system further demonstrated the expected graceful degradation - an intermittent fault occurred on one of the ten modules and the only observable effect was a reduction in output power to 13.3 kW with a slight reduction in efficiency. Combining of multiple cavities was also demonstrated at low power.

INTRODUCTION

Achieving high power from solid state amplifiers is only possible by combining the outputs of multiple transistors. Each UHF transistor is limited to relatively modest power levels (less than 1000 watts CW), so hundreds to thousands of devices must be combined to compete with large conventional Vacuum Electron Devices, such as klystrons. In contrast to phased array radars, where space combining enables the contribution of thousands of individual, low power amplifiers to create a high power beam, the RF power for accelerators must be available at a single coupler to drive the accelerator cavity. Efficiently combining multiple transistors, while delivering high reliability at an affordable cost, are the main challenges for high power solid-state amplifiers (SSAs).

Binary combining (2N) is common at lower power, but high total insertion losses rule it out for most accelerator applications. DTI's cavity combiner is a unique form of the so-called N:1 combiner. The amplifier module combines the power of more than 96 transistors in one step. While there are other types of N:1 combiners, they typically require high power RF connectors and water cooling lines for each individual amplifier stage, leading to a level of complexity which scales with output power and total number of transistors. DTI's approach avoids most of this complexity, while the demonstrated graceful degradation feature ensures high reliability.

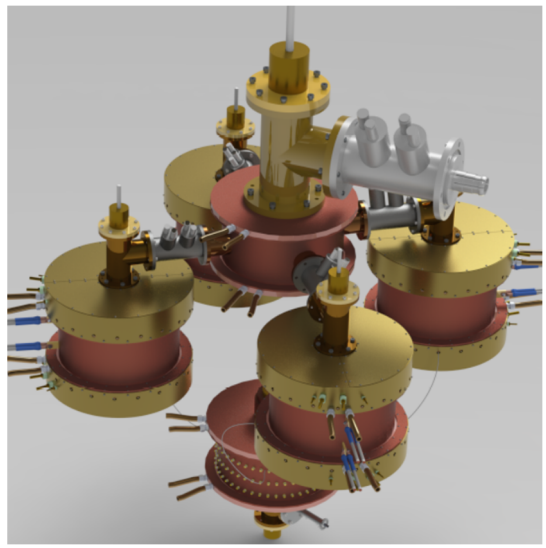

Figure 1: Conceptual layout of a high power solid-state transmitter based on four DTI cavity amplifier modules combined in a passive 4:1 cavity combiner. Power level of this concept scales to at least 500 kW

In this approach, the cavity serves as both a power combiner and also as an integral part of the transistor output matching network. The low output impedance transistors are not matched to an arbitrary 50 ohm impedance level; rather the coupling loop and associated transmission line (when operated in the cavity) operates at a lower impedance level, presenting the optimum load impedance at the drain of the devices. This configuration is simple, has low losses and is responsible for the graceful degradation property.

DTI's design is a radical simplification of high-power, narrow band transistor-based amplifiers, and allows for straightforward scaling to increased power levels (hundreds of kilowatts) via combining multiple amplifier modules into a passive combiner (Fig. 1).

In Phase II of this Small Business Innovation Research (SBIR) grant, DTI built and tested a single-cavity system which reached 15 kW at 66% power-added efficiency with ten of 12 slots filled, on only one of two cavity faces. Combining of multiple cavities was also demonstrated at low power.

In a related effort, DTI has extended this design from 650 MHz to 1.3 GHz with similar results and hardware performance.

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CAVITY COMBINING OVERVIEW

The resonant cavity is a well-known means of combining or dividing power. Typically, a cavity has a high Q when unloaded; this means intrinsic losses can be very low. With heavy input and output loading, the loaded Q is much lower, giving good (wide) bandwidth while retaining the intrinsic low conduction losses of the cavity. The specified cavity mode offers a large, well-defined electromagnetic field structure which can be driven simultaneously by many transistors. In principle, various cavity geometry and mode combinations could be used with the cavity-combined amplifier concept. For simplicity, and many practical reasons, a cylindrical design (TM_{010} mode) was chosen for the prototypes, though a more complex coaxial or other structure may ultimately be used for a specific market-ready product.

The resonant cavity's ability to accommodate additional transistors without significantly changing the interior magnetic or electric fields by increasing the output coupling allows nearly linear increases in power per transistor and greatly simplifies each power output stage. The combination of many isolated inputs into a single cavity naturally gives a high degree of redundancy and a graceful degradation characteristic. With this design, a failure of one or several of these combined transistors has negligible performance impact. The amplifier module can continue operating stably with no interruption, and the low-level RF control system can simply adjust the drive to keep the accelerator field constant.

This behavior is important in an amplifier with a large number of transistors integrated into one module. An adequate (excess) number of devices are designed into the amplifier to provide a performance margin for one or more failures.

HIGH EFFICIENCY OPERATION

The power amplifier contains the Class-E output circuitry implemented for the transistor. The output cavity coupling circuit incorporates the harmonically-tuned output matching network for the transistor and interfaces directly to the cavity coupling loop. The ideal Class-E waveform allows a large current conduction angle for the transistor while simultaneously minimizing V x I losses in the device. This allows high efficiency and high power to be achieved in the same circuit. Thus Class-E (and related topologies) is superior to Class-AB which achieves high linearity at the cost of efficiency and Class-C which achieves high efficiency by employing a narrow current (conduction angle) waveform.

The DTI coupling loop topology is ideally suited for push-pull transistors. The output matching network was implemented with transmission-line matching elements via the stripline, stubs and the coupling loop itself.

SIMULATION AND DESIGN

The performance of the cavity amplifier was computed analytically and simulated in electromagnetic finite element analyses (FEA) and electronic design automation (EDA) software. The analytic results were useful for initial sizing and performance calculations, and the FEA and EDA results were useful for determining precise operating characteristics. Analytic solutions are used to identify the fields and generate the mode spectrum for the basic cavity, but FEA is used to investigate more complex structures incorporating the input and output couplers. Modelling is done in ADS and EMPro by Keysight.

CLASS-E CIRCUIT DESIGN

In the Phase I effort, a Class-E type tuning network was selected due to the large parasitic inductance of the drain connection to the transmission line (~2 nH per side) and the large output capacitance (~200 pF per side) intrinsic to high power RF LDMOS transistors. The effects of the large output capacitance and parasitic inductance can be resonantly tuned-out by presenting a capacitive load at the transformed end of the transmission line such that the transistor output capacitance, parasitic inductance, and capacitive transmission line load are able to efficiently resonate power out of the transistor.

A classic Class-E circuit presents a partially inductive impedance to the drain at the fundamental, creating a phase shift of about 50 degrees between the total drain current and voltage. This phase shift determines the point at which the load current is diverted from the transistor conduction channel to the transistor output capacitance. The phase shift along with the real loading resistance is chosen so (a) the capacitor voltage drops to zero before the switch turns on and (b) the capacitor voltage rises slowly when the switch turns off, thereby minimizing switching losses. Ideally a resonant tank at the load presents a short circuit at the load to all the harmonics, and the quarter-wave transmission line transforms these shorted harmonic impedances to a short circuit at the drain for the even harmonics and an open circuit to the drain for the odd harmonics.

In the cavity-coupled circuit, the impedance at the coupling loop is initially an inductance L_{loop} with an equivalent cavity loading resistance R_L in parallel. A capacitance stub can be added at the coupling loop to properly tune the impedance at the loop so the transformed impedance at the drains can efficiently resonate power out of the transistor, as mentioned above.

Based on the range of impedance values presented by the loaded cavity at the coupling loop, it was determined that a coupling loop impedance of $R_L = 20\ \Omega$, $L_{loop} = 4$ nH was an efficient and realizable operating point. Given the quarter wave transmission line, it was found that a net capacitance ~15 pF was near optimal for presenting a Class–E type inductance load.

EXPERIMENTAL RESULTS

We extensively measured transistor performance outside of the cavity, with a cavity equivalent load, to better model the parasitic components and design the tuning technique for efficient operation in the cavity. The input matching network was designed for a good match across a broad frequency range.

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The tuning stubs were then tested and found to conform to the simulations. Once the transistor was properly characterized outside of the cavity it was placed back into the cavity. Figure 2 shows the progression of power and efficiency for 1 to 4 coupled transistors, which achieved over 650 W per transistor at approximately 70% efficiency.

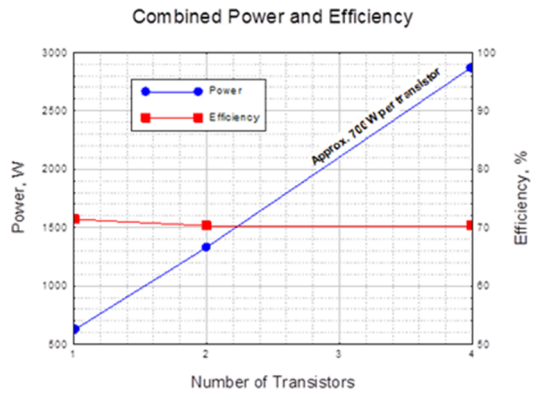

Figure. 2: Improved Phase I Class-E cavity output vs. Number of Transistor Inputs

200 kW SSA CONSTRUCTION

The next step was to build a complete 200 kW-class transmitter utilizing multiple cavity amplifier modules. The medium power outputs will be combined using a passive cavity combiner (Fig. 3). This SSA will operate at 650 MHz as required for PIP-II and other advanced linear accelerators, though the concept is readily scalable to other frequencies (as we recently demonstrated at 1.3 GHz).

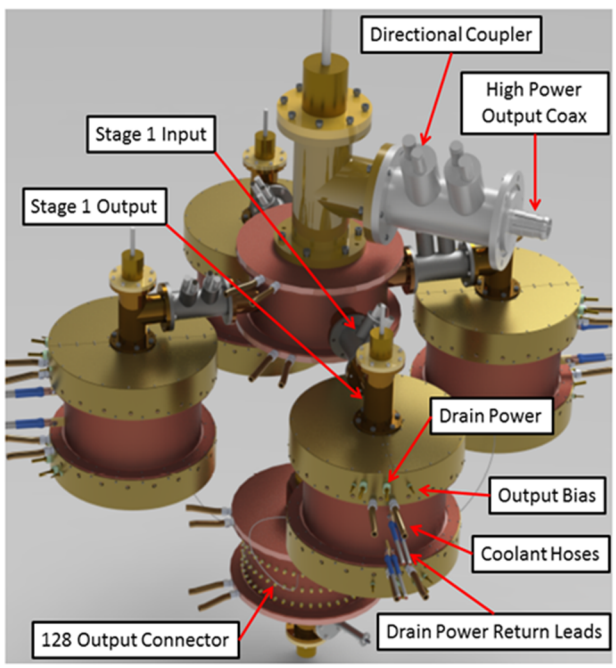

Figure. 3: Arrangement of 200 kW-class transmitter based on four cavity amplifier / combiner modules.

The modules consist of two "bolt-circle" diameters of transistors on each endwall. A set of twelve slots in each bolt circle allows 24 total coupling loops, each driven by one or more transistors. Recent developmental efforts, in addition to related work at 1.3 GHz, successfully demonstrated driving each coupling loop with four transistors. Assuming a saturated power output of 600 watts per transistor, four transistors per loop, and 24 loops, this results in the desired goal of 50 kilowatts per module with at least one redundant device, allowing N+1 redundancy and graceful degradation of output power in the event of a random transistor failure. Moreover, by driving each loop with four transistors, the system complexity is reduced and power density is increased for a given number of transistors. The cavity amplifier module mechanical details will also be upgraded for high average power operation with improved RF joints and cooling.

The outputs of the 50 kW class modules will be combined in a passive cavity combiner. We plan to combine approximately four amplifier modules in a simple pillbox cavity with four 31/8 " coaxial inputs and one larger coaxial output.

FEA modeling will be performed to estimate the voltages and currents in the passive cavity combiner and on the high power coupling loops. It is expected that the passive cavity may require purging or pressurization with dry air to prevent electrical breakdown.

CONCLUSION

DTI has demonstrated the efficiency and scalability of this cavity combiner design to optimize its performance under the Phase II of our SBIR grant from the Department of Energy. Moving forward, we believe that this technology will provide significant life cycle cost savings for existing and planned accelerator systems, in three areas : high reliability (much greater than klystrons); improved efficiency (lower electrical power costs); simplified drive electronics (no need for high voltage power supplies or modulators); and minimized RF and thermal connections.