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MTCA.4-BASED LLRF SYSTEM PROTOTYPE STATUS FOR MYRRHA

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Abstract

Within the framework of MINERVA, the first Phase of MYRRHA (Multi-purpose hYbrid Research Reactor for High-tech Applications) project, IN2P3 labs are in charge of the development of several accelerator elements. Among those, a fully equipped Spoke cryomodule prototype was constructed. It integrates two superconducting single spoke cavities operating at 2K, the RF power couplers and the associated cold tuning systems. On the control side, a MTCA.4-based Low Level Radio Frequency (LLRF) system prototype has been implemented by IJCLab including FPGA specific firmware, a new µRTM frequency downconverter module from the company IOxOS Technologies and EPICS developments in collaboration with the SCK CEN. The status of the LLRF system will be shown as well as its preliminary tests results.

INTRODUCTION

The MINERVA, is the first construction phase of the future MYRRHA facility (Fig. 1) [1]. It involves the realization of an accelerator up to 100MeV, composed of one injector operating at 176.1MHz [2] associated to a MEBT line including a fast switching magnet for a future parallel redundancy using a second injector, the first superconducting linac section (single Spoke cavities @352.2MHz) composed of fifteen cryomodules integrating 2 cavities each and a Proton target Facility.

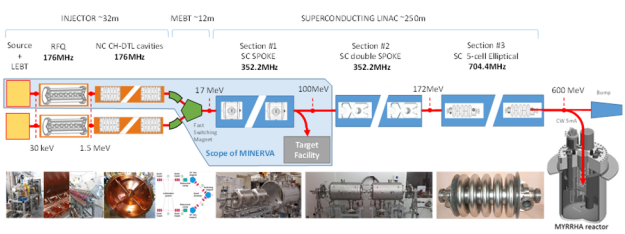

Figure 1: Conceptual layout of the MYRRHA Facility with in the cyan area, the MINERVA project (2019-2026).

A cooperation agreement on the ADS between the CNRS and the SCK CEN in 2017 has allowed to launch a specific prototyping contract, focusing on the realization and the tests of a fully equipped Spoke cryomodule at 2K and 20kW available by cavity for the accelerator field regulation [3]. Within this framework, a MTCA.4-based Low Level Radio Frequency system prototype has been developed and evolved with the a new flexible RF front-end µRTM prototype developed by IOXOS and IJClab, a complete overhaul of the firmware with new functions and an optimized implementation for a maximal 250 MHz clock operation, allowing to use this LLRF system for the superconducting linac and the injector of MINERVA.

LLRF SYSTEM: HARDWARE

The MTCA.4-based LLRF system prototype is designed around a main ditigal board, called IFC1420, a NATIVE-R5 from NAT and a MRF Timing system (Fig. 2) [4].

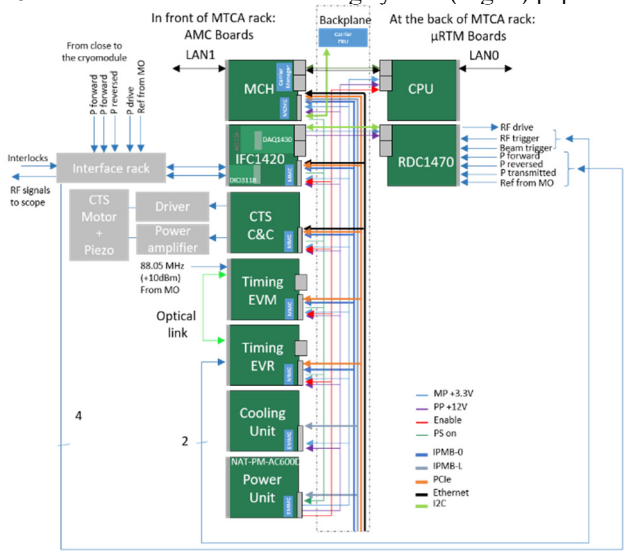

Figure 2: MTCA based LLRF prototype system scheme.

For more flexibility, the planned "Fast RF interlock" FMC mezzanine board prototype has been replaced by a FMC digital IO board called DIO3118 from IOXOS Technologies, associated to a specific 19" rack for the RF and interlocks signals conditioning and interfaces. Two boards have been also developed in collaboration, a µRTM RF Front-end prototype called RDC1470 and a second Cold Tuning System AMC board prototype including Motor and piezo-actuators C&C.

The RDC140 board integrates four RF channels allowing a signal conditioning (variable gain, filtering and two operation modes: Direct sampling or down converter) for sampling up to 250 MS/s. A specific Accelerator reference channel associated to a PLL provides the synchronized clocks to ADC, DAC, mixers in particular. In addition, 3 DAC channels enable two output operation modes: vector modulator or direct sampling. The board operates with RF signals at 176.1 MHz or 352.2 MHz selected by soft configuration.

The RDC1470 µRTM prototype (Fig. 3) has additional features including three triggers inputs (useable for RF, Beam and RF authorization triggers), two slow DAC and

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the possibility to provide a calibration signal to the RF channels and mezzanine filter circuits adapted to the frequency range used.

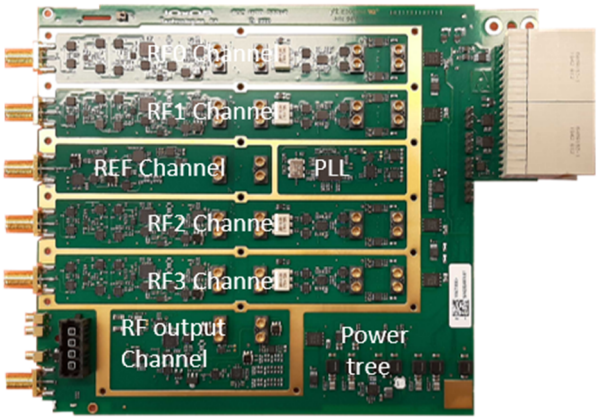

Figure 3: RFC1470 µRTM prototype board (IOXOS Technologies).

The RF channels have been characterized @176.1 ADC clock and a 44 MHz intermediate Frequency (IF), using High Speed data converter (Texas Instruments, rectangular window, full analysis bandwidth, 32768 samples).

Table 1: Channels Measurements

Signal (MHz)	SNR (dBFS)	SFDR (dBFS)	ENOB (bits)	Crosstalk (dB)
176.1	~67.2	~81	~10.85	>90
352.2	~66.6	~85	~10.76	>80

With a 10 MHz bandwidth of interest, the SNR is improved of 3 dB and the ENOB superior to 11.2 bits.

Concerning the CTS C&C AMC board (Fig. 4), it's associated to an external motor driver and a power module for the piezo-actuators in order to tune the superconducting cavity frequency using a cold tuning system [5]. An IPBUS interface with the LLRF IOC is implemented into a FPGA (KINTEX7) for receiving detuning data, as well as signal processing and data transfer to a microcontroller dsPIC managing the control signals of the piezo-actuators and the communication with the motor driver.

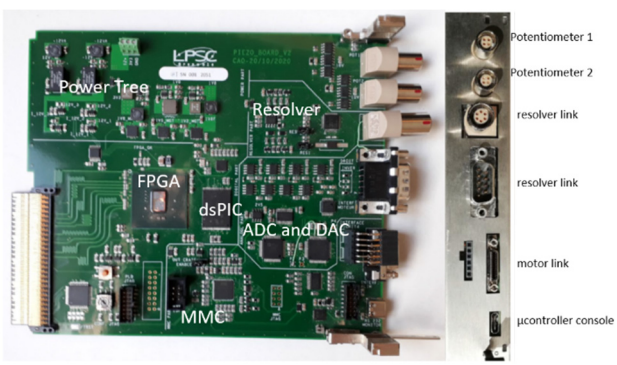

Figure 4: CTS C&C AMC board (LPSC).

LLRF SYSTEM: FIRMWARE

The user firmware developed with Vivado2018.3 is localised in a specific area where all the input and output signals linked to the hardware and data transfer are available. Compared to the RFQ firmware version (In-house LLRF prototype) [6], all the existing functions have been modified and improved to pass the timing constraints due to a max frequency used up to 200 MHz synchronized with the ADC clock and new functions added:

- Demodulation: two modes exist allowing an IQ demodulation with the minimum of latency needed for the normal conducting cavities used into the injector and the Non IQ demodulation with a 9/2 ratio, one extra ENOB for 20% of latency increase.
- Low pass filter (FIR): a low pass filter on I and Q values is implemented and can be by-passed.
- Amplitude and Phase conversion: the CORDIC IP of Xilinx is used with vector length adaption for respecting the constraints associated.
- IQ calibration: a rotation of the phase of the transmitted signal is realized to align it with the drive signal.
- IQ error and IQ set point: the error is calculated in function of the set point which can be a static value or a sequence of values corresponding to a ramp calculated into the FPGA.
- IQ GDR/SEL: it allows to operate either in Generator Driven resonator (GDR) mode using a Proportional Integral controller for regulating the accelerator field in magnitude, phase and frequency or in Self excited loop (SEL) mode allowing to find the eigenfrequency of the superconducting cavity in order to tune it with the CTS.
- IQ Open/Closed Loop: the open loop mode implies the application of specific values on the IQ drive signals for debugging or calibration and the closed loop allowing the GDR or SEL operation.
- Min Sign Level: to provide the detuning phase for tuning the frequency of the cavity, it necessary to verify that a signal level is sufficient for calculating the phase with the CORDIC avoiding the mechanical deformation if not the case.
- Limit voltage detection: an interlock is implemented for the forward, reflected and transmitted RF signals in order to protect the accelerating section: cavity, FPC, HSSPA.
- Triggers and operation modes: Triggers and operation modes are managed in function of the Machine protection System and the Personnel Safety System.

The LLRF data are exchanged using 64 registers of 32 bits using in read mode for the commands registers and in write mode for the supervision registers. In parallel, others data interesting IQ data are also buffered in large buffers used as circulars buffers with a time resolution around 130ns and the time depth of 0.5 ms working with a pre and post trigger data.

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LLRF SYSTEM: SOFTWARE

Based on the ESS E3 framework [7], an EPICS IOC has been developed to run via NFS (Network File System) on the IOxOS board under the "YOCTO" embedded OS (Fig 5). This IOC manages the data exchanges between the board's FPGA and the supervision. It also allows raw data from all RF channels to be captured in buffers for post-mortem analysis. The TscMon runtime is integrated into the IOC to allow configuration via simple scripts.

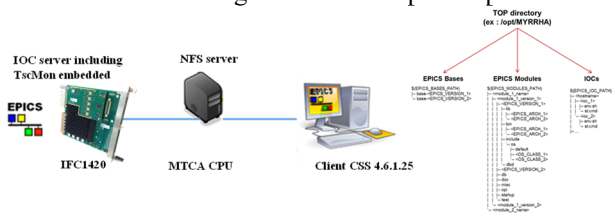

Figure 5: EPICS and OS integration.

TEST RESULTS @176.1 MHZ

A power tests campaign has been realized on one rebuncher cavity of the injector operating at 176.1 MHz using 6kW RF power (max). The first step concerns the frequency tuning of the cavity, using the open loop mode allowing to use a lower RF power level, for tuning the cavity frequency to 176.1 MHz: the LLRF system provides to the motorized plunger driver the detuning angle, an available process variable thanks to EPICS IOC, which is moved by the operator targeting the best return loss value.

The second step consists to calibrate the transmitted power signal to be in phase with the RF drive signal. Once done, the frequency tuning system is set to automatic mode. The increase of power, the third step, is facilitated with the automatic ramp to the nominal value.

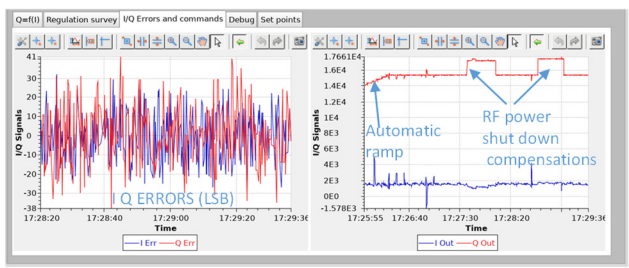

Figure 6: IQ errors and drive during a ramp and PSSA modules shut down.

As shown in Fig. 6, the system is sufficient to operate with the increase of power, during the nominal set point operation and with the loss of one module of the SSPA thanks to a low latency. As shown in the Table 2, the worst latency is due to the RF front-end and the signal processing performed by the FPGA with the Non IQ demodulation mode (9 Samples /2 IF periods), but a factor 3 lower than the filling time of a the RFQ or the rebunchers cavities used into the injector.

Table 2: Latency

Components	Latency
LLRF system (Non IQ demod. mode)	0.680 µs
SSPA (Measured with cables =0.4µS)	0.100 µs
Cables (estimate : 5ns/m)	0.300 µs
Total Latency	1.180 µs

Concerning the amplitude and phase, the stability values achieved the requirements +/- 0.1% rms and +/- 0.1° rms until an operation set point under -10dBFS, knowing that the input signal range could be adapted to the ADC range with gain up to 52 dB (60dB in the new version).

CONCLUSIONS

The LLRF prototype is validated at 176.1 MHz for operating on the injector prototype. This system constructed around an IOXOS technologies main board (IFC1420) has involved a major effort of improvements and reliability concerning the firmware and the driver associated, through numerous test, today rewarded. A new version of the µRTM RF front-end will be designed to add more flexible about the usable frequencies (RF, IF and ADC/DAC clocks) for future Accelerator projects. Last step is the validation of the LLRF prototype performances @352.2 MHz in nominal condition on the two Spoke superconducting cavities inside a cryomodule prototype at 9 MV/m and 2 K before the end of 2022. Fault tolerance strategies will be also tested with it.

ACKNOWLEDGEMENTS

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