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PROGRAMMABLE SLED SYSTEM FOR SINGLE BUNCH AND MULTIBUNCH LINAC OPERATION

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Abstract

The Diamond Light Source pre-injector linac generates single bunch and multibunch 100 MeV electron beams for top-up and fill of the storage ring. Two high-power 3 GHz klystrons are required for reliable injection into the booster. In order to introduce redundancy, a SLED pulse compressor is being installed so that the linac can operate from just one klystron, with the second klystron held as a standby. A phase flip can be used to generate a transient RF spike, suitable for single bunch operation, and a programmable amplitude and phase drive profile can be specified to generate a constant-power output suitable for multibunch operation. Details are presented of design, installation and high-power operation of the SLED system, and the ability to generate a long pulse, including corrections for klystron nonlinearity and deviations from modulator flat-top, is demonstrated.

LINAC DESIGN AND OPERATION

A schematic diagram of the present Diamond linac power distribution is shown on the left side of Fig. 1. Klystrons K1 and K2 power primary and final bunching units (PBU and FBU) and two accelerating structures (AS1 and AS2). One klystron powers PBU, FBU and AS1 and the other powers AS2. Beam from AS1 can drift through AS2 and so two waveguide switches (SW1 and SW2) allow either klystron to power the bunchers and AS1 to deliver low-energy beam to the booster in the event of a klystron or modulator failure [1].

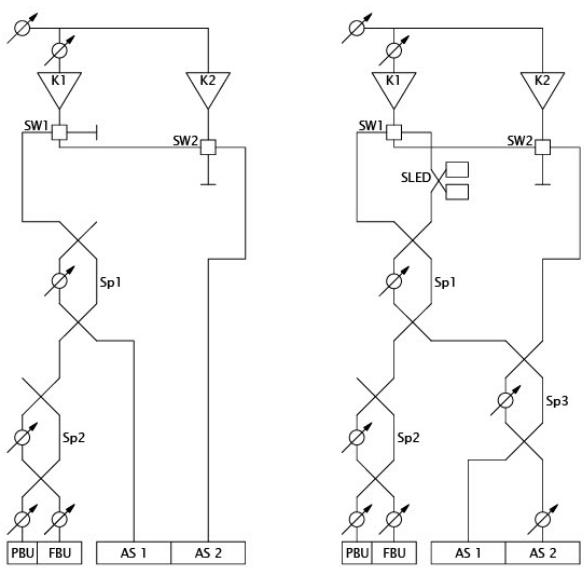

Figure 1: Linac configuration without (left) and with (right) SLED cavity.

Injection efficiency into the booster is poor at low energy, and so a SLED is being installed to enable full energy operation with one klystron. The right side of Fig. 1 shows the network with the SLED. Power from either klystron is compressed in the SLED and then split to the linac structures by power splitters Sp1, Sp2 and the new Sp3, which controls relative powers in AS1 and AS2.

SLED CAVITY PARAMETERS

Pulse compression is achieved by using the first part of a high-power RF pulse to charge the SLED cavities and then adding the second part of the pulse to the SLED cavity discharge [2]. Figure 2 shows an analytic solution for the fields (= √power) in the cavity charge and discharge process, with the bold blue line representing the summed pulse delivered to the linac. The RF pulse is divided in two by a 180° flip of the input phase, shown as a change of direct output from +1 to -1.

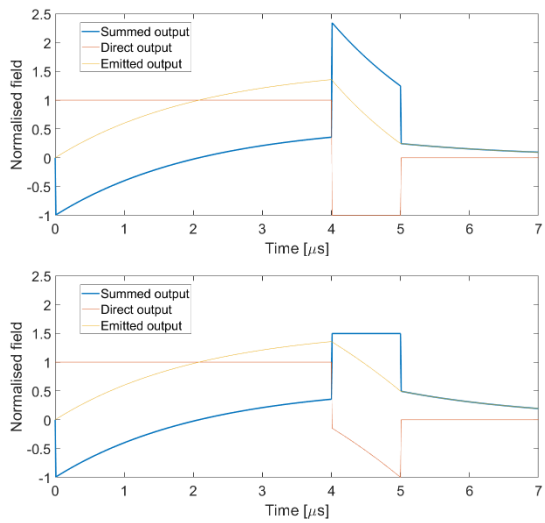

Figure 2: Calculated SLED performance with phase flip (above) and additional amplitude shaping (below).

The upper plot in Fig. 2 shows the sharp spike generated by a simple phase flip. This pulse shape can be used for single-pulse operation, but multibunch operation requires equal acceleration of every bunch in a 500 MHz 120-bunch train, duration 240 ns. The accelerating structure filling time is 740 ns and so the SLED must deliver a flat high-power pulse of duration 1 μs. The lower plot shows a 5 μs RF pulse with a flip at 4 μs and a post-flip pulse amplitude modulated to generate this 1 μs flat output pulse.

SLED parameters were chosen to generate a long flat pulse: cavity Q_0 was slightly above 100,000 and coupling β was 4.0, suitable for a 1 μs double-power pulse.

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The SLED cavities and hybrid combiner, supplied by RI Research Instruments, are shown in Fig. 3. The linac waveguide is filled with SF_6 and the SLED operates under vacuum and so two windows are required: a low power input window suitable for uncompressed klystron output, and a high-power output window capable of transmitting the full klystron power after maximum compression. The output window was built by VitzroNextech based on the PLS-II/PAL-XFEL high-power linac window design [3].

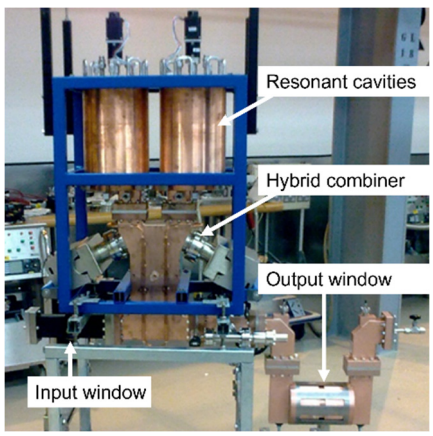

Figure 3: SLED cavity assembly.

LOW LEVEL RF

The digital LLRF system architecture, shown in Fig. 4, is based on the Micro Telecommunications Computing Architecture (MicroTCA) standard. The LLRF consists of a 2U MTCA.4 chassis, a MCH, an AMC computer board, a Struck SIS8300-KU card and a Struck DWC8VM1 rear-transition-module with supporting clock/local oscillator (LO)/reference generation RF circuits.

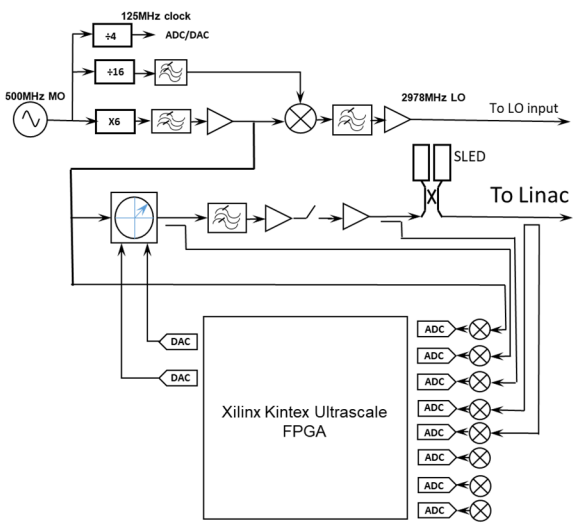

Figure 4: Low level RF schematic.

The AMC computer board is an AM G64 from Concurrent. It communicates with the FPGA through PCIe bus. It runs Linux and EPICS IOC and provides the interface to the Diamond control system. The SIS8300-KU has a Xilinx Kintex Ultrascale FPGA, 10 channels 16-bit ADC and 2 channels 16-bit DAC. It has a 4 lane PCIe Gen3 interface. The DWC8VM1 has 8 channels downconverter and one vector modulator.

The clock, IF, LO and 3 GHz are all derived from the 500 MHz master oscillator and are naturally synchronized. Clock frequency is four times the IF frequency, as IQ demodulation is used in the firmware.

An external trigger is provided by the timing system. It is sampled by one of the two DC ADC channels. The IF signals are sampled and demultiplexed into IQ components. The CORDIC algorithm translates IQ components to amplitude and phase before comparing them with the set points. Three modes were built into the firmware: standard phase flip, arbitrary output in the final 1 µs and full arbitrary output. Phase and amplitude feedback can be used to correct the pulse-to-pulse variation and long-term drift in the first two modes.

There are two RJ45 connectors on the front panel of the SIS8300-KU, providing 4 LVDS digital inputs and 4 LVDS digital outputs. They are isolated and translated into TTL signals using CN0256 board from Analog Devices. These digital inputs and outputs are used for interlock signals.

LOW POWER TESTS

The two resonant cavities of the SLED can be mechanically tuned by deformation of the end plates using a screw mechanism. Cavity frequency as a function of screw turns is shown in Fig. 5. The cavities were tuned to the operating frequency and low-power pulse compression was demonstrated. No further mechanical tuning is envisaged.

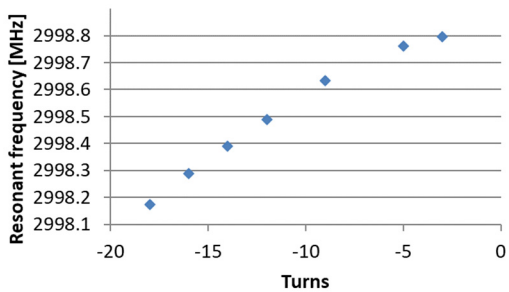

Figure 5: Mechanical tuning of SLED cavity.

Further frequency tuning is possible by changing the temperature of the water-cooling circuit, shown in Fig. 6 for temperatures of 37°C and 50°C. Fine tuning established an optimal operating temperature of 38.4°C.

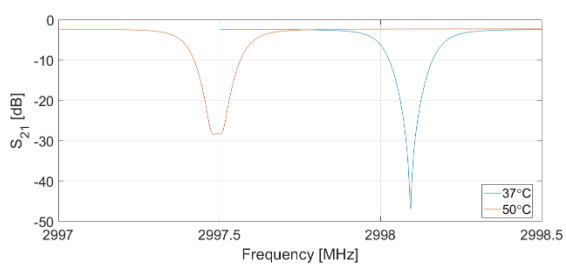

Figure 6: Thermal tuning of SLED cavity.

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HIGH POWER TESTS

The SLED system was mounted for high-power testing on the free stub of switch SW1 in Fig. 1. SLED output was directed to a water-cooled load and measured with directional couplers after the output window. The SLED was isolated from the klystrons with a 4-port circulator, as shown in Fig. 7.

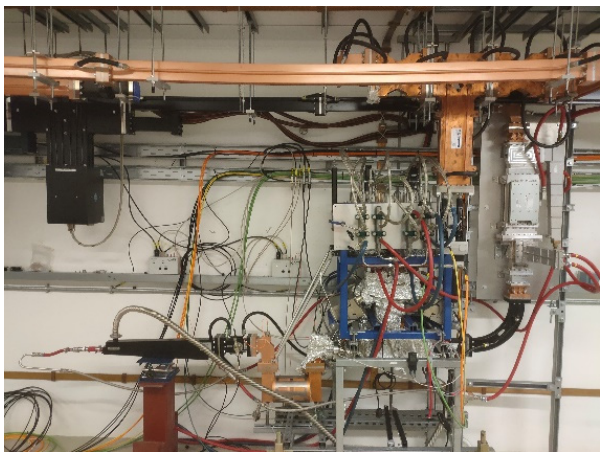

Figure 7: Installation for high power test into water load.

The ideal klystron pulse calculated in Fig. 2 assumes a klystron RF output with a perfect flat-top and zero rise and fall times. The true pulse, shown in Fig. 8 for a rectangular drive with constant phase, differs somewhat from this ideal, and so the LLRF drive pulse must be empirically tuned to compensate for modulator and klystron nonlinearities and limited switching bandwidth.

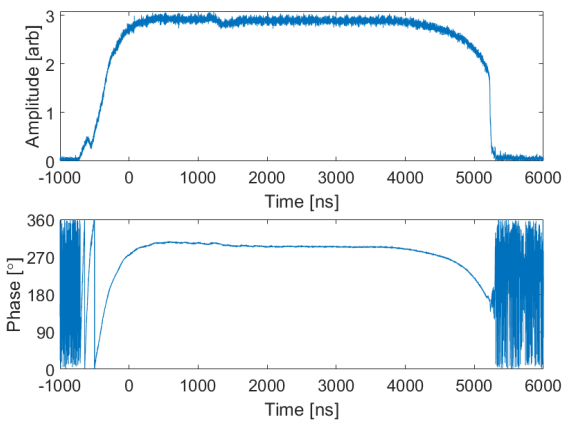

Figure 8: Klystron output with square drive.

The flexible digital LLRF defines the drive amplitude and phase as independent arrays that can be modified point-by-point, allowing the SLED pulse to be optimised. Figure 9 shows in blue the droop in klystron output at the ends of a 10 MW 5 µs RF pulse when driven by a linear approximation to the ideal waveform. The droop in amplitude ramp after the phase flip can be easily corrected by editing the LLRF demand, leading to the linear red curve.

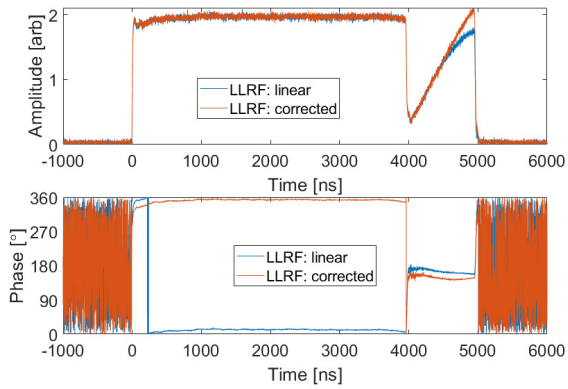

Figure 9: Klystron output with empirical LLRF tuning.

The droop in the uncorrected output is clear when measured after the SLED, shown in blue in Fig. 10. The corrected red curve, however, maintains a flat 20 MW output over the entire 1 µs duration.

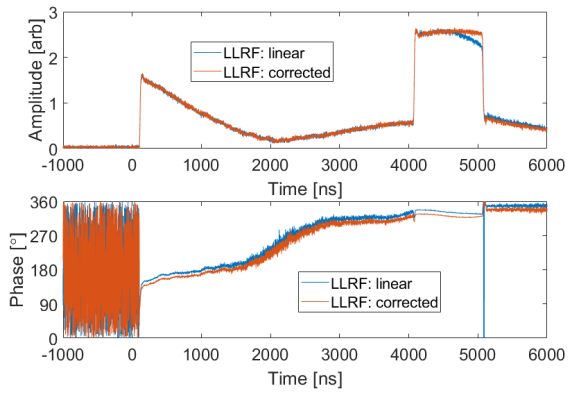

Figure 10: SLED output with empirical LLRF tuning.

PRESENT STATUS AND SUMMARY

High-power pulse compression and doubling in amplitude of the flat 1 µs RF pulse has been demonstrated, and so in August 2022 the water-cooled load is being removed and the waveguide link from the SLED to the bunchers and first linac accelerating structure is being installed. This will allow the pulse compression to be further optimised to generate a uniform train of 120 bunches in long-pulse mode and enable a new high-energy single bunch mode of operation. Once satisfactory operation with beam has been proven, the waveguide network can be completed and the linac can function with one operating and one redundant klystron.

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[3] Y. Joo *et al.*, "Development of new S-band RF window for stable high-power operation in linear accelerator RF system", *Nucl. Instrum. Methods Phys. Res. Sect. A*, vol. 866, pp. 1-10, 2017. doi:10.1016/j.nima.2017.05.031