Single LLRF for Multi-harmonic Buncher

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Introduction

The re-accelerator (ReA3) at the National Superconducting Cyclotron Laboratory (NSCL) mainly runs 80.5 MHz RF. The existing multi-harmonic buncher (MHB) runs at 80.5 MHz, 161 MHz and 241.5 MHz RF (latter not actively used). To achieve an increased separation of the beam bunches and minimization of bunch lengths desired for many types of experiments that use time of flight measurements, a lower frequency prebuncher that runs at 16.1 MHz (f_1), 32.2 MHz (f_2) and 48.3 MHz (f_3) is designed.
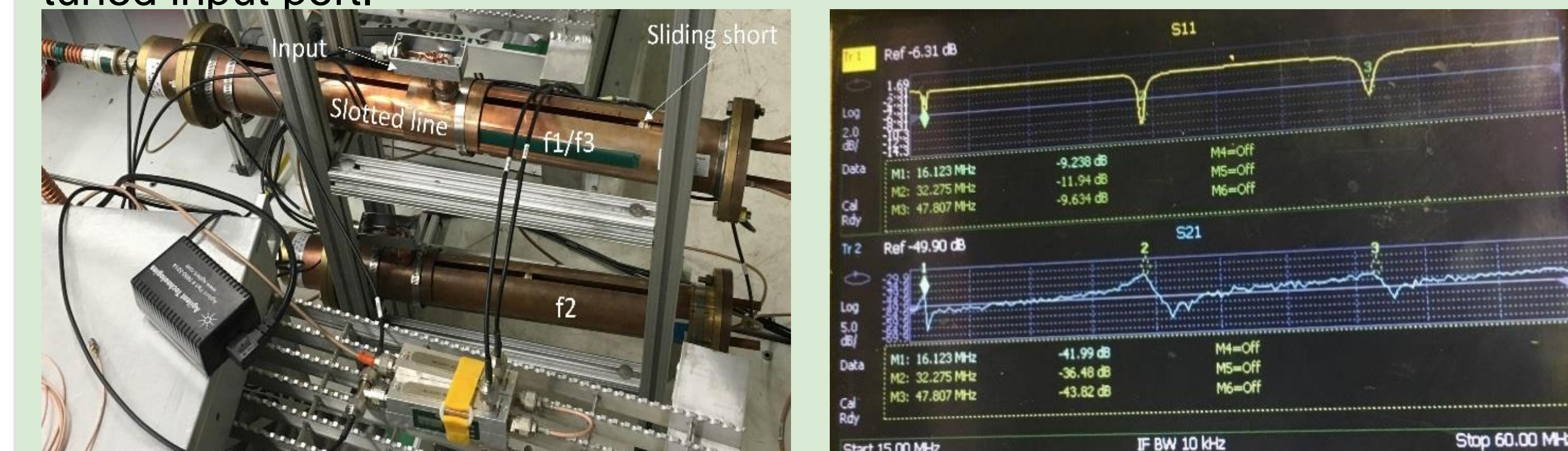
RF Design

Normally three low level radio frequency (LLRF) controllers will be needed for the control of each frequency component of the MHB, e.g. in the ReA3 MHB and FRIB MHB. Since the frequencies of the prebuncher are close enough, one wide band power amplifier could be used for all three frequencies. Also with the more powerful field programmable gate array (FPGA) chip, it is possible to accommodate the logics, including digital mixing, filtering and feedback control, for all three harmonics in a single LLRF controller.
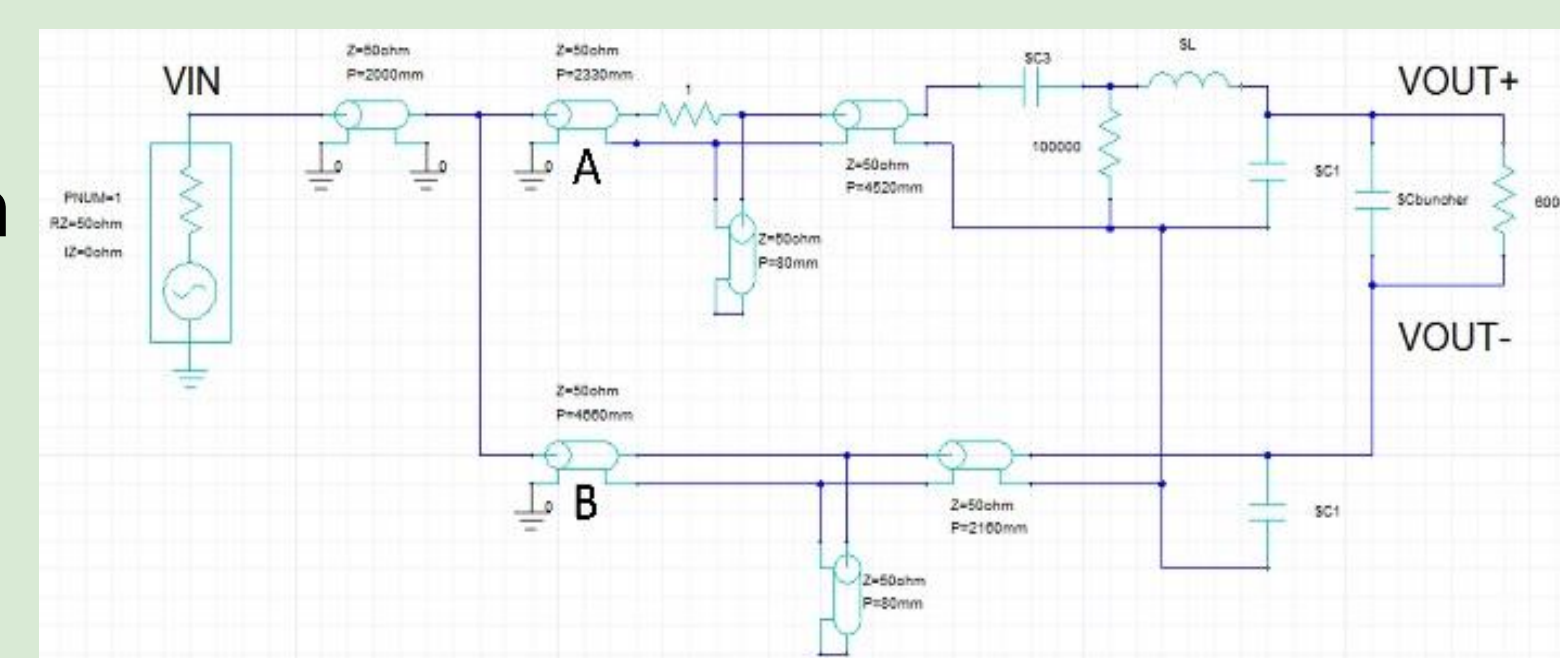
Resonant Circuit

An effective way to achieve high voltage across the buncher Electrodes is using resonant coaxial structures. For this application, two resonant structures were used in parallel. A first coaxial cable was resonated at f_1 and f_3, and a second cable was resonated at f_2. In the above schematic of the RF circuit, the lumped elements represent the feedthrough connections and electrode gap capacitance. Good isolation can be achieved by carefully selecting the lengths of cables A and B.

Each resonant structure includes a roughly quarter wavelength section of 7/8" air-dielectric coaxial cable (RFS HCA78-50J) that was coiled to save space. A piece of 3-1/8" rigid transmission line was used as an input-tuning section (picture on the left), which consisted of a sliding short and a slot tuned input port.
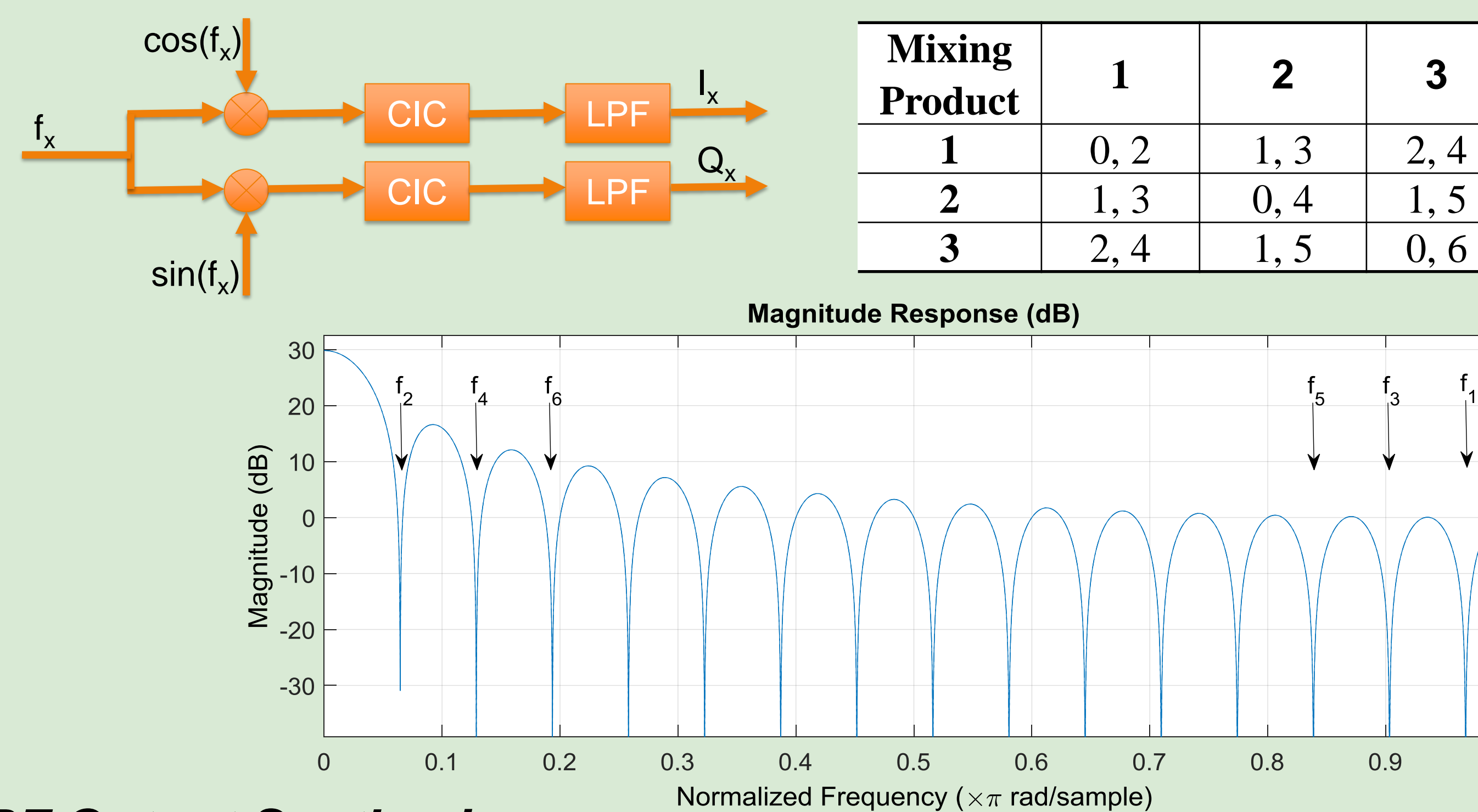

All three frequencies were matched simultaneously with return loss better than -9 dB.

RF Design

RF Inputs Sampling and Processing

The sampling frequency is chosen as 31.19375 (=16.1*31/16) MHz.

| Mixing Product	1	2	3
1	0, 2	1, 3	2, 4
2	1, 3	0, 4	1, 5
3	2, 4	1, 5	0, 6

RF Output Synthesis

The digital-to-analogue converter (DAC) sampling frequency is set to $16*f_1$ (257.6 MHz). The coordinate rotation digital computer (CORDIC) algorithm is used to generate the additional points, by converting the I/Q pair to amplitude/phase, adding fixed phase offsets of 22.5º, 45º, and 67.5º, then converting back to I/Q pairs.
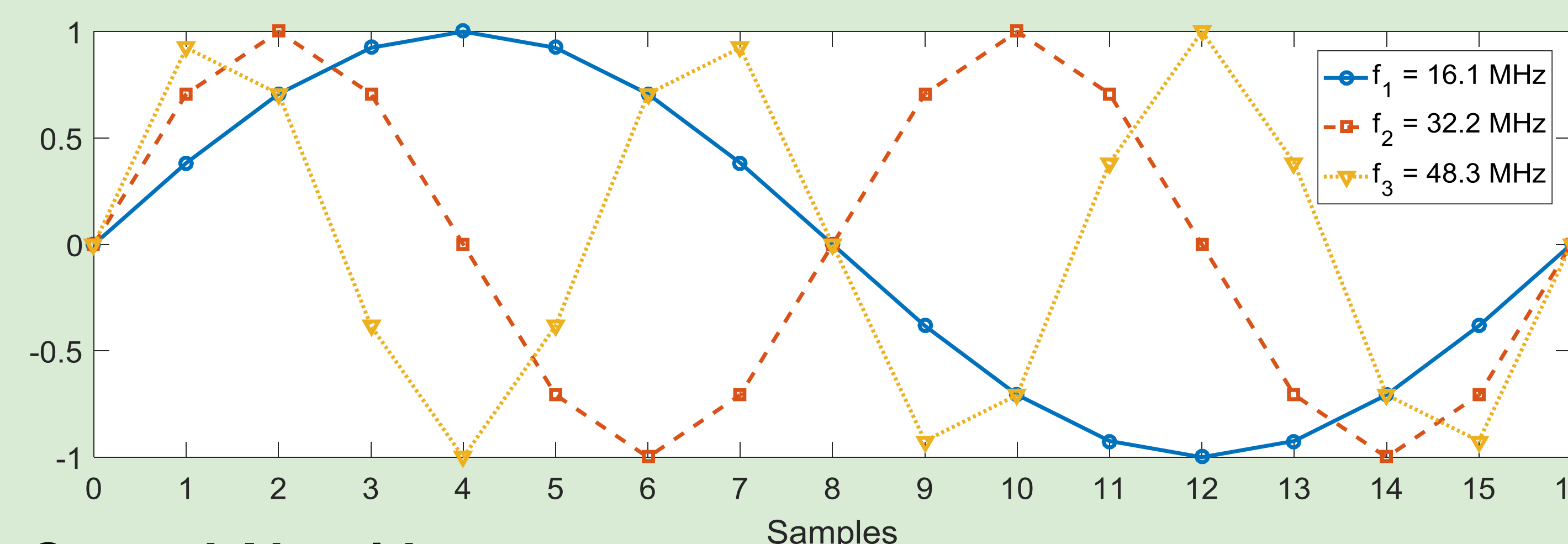

Control Algorithm

A special advanced control algorithm called active disturbance rejection control (ADRC) is used at NSCL for microphonics suppressing since 2011. The ADRC is well known for its capability of decoupling system variables.
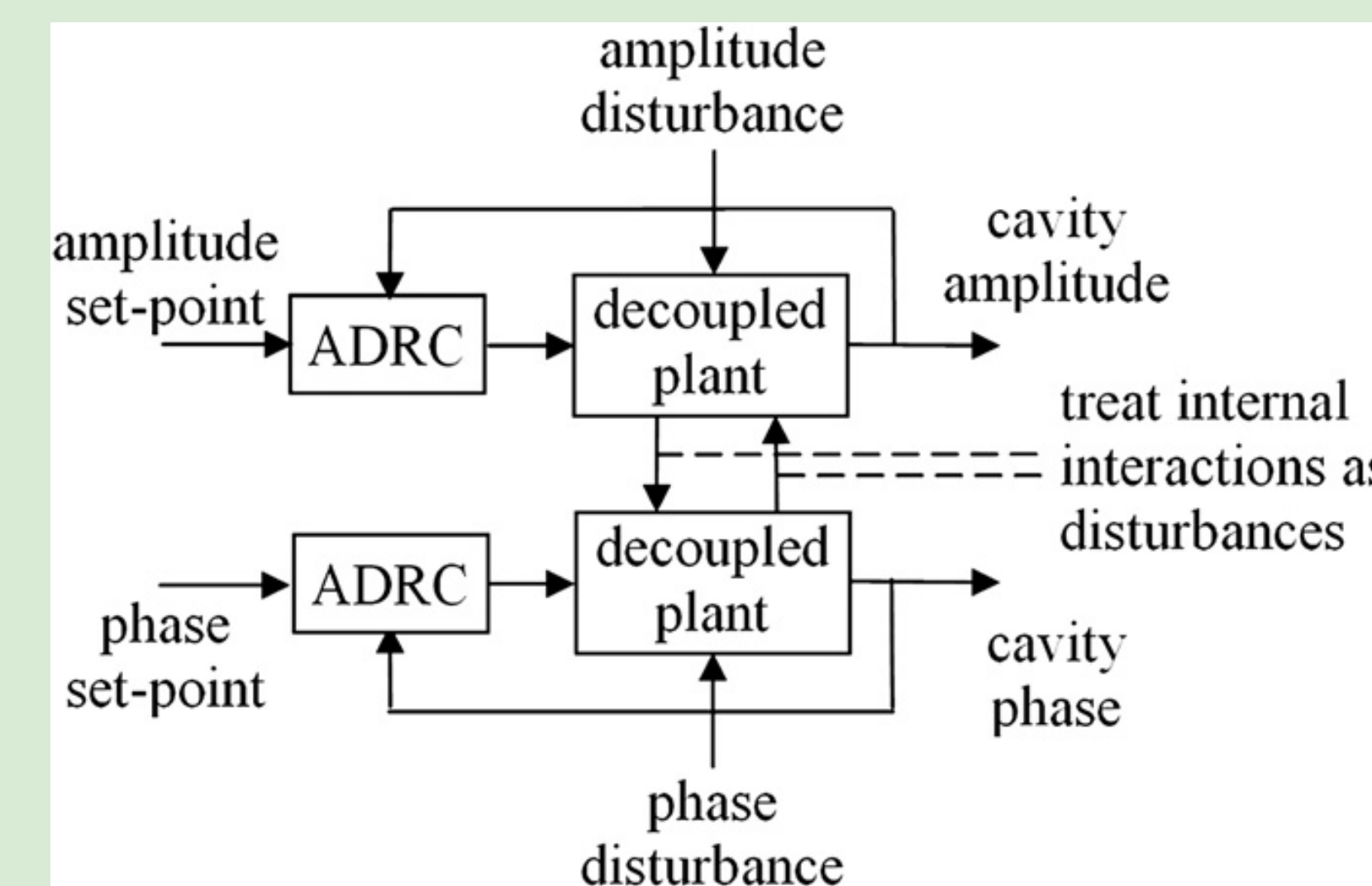
In this application, there is an independent ADRC process for each output frequency. Each control loop produces an I/Q output. I/Q control rather than amplitude and phase control is adopted, due to the simplicity of RF output synthesis in the I/Q domain.

Bench Test

Test Setup

EMPOWER 2160-BBS2E3DKM
20~125 MHz, 100 W
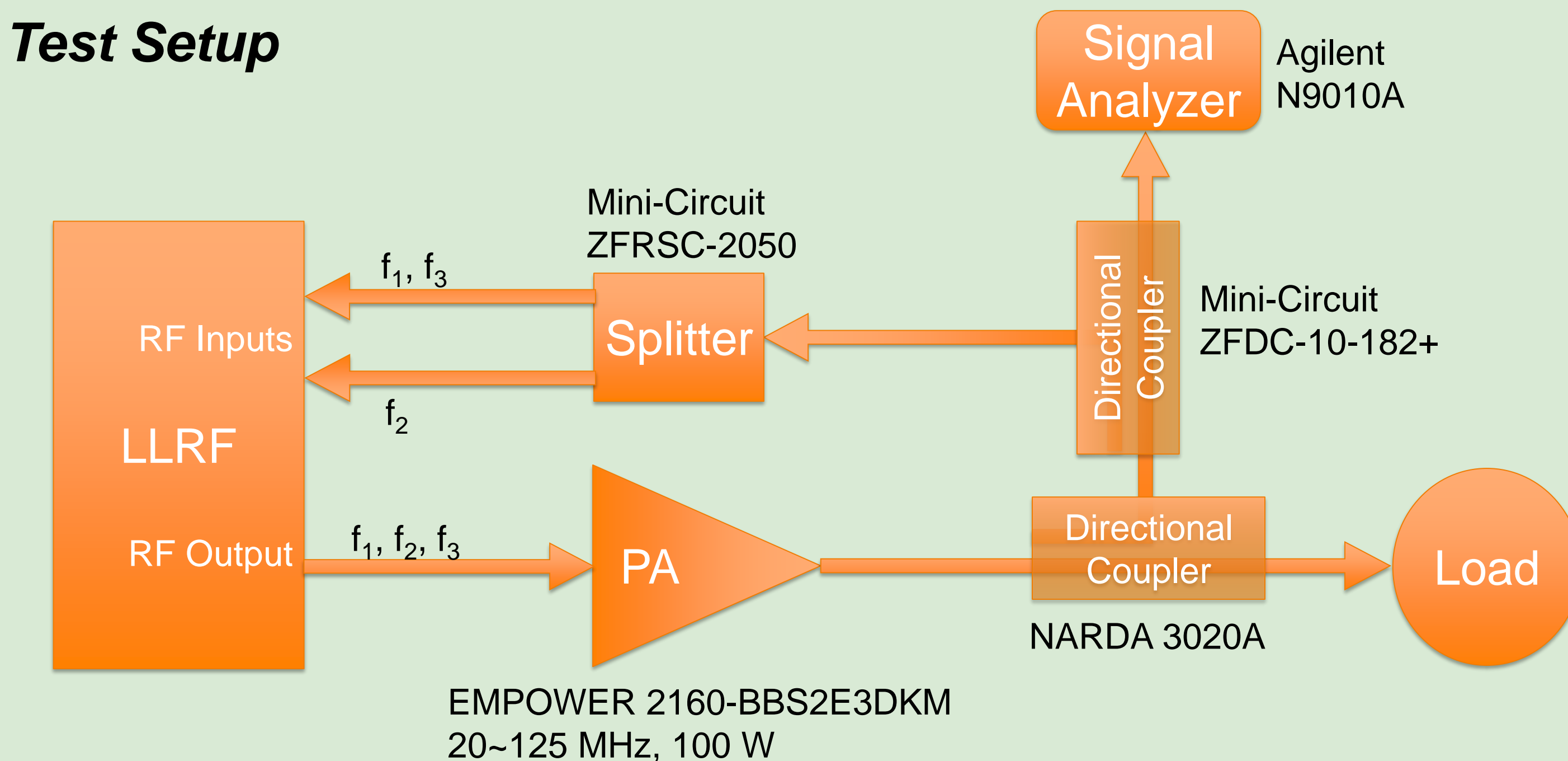
Test Results

f_1, f_2 and f_3 are all in open loop, set-points for f_2 and f_3 are zero.

f_1, f_3 are in closed-loop, f_2 is still in open loop.

Experimental Results

In February 2016, an experiment using the prebuncher was carried out in ReA3. The amplitude and phase set-points for f_1 are 335 V and 22°; the amplitude and phase set-points for f_2 are 35 V and 202°; f_3 is not used and was driven to zero.

Error	f_1 (16.1 MHz)	f_2 (32.2 MHz)
Amplitude peak	0.249%	2.775%
Amplitude rms	0.069%	0.756%
Phase peak	0.146°	1.832°
Phase rms	0.066°	0.429°
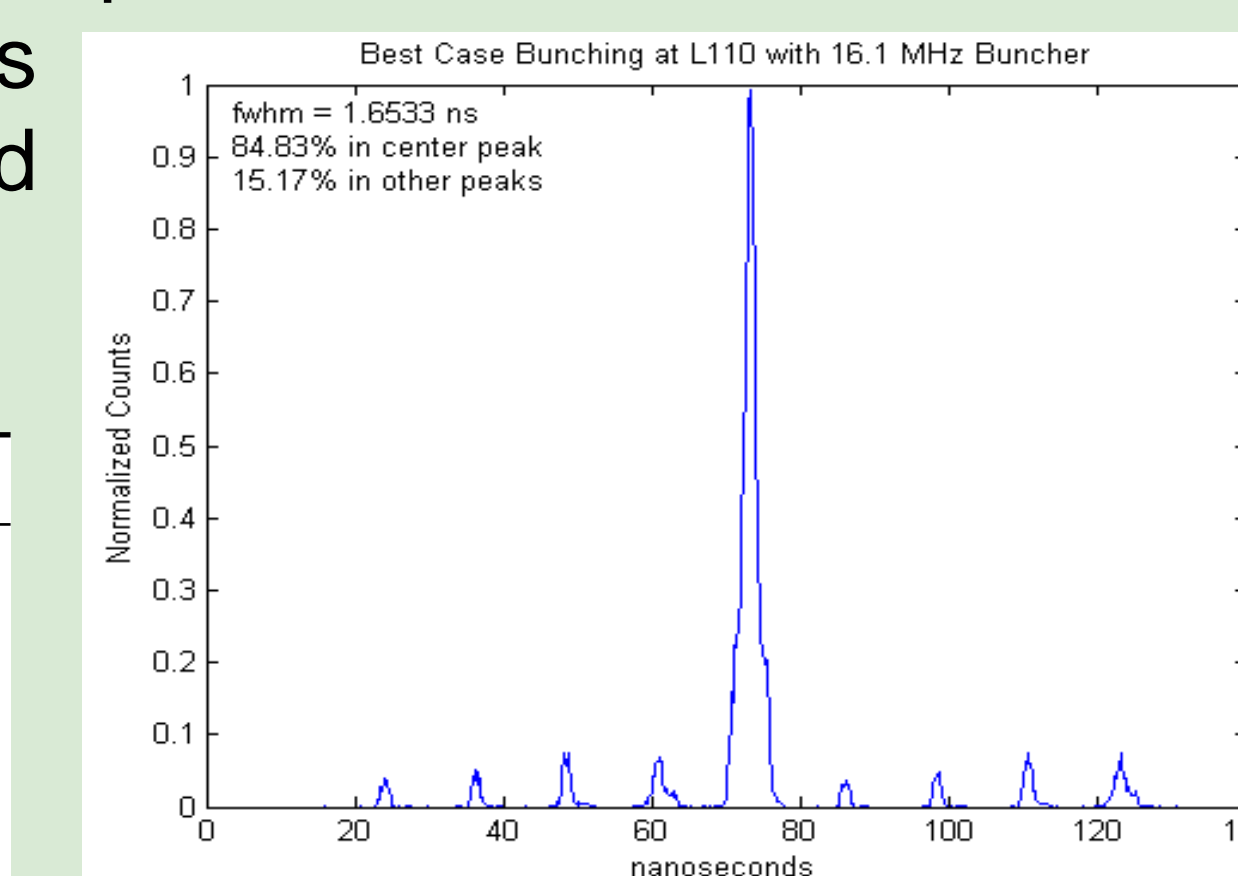
Conclusions

This unique LLRF design is more cost effective compared to the conventional designs (saves two sets of LLRF controller and amplifier), while providing satisfactory performance.