EPICS IOC Prototype of FRIB Machine Protection System

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Introduction

The FRIB Machine Protection System (MPS) is designed to protect accelerator components from damage by the beam in case of operating failure. It includes one master and fifty-six slave nodes and monitors critical signals. Once the condition to stop beam is detected, it issues a command to evoke the mitigation devices to switch off the beam. MPS interfaces with all the devices required to stop the beam quickly as well as the Run Permit System (RPS), Global Timing System (GTS), and the MPS IOC. The MPS IOC is based on the asynPortDriver module and communicates with MPS nodes via a custom UDP-based protocol.

System Overview

The MPS system consists of 3 virtual machines running a Master IOC, a Slave IOC, and a CS-Studio OPI. The Master IOC communicates with the master node and the Slave IOC communicates with all the fifty-six slave nodes.

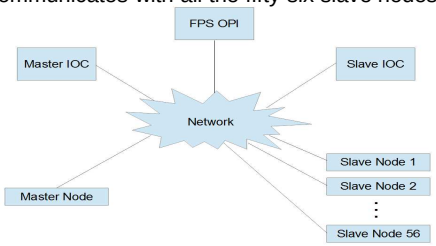

Figure 1: MPS Network Architecture

LCP Protocol

LCP (LLRF Control Protocol) is a UDP-based application layer protocol originally defined for FRIB LLRF. LCP has the following features:

- *Command Definition:* It defines commands for register read/write, waveform upload, persistent memory erase/read/write, and DDR raw data upload.
- *Register Definition:*
  - Read-Only register: Read from controllers periodically.
  - *Write-Anytime register:* Written to controllers periodically.
  - *Write-Once register:* Written to controllers once/value change.
- *UDP packet process:* Two threads are responsible for reading or writing data from or to controllers. A Sync thread used in request/response mode and an async thread used in streaming mode.
- Implementation: The source code of LCP is divided into a base class for UDP communication and a derived class for application-specific logic.

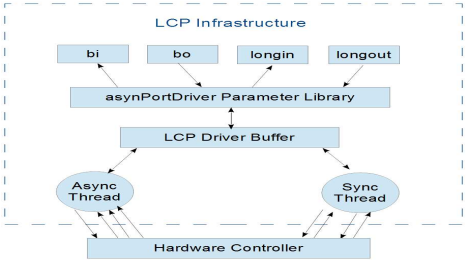

Figure 2: LCP Infrastructure

MPS IOC Basic Functionality

The MPS Master IOC is responsible for controlling the Master node and the MPS Slave IOC is responsible for controlling all the slave nodes. Most of functionality in the Slave IOC are also included in the Master IOC. The MPS Master IOC has the following features:

- *LCP Status: The* IOC reads hardware information from controller and monitors the UDP connection status. It is a useful diagnostic feature to track UDP communication between IOC and controller.
- *I/O Port Status:* Reads INP/OUT port configuration and OK/NOK port status from the controllers.
- Daisy Chain Status: Reads daisy chain diagnostic information from the controllers.
- Mask Config: Each MPS slave node has 96 ports connected to sensors in other systems. The IOC provides a mask bit for each slave port to mask or unmask.
- Self-Test: The IOC provides a self-test interface for DDR test, LED test, front panel test, rear panel test, and so on.
- Response Time Calculation: When MPS trips, the IOC calculates response time as follows: respTime (ns) = (ts_master - ts_slave) * 1000 / 80.5

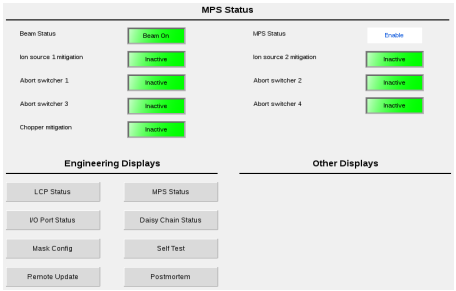

Figure 3: MPS Master OPI

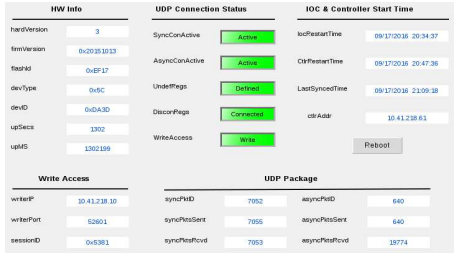

Figure 4: LCP Status Page

Remote Update

A remote update feature is included to update the FPGA firmware in the flash memory in the Master and Slave node controllers. The image that needs to be written to flash is divided into a header, a golden image, and a working image. Updates are performed by writing to a waveform PV. Update command and progress PVs are provided for each MPS node.

Figure 5: Remote Update User Interface

Table 1: Remote Update Performance Test

Nodes	1st	2nd	3rd
1	2m 02s	2m 04s	2m 01s
5	2m 02s	2m 02s	2m 00s
10	2m 03s	2m 02s	2m 03s
56	2m 22s	2m 21s	2m 22s

DDR Raw Data Transfer

When MPS trips, up to 256MB raw data may need to be transferred from a controller to the IOC. In order to improve the performance, DDR raw data is transferred in streaming mode. One transfer thread, one receive buffer and two UDP sockets are created to receive and process the UDP packets

Table 2: DDR Raw Data Performance Test

Test	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	Ave
Time (s)	21	22	18	20	15	22	17	20	18	19.2

Conclusion

At this time, all the MPS features for FRIB Front-End commissioning have been completed and the IOCs deployed in the FRIB test bed.

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