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RF SYSTEM ON A CHIP: A COMPACT CONTROLLER FOR SRF CAVITY FIELD AND DETUNING CONTROL

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Abstract

For SRF cavity systems operated in continuous wave (CW) at low effective beam loading as in Energy Recovery Linacs or Free Electron Lasers with rather low beam current, control of the tuning and counteracting any detuning caused by microphonics or Lorentz force driven coupled ponderomotive instability is mandatory to deliver and preserve a stable beam in longitudinal phase space regime.

To develop beyond the currently employed mTCA based LLRF systems, a compact RF on a chip system was developed, which features several potential applications.

Those range from a digital PLL to test and characterize the RF performance of cavities to a selection of detuning control algorithms, we have worked on it recent years, as e.g. a Kalman filter based state estimator controller [1] or an adaptive feedforward algorithm [2].

Here, we will show our first experimental findings with a TESLA style nine-cell SRF cavity operated in CW at our horizontal test facility HoBiCaT.

FUNCTIONALITY OF RFSOC CONTROL AND MEASUREMENT SYSTEM

The existing RF resonator characterization system of the HoBiCaT laboratory is quite extensive equipment, including an analog PLL, information acquisition and processing systems based on NI components used for such service functions as determination of resonator quality factor by pulsed signal attenuation curve, digitization of resonator detuning and others, as well as a control system based on mTCA equipment. The latter surpasses for the moment the projected RF System on a Chip (RFSoC) both in quantity of simultaneously controlled resonators, and in functionality, thus introduction of any service functions is possible, but limited by inconvenience of interface with existing framework of firmware, involvement of developers and so on. As a result of the two above-mentioned definitions, it was decided to develop a prototype device that replaces the functionality of all expensive measuring equipment, while allowing the developer without special knowledge of FPGA architecture and high skills in its programming to quickly implement scientific ideas and test them. Xilinx RFSoC was chosen as a market available integrated solution, supported by both Xilinx and third-party development tools such as Matlab SoC Blockset. A great advantage of this system on the Fig. 1 is the presence of a template that integrates the analog part of the chip, the user programmable logic and the processor through an automatically generated AXI interface between these components, the presence of an RF Data Converter interface, and intellectual property support from tools like the DSP HDL, HDL Coder for the programmable logic and the Embedded Coder for the processor logic. In this case, the system description familiar to many users can be classified for execution in programmable logic or processor and automatically transferred.

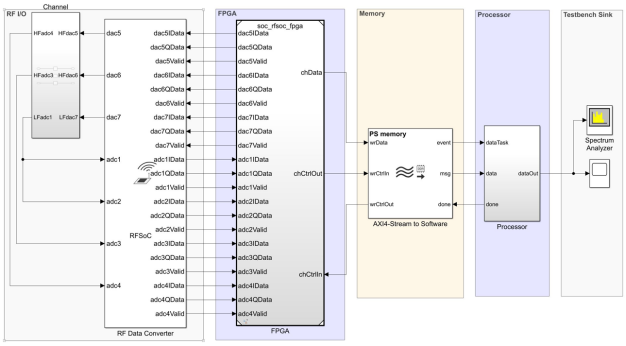

Figure 1: General RFSoC frame of the project provided by the SoC Matlab Blockset.

RFSoC Architecture and Components

The system under design is currently running with the user interface on a third-party computer. The RFSoC will then be interfaced to the EPICS control system. Several functions are supported by the control and visualization computer processor. For example, VNA functionality like S-parameter calculation as well as signal power measurement is performed based on data taken from the digitized forward, reflected, and pickup channels. The interface also considers channel scaling through attenuators to an acceptable ADC input power. At the same time, all output signals are currently not scaled and are equal to the full 14-bit DAC scale. One obstacle to sending data is the bandwidth of the bridge between the logic and processor, equal to the FPGA/ down sampling frequency, i.e., 122.88 MHz/128 = 960 kSps for the sum of all channels. The functions that will be inherent to the FPGA have also been highlighted. These are any feedback loops. At the moment a digital version of the PLL, Self-excited loop (SEL) control system, and adaptive feedforward control algorithm to reduce the influence of microphonics interference by means of a piezo actuator are in development and waiting to be tested in HoBiCaT.

Self-excited Loop Implementation by the RFSoC

The SEL [3] was first simulated in Simulink. The initial conditions are as follows:

1. The reference frequency fc1 of 19.967 MHz is generated by a 31-bit numerical control oscillator (NCO). This provides a phase resolution of 0.1 Hz with respect to the sampling frequency fs of FPGA of 122.88 MHz. A minimum frequency change of 0.1 Hz corresponds in this case to the number 1.7476.
2. The model-based simulation does not consider the delays in the FPGA processing algorithm, or the

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limitations of the intermediate frequency generation circuitry performed by the NCO.

3. The real hardware model considers all the above aspects. Therefore, each frequency generation channel in the final design has 4 NCOs simultaneously generating 4 pairs of IQs. Time delays are also considered.

The overall performance of the SEL depends on the internal parameters, such as the PI controller proportional and integral coefficients, as well as the error parameters. The loop is unable to counteract the error above a certain frequency. On the Fig. 2 the block scheme of the project simulating the behavior of a resonator subject to a destabilizing process that deviates the resonant peak from the reference can be seen. One NCO simulates the reference. The sum of the modulating signal and the reference is fed to output NCO, which simulates the resonator. At the same time the phase error, scaled by the PI controller, is fed to the reference NCO, counteracting the error.

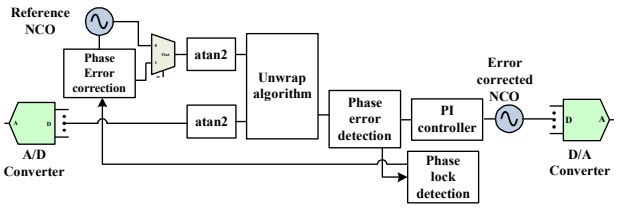

Figure 2: Current SEL implemented in ZCU111 RFSoC.

The SEL has a limit to its ability to follow the resonant peak, related to the response rate of the feedback loop. Therefore, Fig. 3 shows the error phase excitation with significant modulation of the resonant peak of the resonator of 1.2288 MHz and ability of SEL to process this modulation. The resolution bandwidth in this case is 1.875 kHz. A phase error is fed to the input of the PI controller, which is calculated as the difference between the phases of the corrected reference channel and the feedback channel. The specified phases are limited to a period of 2*pi. Therefore, the unwrap function extends the phase sign change from 2*pi through zero to a new period. The aggressiveness of the PI controller affects the allowable control error. The largest up to now predictable error occurs when the phase sign is changed. This can also be explained by the relatively low proportional gain available for digital PLL controllers with a damping factor of 0.9 [4].

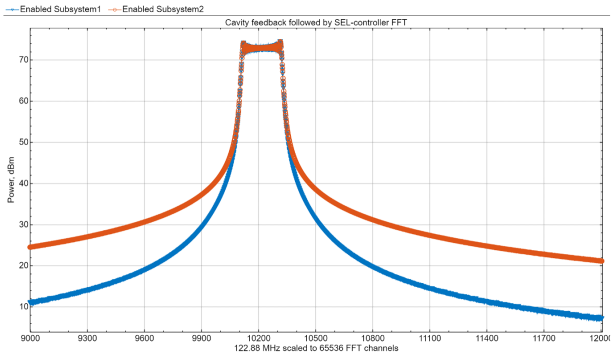

Figure 3: FFT of cavity feedback followed by the cavity reference corrected by the phase shifter.

The Xilinx RFSoC ZCU111 evaluation board was chosen as a prototype system to implement the SEL functionality. This choice determines the complexity of the firmware. Several ratios between board parameters must be observed:

- The ratio between the system reference frequency (PLL) and the sampling frequency must be an integer. The system reference is 7.68 MHz and the FPGA/AXI sample rate is 122.88 MHz.
- The sampling rate is 3932.16 MHz, which is the product of the AXI bus frequency of 122.88 MHz, interpolation mode 8 and the number of samples per clock cycle 4.

First, before starting SEL, a one-time scan of the resonator bandwidth is performed to search for resonant peaks using a convolution operation [5] with the band-pass information previously recorded with the vector analyzer. Once the reference peak frequency is established, the algorithm matches the resonator phase to the reference channel phase to an acceptable match. This is currently 36º, but can be increased by increasing the NCO resolution. After that the phase error correction block of the regulator is turned on at any perturbation of the resonator, leading to a shift of the resonant peak. The controller thus follows the resonator and compensates for the error. Now the algorithm has no amplitude limiter and in fact the DAC bit limit acts as such a limiter.

Adaptive Feedforward Control by RFSoC

The adaptive algorithm [2] in the Fig. 4, aims to compensate for microphonics interference with a piezo actuator. The phase error of the resonator, also called detuning, is compared at the LMS filter with the reference signal. That is, the delayed input signal of the resonator is matched to the detuning caused by it. The adaptive filter thus performs a system identification function. The found system coefficients at the filter output error close to zero are further translated into the "ideal" system model on the filter FIR. The sampling frequency of the LMS filter input signals corresponds to the piezo actuator response frequency, that is within units of kilohertz. To reconstruct the piezo perturbation signal as closely as possible by an unknown source, the observed piezo perturbation at the moment and previously recorded with the lock-in amplifier on the PLL are deconvolved. The inverted detuning signal is then sent to the piezo to counteract the unknown perturbation. The LMS filter has 2 tuning parameters, which must be chosen during the tests: the number of taps and the filter step [4].

Kalman Filter Control Implementation by RFSoC

The third microphonics interference minimization algorithm ported to the RFSoC platform was the Kalman observer-based algorithm in the Fig. 5. Previous modelling and development for mTCA equipment [6, 7] was focused on integrating multiple sources of microphonics interference into a single state-space matrix. This approach did not mathematically yield an acceptable level of system tracking. The result of this development was a finite state

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machine that minimized the DSP and on-board memory resources of the SIS8300L2 and FMC25 boards. However, this algorithm was never tested on the hardware due to the high degree of utilization of FPGA chips by existing firmware. RFSoC makes it possible to forget about resource limitations. Moreover, considering experiments on tracking individual perturbations, as well as the existing successful practice of tracking many objects with a Kalman filter, it was decided to change the model. Now the algorithm performs a periodic update of the frequency response of the resonator and searches for individual most distinguishable peaks of microphonic disturbances. When such a component is found, its quality factor and half-bandwidth are calculated. After that, the tracking of this microphonics interference is activated by a separate Kalman filter. Then the adaptive filter in the system identification mode, as in the previous case, mimics the real system exposed to external disturbances as accurately as possible. In the case of successful tethers of such an observer it will be combined with an adaptive feed forward controller.

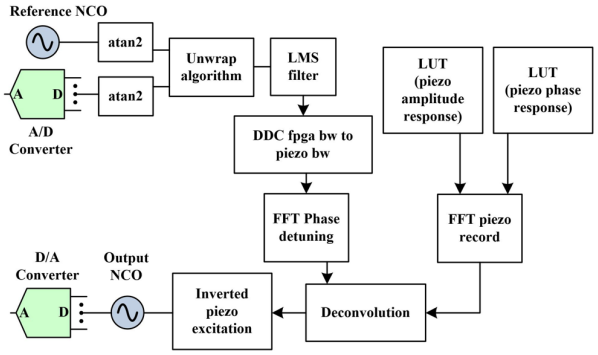

Figure 4: Adaptive feedforward regulator by RFSoC.

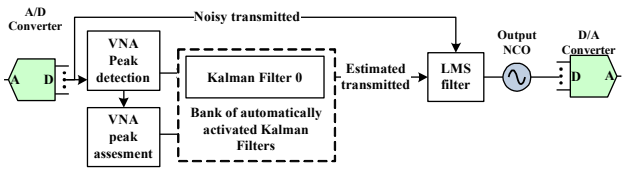

Figure 5: Current Kalman regulator implemented in ZCU111 RFSoC.

RFSoC ADC/DAC Performance

The ADC/DAC characteristics were obtained for the high frequency case i.e., with two channels of 1-4 GHz additional XM500 RFMC balun board, as the most suitable for Tesla cavity control. The ADC was tested in the following scheme: Signal generator, then the RFSoC ADC, then the internal RFSoC signal analyzer (see Table 1).

The sampling frequency Fs was set to 4096 Msps, the reference frequency generated was 1290 MHZ, the resolution bandwidth was set to 100 MHz for the reference and first harmonic, the source power step was 5 dBm from 0 to -15 dBm. The ADC channel under test is ADC224_T1_Ch0.

The high-frequency output of the DAC was measured according to the following scheme: RFSoC DAC generates a reference signal, then the output week signal is amplified by the Automatic Gain (AGC) Control amplifier with a gain of 55 dB and finally fed to an external signal analyzer. Other measurement settings are as follows: the DACs under test are DAC229_T1_Ch0/Ch1 at full 14-bit output, sampling frequency Fs = 6512 Msps, and reference frequency Fund = 1288.69 MHz.

Table 1: High frequency ADC channel characterization

Reference power at 1950 MHz in dBm	ADC channel measurement units	Reference tone detected by ADC	1st harmonic detected by ADC
0	dBFS	-12.69	-61.84
0	dBc	0	-49.14
-5	dBFS	-17.7	-66.33
-5	dBc	0	-48.63
-10	dBFS	-22.71	-71.12
-10	dBc	0	-48.41
-15	dBFS	-28.61	-73.68
-15	dBc	0	-45.07

For further work in HoBiCaT the following scheme was adjusted, considering the low level of DAC output signal: from the high-frequency output of DAC05/06 the signal comes to the Alto AGC amplifier with the gain of 20-30 dB, is limited by the limiter ZFLM-252 and, finally, comes to SSA. The first measurement with the maximum 14-bit output of DAC05 and 25 dB gain of the Alto amplifier yields 223 Watt of direct Tesla power, 4.5e-9 W of transmitted power, and 2.6e-3 MV/m of accelerating field at 30.9255 Eacc/sqrt coefficient for transmitted power.

CONCLUSION

RFSoC is a competitive control and instrumentation solution for laboratories with limited developer resources, but with a desire to develop their own scientific solutions. Despite the relatively small market, the RFSoC is already significantly supported by both low-level and high-level development tools from both chip manufacturers and third-party developers to reduce development time. Tests on the Tesla resonator have already begun and have revealed the first issues of the system that need to be corrected. Among them is the sensitivity of the synchronization circuit of the digital and analog circuits to phase jitter, which manifests itself in the rattle of the amplitude within 0.1 dB, as well as the low signal level, which does not correspond to the declared by the manufacturer. Soon, the algorithms will be provided with means for visualization and continuous recording of digitalized data of analog channels on the control computer. All developed algorithms are going to be tested soon and the results are going to be provided to the scientific community.

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