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A MTCA.4-BASED RESONANCE CONTROLLER FOR SUPERCONDUCTING CAVITIES

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Abstract

The growing interest in upgrading European XFEL to high duty cycle operation requires an adaptation of the current low-level RF system to the new machine specifications. In the current upgrade scenario, the principal change in the RF parameters will be the loaded quality factor (Q_L) of the superconducting cavities, which will increase from the current value of $4.6 \cdot 10^6$ to more than $5.3 \cdot 10^7$ to reduce the required RF power. As a result, the accelerating system will be an order of magnitude more sensitive to detuning disturbances, such as *Lorentz force detuning* or external microphonic vibrations. Therefore an MTCA.4-based chain to precisely measure the cavity RF signals, calculate the detuning error, generate a control signal and drive the piezoelectric tuner was developed both for single cavity and Vector Sum mode of operation. While the detuning measurement chain is implemented in programmable logic, the control algorithms are implemented on embedded processing systems of FPGA-enabled devices like DAMC-FMC25, DAMC-FMC1Z7IO, and DAMC-FMC2ZUP MTCA AMCs. This provides a flexible platform to develop resonance control algorithms. In this proceeding, the implemented architecture is discussed.

INTRODUCTION

For the European XFEL (EuXFEL) High Duty Cycle (HDC) upgrade, major modifications of the LLRF system will be needed on the hardware, firmware, and software levels. The motivation for such changes lies in the Loaded Quality factor (Q_L) value, which is going to be higher than $5.3 \cdot 10^7$. Such a high value of Q_L is required to limit the peak power consumption of each cavity to less than 6 kW when operating with full beam loading. As a consequence, the cavity half bandwidth ($f_{1/2}$) will be smaller than 12.3 Hz. At the same time, it will be required to drive the cavities at gradients up to $E_{max} = 20\,\mathrm{MVm}^{-1}$. Since for the TESLA cavities installed at EuXFEL, the Lorentz Force Detuning (LFD) coefficient (k_{LFD}) can be as low as $-1.6\,\mathrm{HzMV}^{-2}$, the ratio between the LFD and the half bandwidth will be

$$-\frac{k_{LFD}E_{max}^2}{f_{1/2}} \simeq 52. \quad (1)$$

It was shown that ponderomotive instabilities affect RF operations for ratios above 1.54 [1]. Additionally, the expected microphonics level in the EuXFEL tunnel is expected to be around $3 - 6$ Hz, roughly the same order of magnitude of the cavity bandwidth. Therefore, to compensate for these detuning effects, a resonance control loop is foreseen. A control chain was developed to pre-process the RF signals, compute the resonator bandwidth and detuning and to control the cavity piezoelectric tuner [2].

Due to cost optimization of the RF amplifiers, for the EuXFEL HDC upgrade, it might be necessary to switch part or all of the RF driving scheme from Vector Sum (VS) to single cavity.

Therefore, a compact and cost-effective LLRF solution has to be found to drive more than 800 cavities in single loop mode of operation.

HARDWARE CONFIGURATION

The choice of the LLRF control hardware for the HDC upgrade strongly depends on the high-power driving scheme. If the VS mode of operation will be used for the main LINAC, relatively low changes will be needed to the actual LLRF crates, except for upgrading the LLRF boards to their more recent version [3]. In this scenario, the controller board DAMC-TCK7 Advanced Mezzanine Cards (AMC) and the digitizer board SIS8300-L2 could be updated with DAMC-FMC2ZUP and SIS8300-KU unless at the time of the upgrade more advanced digitizers might be available [4–7]. Using more recent boards with integrated processors and more FPGA resources will be beneficial in developing CPU-based high-performance resonance controllers.

If single cavity control of the entire LINAC is decided, more significant changes will be needed. Here we present three possible schemes:

1. Two DAMC-FMC2ZUP controller boards are installed. These boards are equipped with eight-channel Vector Modulator (VM) Rear Transition Module (RTM) boards. Such a board has yet to be designed. Six SIS8300-KU with DoWn-Converters (DWC) RTMs are installed to provide the probe, forward and reflected RF signals. This solution allows to drive up to 16 cavities with a single MTCA.4 crate. The PZ16M box will be used to drive the piezoelectric tuners [8].

2. Each crate is equipped with eight SIS8300-KU AMCs with DWC8VM1 RTMs [9]. Since each board will be able to drive a single resonator, a MTCA.4 crate would be capable of managing up to 8 cavities. Two DAMC-FMC1Z7IO each with DRTM-PZT4 will be used to actuate the tuners [5, 10, 11]. The resonance control algorithms will run on the DAMC-FMC1Z7IO embedded processors.

3. As in scheme 2., the crate is equipped with eight SIS8300-KU. Instead of a pair of DAMC-FMC1Z7IO,

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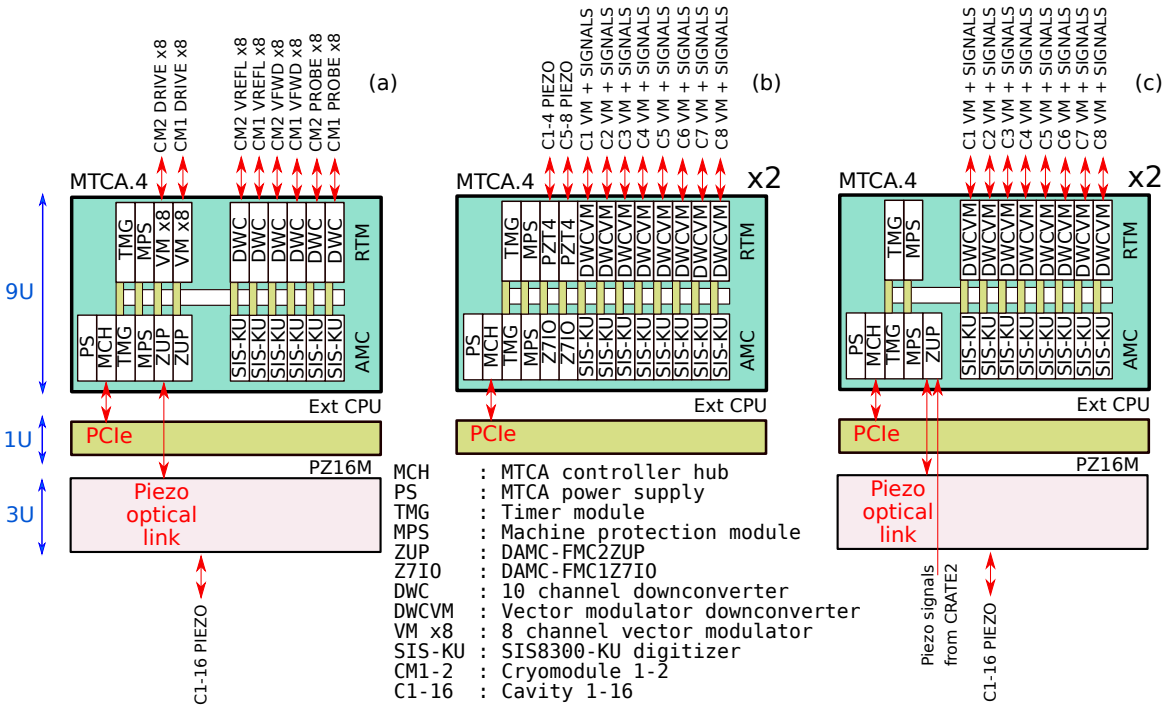

Figure 1: Crate organization for the scenario 1. (a), 2. (b), 3. (c). Note that a single crate for 1. manages up to 16 cavities, while for 2., 3. up to 8 cavities are managed per crate.

a single DAMC-FMC2ZUP will drive a PZ16M box. Two crates must be linked with an optical fiber link to use all 16 actuator channels available in a PZ16M box.

Fig. 1 shows the crate organization for the above schemes. An external rack-mounted edge server will be needed to run the control software in all three cases and will directly communicate with the MTCA.4 PCI-express (PCIe) bus through an optical fiber bridge [12]. The motivation for an external non-MTCA.4 computer unit is that for the above schemes, the requirement in computing power will be up to 16 times higher compared to the current EuXFEL configuration. At the time of writing, no known MTCA.4 AMC CPU would fulfill such a requirement [13].

The major advantage of scheme 1. is that there won't be the need of installing additional MTCA.4 crates in the tunnel or change the current RF cabling of EuXFEL. However, this scheme requires designing a new board with 8 VM channels will need to be designed.

Further cost analysis will be required to choose the most effective configuration for the upgrade.

CONTROL CHAIN

The LLRF control chain for the HDC upgrade requires the real-time estimation of detuning to drive the resonance controller. Additionally, the finite isolation of the directional coupler of the forward and reflected RF signal has to be corrected [14]. The current implementation for a single cavity controller is depicted in Fig. 2 and uses distinct AMC boards for field and resonance control. The detuning estimation is performed on the field control board (SIS8300-KU) with a sample rate of 140 kHz [15]. Once the calculation of the detuning is completed, the value is sent to the resonance controller board with a rate of 4.4 kHz through the point-to-point links of the MTCA.4 backplane, using the Low Latency Links (LLL) protocol. Since the LFD excitation is proportional to the cavity stored energy, the square value of the probe signal is also sent to the resonance controller. The RF signals sampling is performed at 9.028 MHz. Cascaded Integrator-Comb filters are used when a slower sample rate is needed. On the resonance controller board, a routine running on the embedded CPU is triggered every time new data arrives. Such a routine implements the resonance controller to drive the piezoelectric tuners. The advantage of using a CPU-based resonance controller is the ease of development and use of floating point arithmetic. Currently, the controller implements a Narrowband Active Noise Control (NANC) algorithm and an integrator [16, 17]. However, it is foreseen to implement an Iterative Learning Control-based (ILC) algorithm when operating in a long pulse mode of operation to compensate for transient LFD effects [18]. The generated control value is then passed to a tuner protection component that checks and cuts the signal slope and magnitude within a pre-established limit. Finally, the control value is converted by a DAC to an analog signal that drives the piezoelectric tuner.

The entire chain for a single cavity system is depicted in Fig. 2.

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Table 1: Specifications for the Processor Systems Analyzed in this Proceeding

Board/Platform	Processor type	Frequency (MHz)	Cores	DMIPS/core	Memory (MB)	Application
Xilinx FPGAs[19]	Microblaze	100-500	Depends on the FPGA configuration	131-655	Depends on the FPGA resources	realtime controller
DAMC-FMC25	PowerPC 440	400	1-2	889	256	realtime controller
DAMC-FMC17ZIO	ARM Cortex-A9	800	2	2000	1024	realtime controller control server
DAMC-FMC2ZUP	ARM Cortex-A53	1500	4	3450	4096	realtime controller control server
DAMC-FMC2ZUP	ARM Cortex-R9	600	2	1000	4096	realtime controller
AM 900/412 AMC[13]	Intel i7-3555LE	2500	2+2 virtual	9000	4096	control server
Example 1U external CPU[20]	Intel Xeon Gold 6321U	2400	24+24 virtual	13200	131072	control server

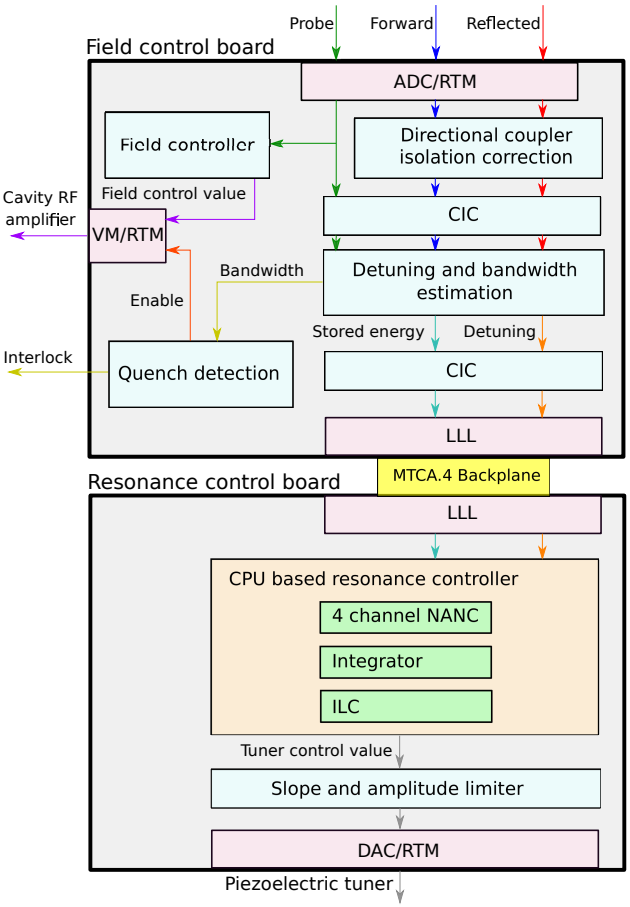

Figure 2: LLRF single cavity data flow chart. The FPGA components for the field and resonance control boards are depicted.

CONCLUSION

In this proceeding, different possibilities of the MTCA.4 LLRF controller architectures for the EuXFEL HDC upgrade are presented. The choice of the boards was made to maximize the use of Commercial Off-the-Shelf (COTS) components and the number of cavities managed by a single MTCA.4 crate. Additionally, the architectural decisions are influenced by the requirement to use a resonance feedback controller. The actual controller is implemented on top of DAMC-FMC25 [21]. The board uses a Xilinx Virtex 5 Field Programmable Gate Array (FPGA) with an integrated dual-issue out-of-order PowerPC integrated processor. The processor runs at 400 MHz. Since past experiments of resonance control with integrated processors used a Microblaze soft architecture clocked at 100 MHz, the DAMC-FMC25 embedded CPU is evaluated as sufficient to control a single SRF cavity. Once the board support package for DAMC-FMC17ZIO and DAMC-FMC2ZUP is completed, the resonance controller will be ported to these MTCA.4 AMCs. Since the two boards, respectively, are equipped with a dual-core ARM Cortex-A9 clocked at 800 MHz and a quad-core ARM Cortex-A53 clocked at 1.5 GHz, a single integrated processor could manage multiple cavities. The additional computing capacity will also be used to experiment with more time-demanding resonance control algorithms. Table 1 presents a summary of the specifications for the discussed computing systems.

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