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DESIGN CONSIDERATIONS FOR CERN´S SECOND-GENERATION BEAM INTERLOCK SYSTEM

I. Romera*, S. Bolton, A. Colinet, J. Guasch-Martinez, C. Martin,
T. Podzorny, R. Secondo, J. Uythoven, CERN, Geneva, Switzerland

Abstract

The Beam Interlock System (BIS) is the backbone of the machine protection system throughout the accelerator complex at CERN, including the LHC. The present BIS needs to be upgraded to ensure the required level of dependability and maintainability for the lifetime of the HL-LHC, which is planned to become operational in 2029. The present BIS, designed more than 15 years ago, has proven its reliability but is becoming obsolete and can no longer be deployed in new installations. In this paper we present the progress towards the deployment of a new beam interlocking solution for the CERN accelerators, including several identified new requirements for the HL-LHC. The prototypes of the main interlock boards have been produced and the first tests to validate their functionality were conducted and are described in detail.

INTRODUCTION

The BIS takes User Permit signals given by various user systems and converts them into Beam Permit signals used by the injection, extraction or beam dumping systems to permit or inhibit beam operation. The BIS can be configured in two different architectures: ring (to protect circular machines, such as the SPS or LHC) and tree (to protect the injection and extraction elements, such as the SPS to LHC transfer lines). In circular machines, a transition from beam permit to beam inhibit triggers the extraction pulsed magnets and causes the beam to be deposited onto a graphite block. In the transfer lines, however, the loss of the beam permit inhibits the injection or extraction of the particle beam [1].

The various instances of the BIS deployed in the CERN accelerator complex (i.e. LINAC4, PSB Extraction, SPS injection, SPS, SPS-to-LHC Transfer Lines and LHC) have proven its reliability and availability during more than 15 years in operation [2]. Nevertheless, the foreseen upgrade of the LHC (HL-LHC), aiming to increase the instantaneous luminosity by a factor 5 compared to the LHC, requires a new BIS which adapts to the new interlocking requirements, see Table 1. In addition, the consolidation of all interlock instances deployed in the injectors aims at enhancing their maintainability.

MAIN DESIGN CONSIDERATIONS

The second-generation BIS (BIS v2) is designed for safety and reliability. Dependability analysis was carried out as an integral part of the system design, with Failure-Mode Analysis (FMECA) providing further insight to the electronics design. The reliability targets set for the new system are maintained: <1 false dump per year and <1 blind failure every 1,000 years [3].

A fundamental aspect to the safety is the redundancy, which has been implemented all the way from the User Systems to the BIS. In addition, redundant power supplies are used to meet the required availability. Another key design consideration was the possibility to test the system from end-to-end in a controlled way, by exploiting this redundancy. Furthermore, flexibility was an important aspect on the design to allow the deployment of the system in different machines with minimum modifications, without compromising safety.

PROTOTYPES

The design of the prototype boards, which started during the Long Shutdown 2 (LS2) in 2020, is advancing well and functional prototypes of the main boards were successfully tested in laboratory conditions (see Fig. 1). All boards designed for BIS v2 share the same technologies, re-using as much as possible proven and reliable circuits across boards. In addition, all boards are equipped with similar diagnostics features: ADCs (monitoring of voltages and currents), EEPROM (providing Unique-ID and up-time counters) and temperature sensors, among others.

Figure 1: CIBM, CIBG, CIBDS and CIBFI prototype boards.

Manager Board - CIBM

The Manager (CIBM) board is responsible for 'AND'-ing the User Permit signals coming from the User Interfaces and generating a Local Beam Permit which is TRUE when all user systems are ready for beam. While in BIS v1 the redundancy of the critical functions is managed by a single board (i.e. implemented in two CPLDs), in BIS v2 it was decided to enhance safety by having redundant boards [4]. In turn, each board is also responsible of the non-critical operations (i.e. monitoring and test routines) as compared to the CIBT board in BIS v1. Thanks to the new redundant

* iromerar@cern.ch

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Table 1: Comparison Between BIS v1 and BIS v2

Requirement	BIS v1	BIS v2	Description
More User Permits	14	20	Greater flexibility, interlock´s concentrator for multiple user equipment
Greater redundancy in critical paths	1 CIBM for A & B	1 CIBM for A, 1 CIBM for B	Increased reliability and reduced probability common-mode failure
Enhanced optical communications	ELED-based	SFP-based	COTS, hot-plug capability, long distance, full diagnostics
Reduced latency to dump other beam	2 turns	1 turn	Minimise risks of missing beam-beam kick
Better on-board peripherals	UART	ADC, Temperature, EEPROM, Up-time counters	Lifetime, loading factors, easier maintenance
Maintain or improve reliability	No-blind failures, MTBF>1000 years	No-blind failures, MTBF>1000 years	Improved reliability, remote testing and monitoring
Higher radiation tolerance	160 Gy TID	>380 Gy TID	Reinforced radiation tolerance

architecture, the new CIBM is able to handle up to 20 User Permits, whereas only 14 can be managed by the actual BIS v1. Another important difference with respect to the present CIBM is the addition of a FALSE frequency to signal the removal of the Beam Permit [5]. This solution has a twofold purpose: 1) to remove unwanted oscillations when transitioning from a TRUE frequency signal to a constant DC value and 2) to provide additional information on the integrity of the optical communication network (i.e. detection of broken loops). An external oscillator is responsible for the generation of the 920 kHz FALSE frequency, which is the same for the two redundant Beam Permit loops.

Frequency Generator Board - CIBG

The Frequency Generator (CIBG) installed at the start of the loop is responsible for the creation of the two Beam Permit frequencies, which are then propagated across CIBM nodes where they are either retransmitted or replaced by a FALSE frequency depending on the status of their Local Beam Permit signals. Given that the generation of Beam Permit frequencies only affects availability, the redundancy is implemented by two FPGAs on the same board [6].

User Interface Boards

User Systems are connected to the BIS via a User Interface. This interface is used to connect to the numerous types of User Systems having different hardware platforms and operating voltages. Depending on the distance between the User Interface and the BIS, two different hardware equipment exist: the CIBU, which is limited to around 1200 m as RS485 is specified for cables of this length, and the CIBF, which extends the communication range to 10 km thanks to the use of fibre optics. In both cases, the interface between the User System and the User Interface is made by current loops. Also, a new optical interface (CIBFX) is provided to facilitate practical and cost-effective connection to the BIS where multiple user equipment devices are installed in the proximity.

CIBU The User Interface (CIBU) board has been re-engineered to improve its maintainability, availability and tolerance to radiation, while maintaining the same interfaces with the User Systems as BIS v1 [7]. The board is now equipped with a Microchip Igloo 2 Flash FPGA, where monitoring functions are implemented, featuring a higher immunity to Single Event Upsets (SEU), see CIBU Radiation Testing section below. In addition, the board is equipped with an ADC to remotely monitor the consumption of the redundant power supplies and the current of the User Permit inputs, allowing to detect any possible degradation over time and to trigger a preventive maintenance.

CIBF The Fibre Optic User Interface (CIBF) benefits from the same diagnostic capabilities as the CIBU and hosts a mezzanine board (CIBSFP) with three SFP optical transceivers that serve to convert electrical signals to optical, and vice-versa. The CIBF is equipped with 3 Igloo 2 FPGAs, two of them to handle the critical functions and the other to manage the monitoring and testing features. The communication between the CIBF and the BIS is ensured by 4 fibre optic links that are responsible for the transmission of the redundant User Permits, the Monitor and the Test channels.

CIBFX A 10-input Fibre Optic User Interface (CIBFX) is proposed to interface multiple user equipment connections in a constrained area. This new board will be typically used to interlock power converters located in the same building. Given that the distance between the user equipment and the CIBFX can be of up to 100 m, RS485 differential signaling was chosen for these links as it is better suited for harsh industrial environments and is specified for operation with long cable lengths. The CIBFX uses the same mezzanine board (CIBSFP) and the same communication protocol as the CIBF for the optical communication with the BIS v2 crate.

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Optical User Interface Board - CIBFI

The Fibre Optic Interface (CIBFI) is a new VME board responsible for interfacing Fibre Optic User Interfaces (i.e. either CIBF or CIBFX). Given that a BIS v2 chassis supports up to 4 CIBFI boards and that a CIBFI board can interface up to 3 CIBF/X, 12 Fibre Optic Interfaces could be interfaced by a single BIC. The interface between the CIBFI boards and the CIBM is made through the extension boards and the rear panel. The CIBFI board reduces the number of interface boards required compared to BIS v1 [8].

Redundant Trigger Board - CIBDS

The Redundant Trigger board (CIBDS) is presently used to issue a redundant dump request to the LHC Beam Dumping system (LBDS) in case of failures in the primary link between the BIS and the Trigger Synchronisation Unit (TSU) of the kicker magnet system. In BIS v2, the role of this board has been extended to reduce the latency in dumping both beams, thereby minimising the beam losses due to the missing beam-beam kick. The linking of the Beam Permit Loops is now automatically done when the intensity reaches a pre-defined threshold. For this purpose, the Safe Machine Parameters v2 (SMP) will publish a Link Mode Flag, used by the CIBDS [9].

TESTING AND VALIDATION

Continuous Integration and Deployment - CI/CD

Continuous integration tests based on GitLab's CI/CD feature have been implemented to ensure the quality and reliability of the HDL firmware. A set of tasks are automatically triggered at every commit, including linter checks, unit tests, synthesis and bitstream generation. Automated hardware tests will be included in the CI/CD pipeline in the near future.

Hardware and Functional Test Benches

Every BIS v2 board will have a dedicated hardware test bench to verify the hardware functionality after fabrication and assembly. Another test bench is foreseen to test the functional behaviour. So far, two hardware test benches were designed, one for the CIBU and the other for the CIBM. In addition, a dedicated test platform was successfully set up in the laboratory to perform automated functional tests (see Fig. 2).

CIBU Radiation Hardness Assurance

The CIBU is the only hardware board of the BIS that is subject to operate in radioactive environments, therefore several irradiation campaigns were launched at the Paul Scherer Institute (PSI) and at CERN between June 2020 and April 2022. The purpose of these tests was to assess the cumulative radiation effects and the impact of Single Event Effects (SEE) on the CIBU electronics. The target radiation levels used for the qualification of the CIBU were the ones expected in the RRs (Level 1) areas in IR1 and IR5 [10].

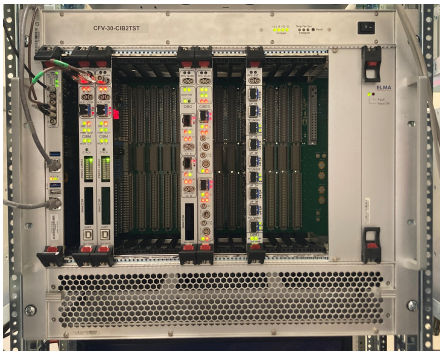

Figure 2: Test platform with BIS v2 prototypes.

Every single component of the CIBU was individually irradiated at PSI using a 200 MeV proton beam up to a Total Ionising Dose (TID) of 500 Gy and a Displacement Damage Equivalent Fluence (DDEF) of 8.42×10^{11} 1MeVneq.cm^{-2}. These initial tests served to discard three components: 1) the INA240A1D (i.e. an instrumentation amplifier), 2) the TPS3808 (i.e. a power-on reset generator) that suffered from Single Event Latchups (SEL) and 3) the LT3083EDF (i.e. a voltage regulator) that did not recover after power cycles.

Following the component-level qualification at PSI, two additional test campaigns were performed at CERN using the CHARM facility, to qualify the CIBU electronics at system-level. A test setup was designed and deployed to fully monitor the behaviour of both critical and monitoring paths, as well as the power consumption. Tests at CHARM were successful and the two tested CIBU did not show any sign of degradation up to 383 Gy of TID. A total HeH fluence of 1.57×10^{12} cm^{-2} and 3.3×10^{12} 1MeVneq.cm^{-2} DDEF was reached in each of the runs without any evidence of SELs nor any other destructive SEEs. In terms of availability, 27 false dump requests were triggered (i.e. due to the sensitivity of the FOD060L optocoupler to Single Event Transients - SETs) that can be easily mitigated by adding a filter on the CIBM [11].

TIMELINE AND OUTLOOK

The development of the second generation BIS started in 2020 and is progressing well. Prototypes of the main boards are working under laboratory conditions. The CIBFX prototype is currently being designed and the rear panel prototype being assembled. In Q3 2023, the development of the last board (the actuator board CIBAB) will be launched. The next goals for the system development are the mass production, that will start in Q3 2023 for the CIBU, and the installation of the equipment in the CERN accelerator complex. The full deployment of the new BIS in the SPS, SPS North Experimental Area [12] and LHC is foreseen during the LS3, i.e. starting in 2026. As the new CIBUs are compatible with the present BIS v1 system, they will be installed in the SPS and the SPS-to-LHC Transfer Lines during the Year End Technical Stops (YETS) 2023/24 and 2024/25 to reduce the workload in LS3 as much as possible.

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