JLAB LLRF 3.0 Development and Tests*

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Abstract

The JLAB LLRF 3.0 system is being developed to replace legacy LLRF systems in the CEBAF accelerator. The new design builds upon 25 years of design and operational RF control experience (digital and analog), and our recent collaboration in the design of the LCLSII LLRF system. The new cavity control algorithm is a fully functional phase and amplitude locked Self Excited Loop (SEL). This paper discusses the progress of the LLRF 3.0 hardware design, FPGA firmware development, User Datagram Protocol (UDP) operation, and recent system tests on the CEBAF Booster cryomodule without and with a beam.

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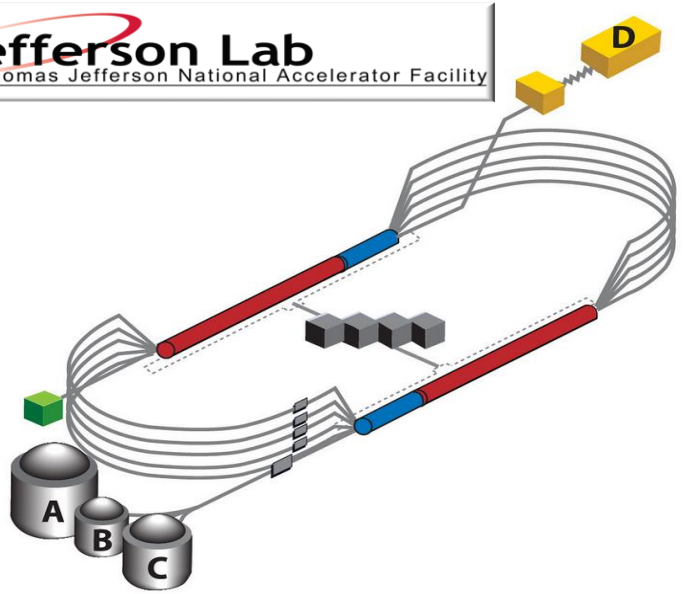
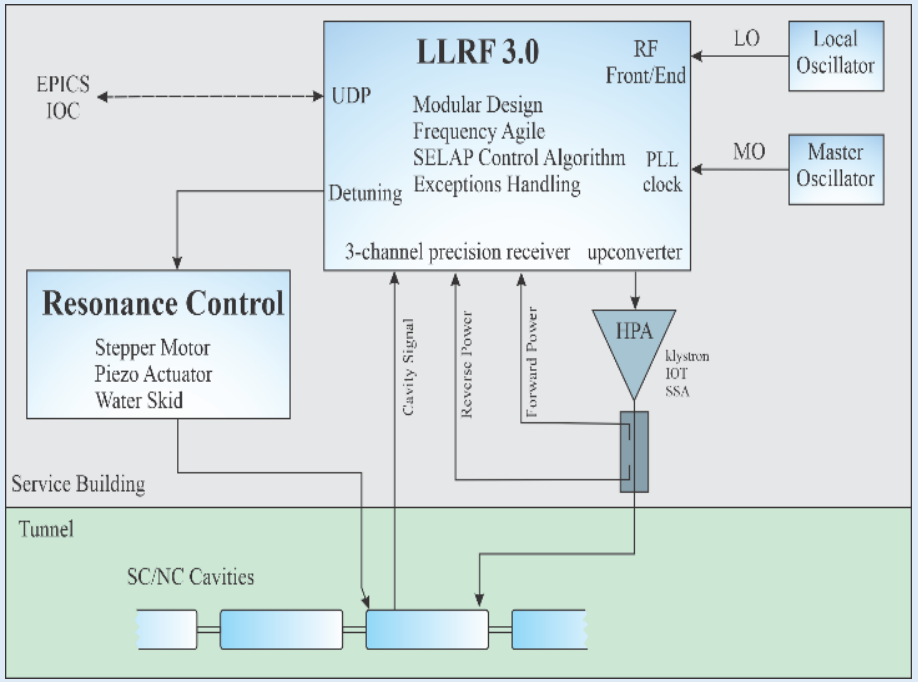


INTRODUCTION

The CEBAF Accelerator at Jefferson Lab provides electron beams to four different physics (experimental) halls at energy up to 12 GeV. This is accomplished using two linacs with over 400 superconducting cavities in 53 cryomodules. The linacs are connected with recirculating arcs. Three of the experimental halls can receive up to five passes and a fourth can receive 5.5 passes [1]. The overall delivered dp/p rms. energy spread is 5x10-5 at currents up to 400 uA (cw).

As part of the CEBAF improvement plan, a new modified cryomodule, C75, has been developed using the existing older cryomodule[1]. The new cryomodule cavity's Q_{ext} is 1.5 x 10^7 and has a Q_0 of 8 x 10^9. In addition to the cryomodule upgrade, plan also calls for upgrading the RF zones with new LLRF systems (LLRF 3.0), which will replace the old analog LLRF (LLRF 1.0) designed in late 1980s. Every cavity is powered and controlled individually similar to the older RF systems. The cavity amplitude and phase field stability remain unchanged and must be smaller than 0.04% and 0.5 deg rms. respectively, measured for frequencies > 1 Hz.



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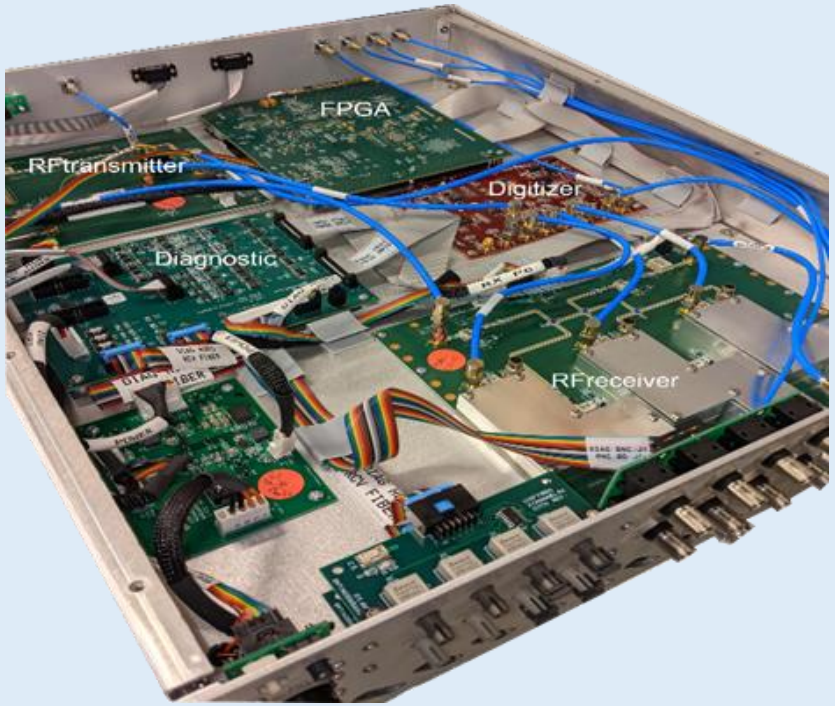
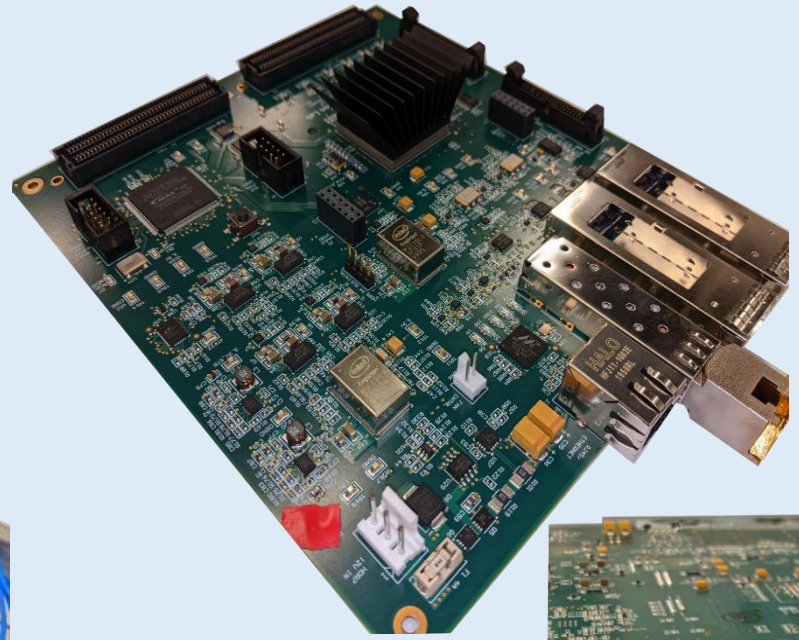
Hardware Description

RF Transceiver

There are three high frequency receiver channels (1497 MHz) and one high frequency transmitter channel (1497 MHz). RF receiver and transmitter use heterodyning in double balanced, level 13 frequency mixer. RF receiver channels are designed to provide very high channel to channel isolation (>90 dB). RF receiver board generates 70 MHz IF (intermediate frequency) signals after heterodyning for the fast Digitizer ADC inputs.

RF transmitter board uses 70 MHz IF signal from the Digitizer DAC output to generate 1497 MHz signal.



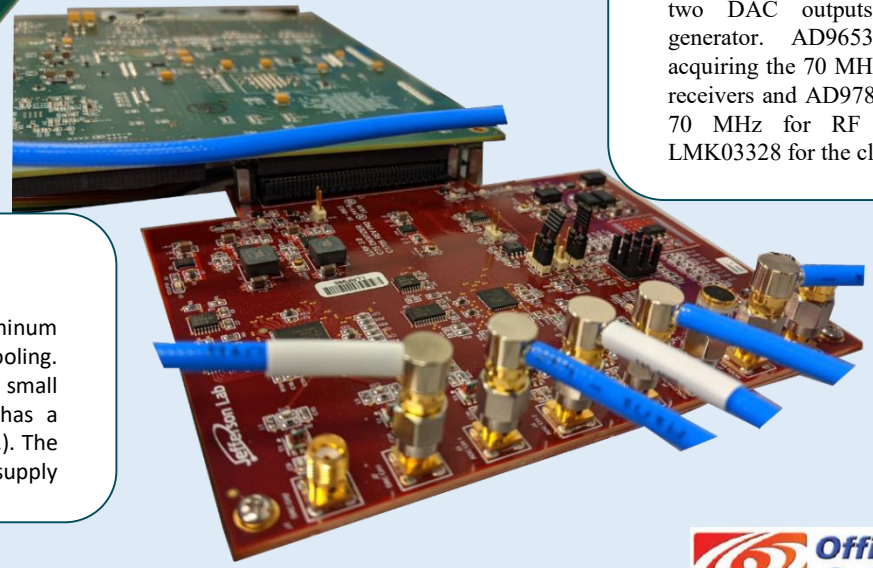


FPGA Board

FPGA board is designed based on Intel Cyclone 10GX 672 pin FPGA. This board uses a MAX10 FPGA for power sequencing and monitoring. This board is a dual LPC FMC carrier. This FPGA is available in four different sizes for resources (85k Logic Elements, 105k, 150k and 220k). This board is compatible with three of the four mentioned models (105k, 150k, and 220k). It is flexible in this sense that user can choose one of the three options at the time of assembly without changing the design. Cyclone 10GX FPGA has ten high speed transceivers. Eight out of the ten transceivers are routed to 2xQSFP (Quad small form-factor pluggable transceiver) connectors. Other two channels are routed to 1xSFP and Marvell gigabit Ethernet PHY.

Fast Digitizer

Digitizer has four inputs to the ADC, two DAC outputs and a clock generator. AD9653 is used for acquiring the 70 MHz inputs from RF receivers and AD9781 to generate the 70 MHz for RF transmitter and LMK03328 for the clock generator.



Chassis Design

All components are placed on a thick aluminum plate in order to provide adequate thermal cooling. Air flow is induced below the plate using a small “PC” chassis fan. In addition, the system has a diagnostic board (slow ADC, DAC, TTL I/O etc.). The chassis is powered using external DC power supply to limit the power supply induced noise.

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Control Algorithm

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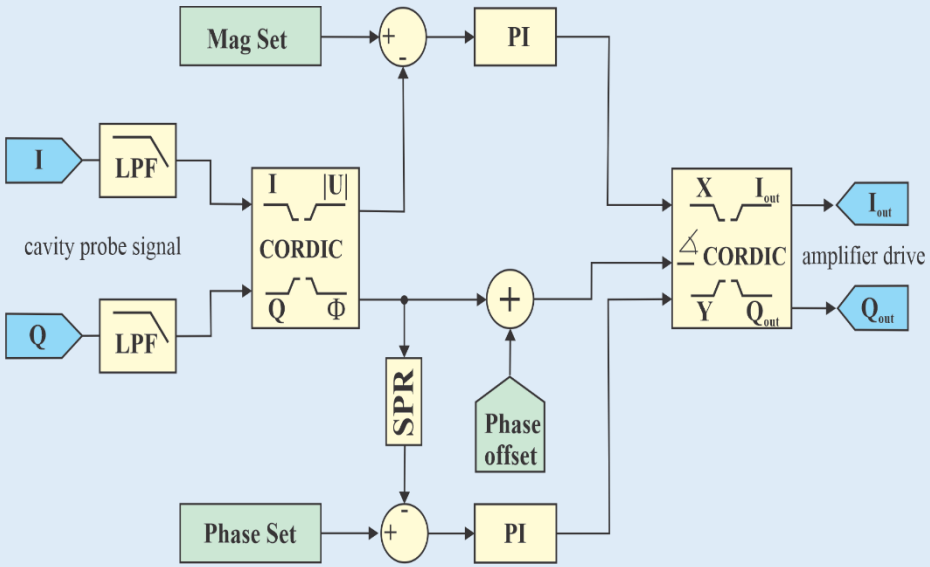
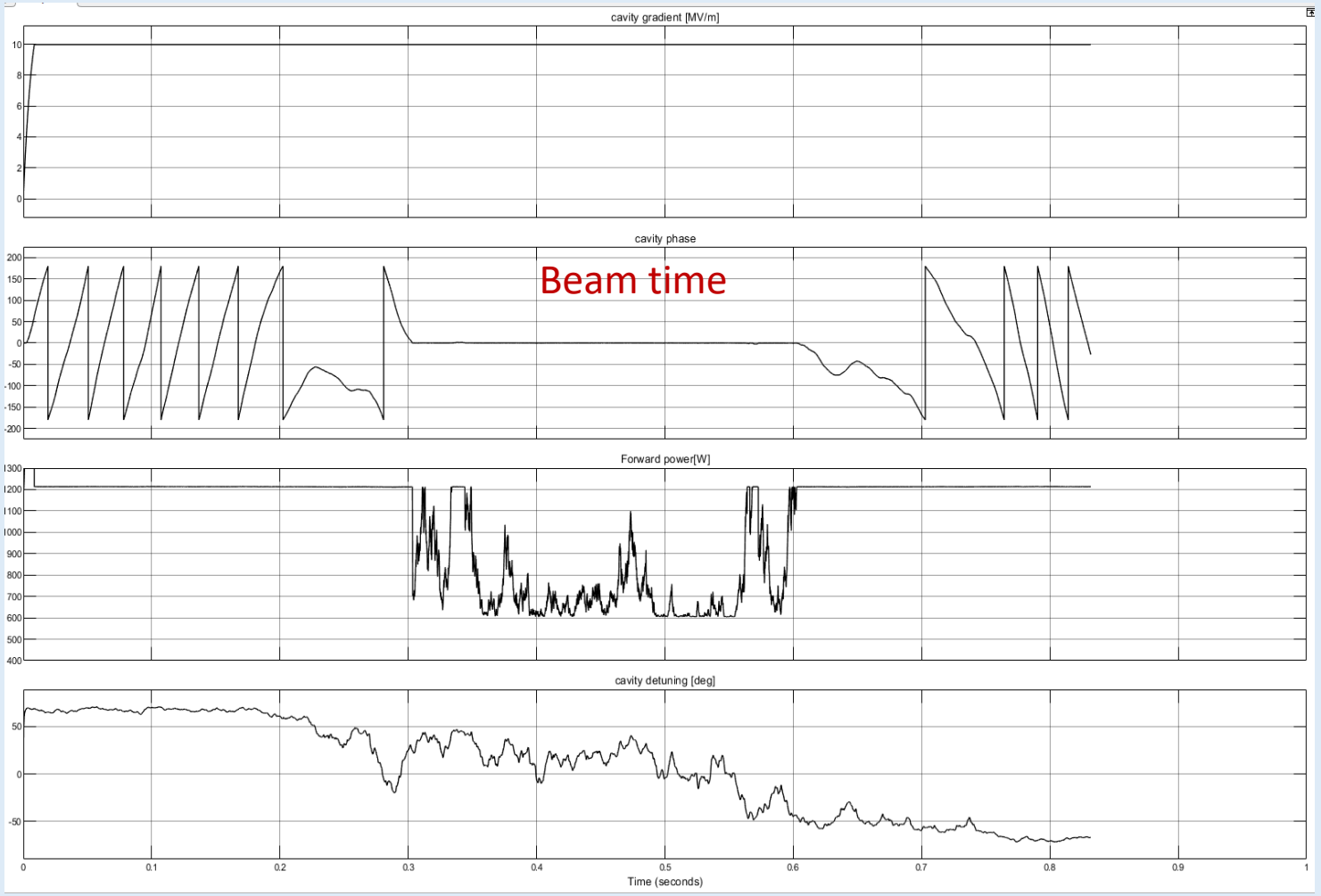
The control algorithm is based on digital Self Excited Loop concept [3,4,5] and extended by an Amplitude and Phase Lock feature, that replaces an analog GDR (Genera-tor Driven Resonator) based system. To distinguish this from GDR topology, we use the name SELAP (SEL with amplitude and phase locked). Figure below shows block diagram of this algorithm, first developed for LCLS-II LLRF project [5]. At JLAB we developed full (cavity +SELAP controller) Matlab model to better understand dynamic behavior of this topology, followed by VHDL firmware.

As one can see when magnitude PI controller output is constant and phase PI controller output equals 0, system is in free running SEL mode. After applying magnitude feedback, amplitude is locked (stabilized) although system is still in SEL mode. This mode (called SELA) helps with compensating small amplitude modulation caused by SEL mode imperfections. Once phase loop is closed (SELAP) system will compensate any cavity detuning by adding offset vector





"Beam time" shows RF operation when cavity detuning can be compensated by available RF power (Forward power is not saturated). Otherwise the system naturally transitions into SEL mode to maintain steady gradient.

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LLRF testing on Upgrade Injector Test Facility (UITF)

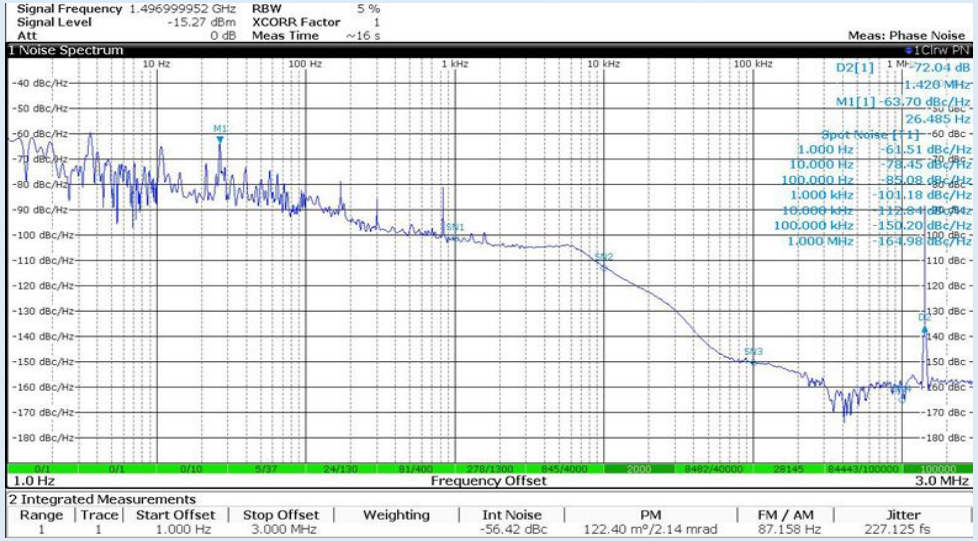
Before installing the new LLRF system in the CEBAF accelerator, the system was tested on a cryomodule in the Upgrade Injector Test Facility (UITF). The system was tested on a 7-cell SC cavity with external Q of 9×10^6 ($^1/_2$ bandwidth=78 Hz). The most anticipated part of the test was to run cavity in SELAP mode.

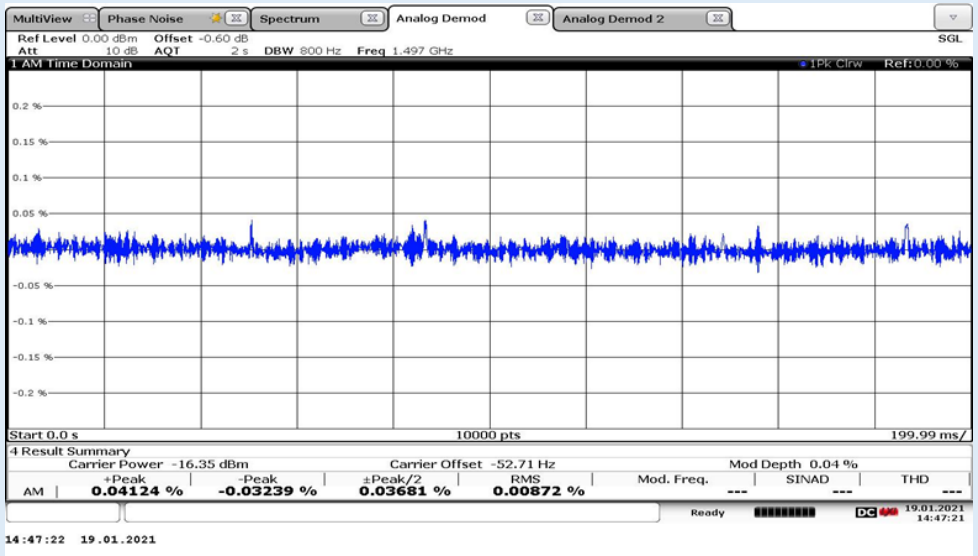
UITF Cryomodule, 7-cell SC cavity

Field Regulation:

Phase noise: 230 fs/ 123 mdeg

Amplitude AC component: < 0.01%





Conclusion

New LLRF system has been designed, built and successfully tested on SC cavity with beam. The design builds upon our own experience as well as our collaboration on LCLS-II LLRF project. The performance of the LLRF system represents the state-of-the-art in engineering. The modular architecture can easily accommodate new operational frequencies as needed in CEBAF.

The new firmware greatly improves superconducting cavity operability. Recovery from an RF trip is instant (once conditions causing trip have been resolved) and does not require any human interaction. The new system surpasses cavity field control requirements.

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[6] Larry Doolittle, private communication

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