ISBN: 978-3-95450-208-0 doi:10.18429/JACoW-IPAC2019-WEPGW092

NANOSECOND-LATENCY SUB-MICRON RESOLUTION STRIPLINE BEAM POSITION MONITOR SIGNAL PROCESSOR FOR CLIC

D.R. Bett, P.N. Burrows, C. Perry, R. Ramjiawan, John Adams Institute, Oxford, UK
G.B. Christian, Diamond Light Source, Didcot, UK

Abstract

A high-resolution, low-latency stripline beam position monitor (BPM) signal processor has been developed for use in an intra-train feedback system for the Compact Linear Collider (CLIC). The processor was designed to have extremely low latency of order nanoseconds and a target position resolution of order 1 micron. The processor consists of a pair of diodes to form the difference and sum of a pair of stripline BPM inputs with microstrip filters to reduce out-of-band noise. The assembled prototype was optimized for use with the electron beam in the extraction line of the Accelerator Test Facility at the High Energy Accelerator Research Organization (KEK) in Japan but the underlying design is readily scaleable to a higher frequency response relevant for CLIC. A latency of 3 ns was measured in a testbench setup. We report the results of performance tests with beam in which the position resolution was measured to be c. 325 nm.

INTRODUCTION

In order to maintain the CLIC luminosity to within a few percent of the design value, intra-train feedback is required to provide sub-nanometre beam stabilisation [1]. For CLIC bunch trains of length 156–176 ns [2], the system latency determines how many iterations of feedback are possible within a single train and consequently the luminosity recovery achievable with intra-train feedback [3].

Particular beam stability challenges include slow drifts, from sources such as thermal drifts, and higher-frequency disturbances, including facilities noise and ground motion [1]. Relative motion of the final doublet (FD) corresponds one-to-one to the displacement of the beam at the interaction point (IP) and an intra-train feedback system must be able to mitigate this effect.

Pulse-by-pulse feedback could mitigate lower frequency disturbances but would be unable to correct motion at frequencies above the train repetition rate. As $\sigma_y/\sigma_x = 1/40$ the luminosity is most sensitive to vertical offsets and, consequently, only feedback in the vertical plane will be considered here.

CLIC Feedback System

A stripline BPM processor has been designed for use in the CLIC IP feedback system [4], shown in Fig. 1. One primary requirement is that it must be very low latency in order to facilitate intra-train feedback on CLIC trains with a bunch separation of 0.5 ns. The processor must also be radiation-hard and be able to operate in a high magnetic field, prohibiting the use of ferrites in the design. Finally, the processor should be simple, reliable and with at least micron-level resolution.

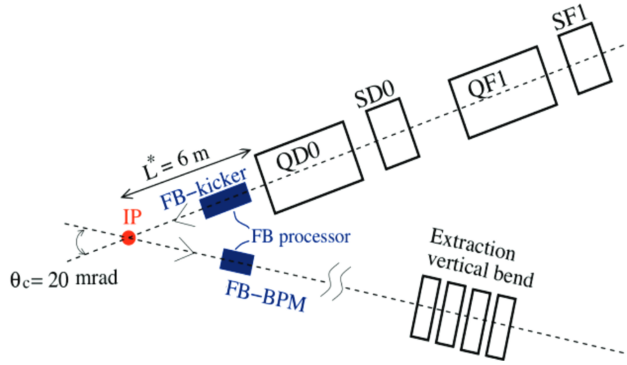

Figure 1: CLIC interaction region showing the IP feedback (FB) kicker, stripline BPM and FB processor [1].

The CLIC IP feedback system (Fig. 1) comprises a BPM and associated processor to measure the deflected beam after interaction and a kicker and amplifier upstream of the IP for beam correction. The beam measurement and corrections are applied to opposing beams so as to reduce the latency from signal propagation.

Accelerator Test Facility, ATF2

The prototype processor was tested at the Accelerator Test Facility, ATF2 [5] (KEK, Japan) in the FONT extraction-line feedback system, depicted in Fig. 2. The processor was implemented on stripline BPM P1 [6]. The charge at the ATF2 (~1 nC) is comparable to the CLIC bunch charges of 1.1 nC and 0.6 nC, for the 0.5 TeV and 3 TeV baseline designs, respectively [1]. The other BPMs, P2 and P3, had conventional FONT processors as described in [6]. The output from the processors were digitised on FONT5A boards as detailed in [7].

A key difference between ATF2 and CLIC operation is the number of bunches; the ATF2 was configured for trains of single bunches compared with CLIC trains of 354 and 312 bunches for the 0.5 TeV and 3 TeV designs, respectively [4]. Single bunch measurements are more challenging and so problems are not expected when scaling the prototype to be suitable for CLIC. The processor was tested on stripline BPM outputs that peak at 700 MHz, compared with the CLIC bunch repetition frequency of 2 GHz. The processors were designed so as to be scaleable to the higher-frequency CLIC signals.

ISBN: 978-3-95450-208-0 doi:10.18429/JACoW-IPAC2019-WEPGW092

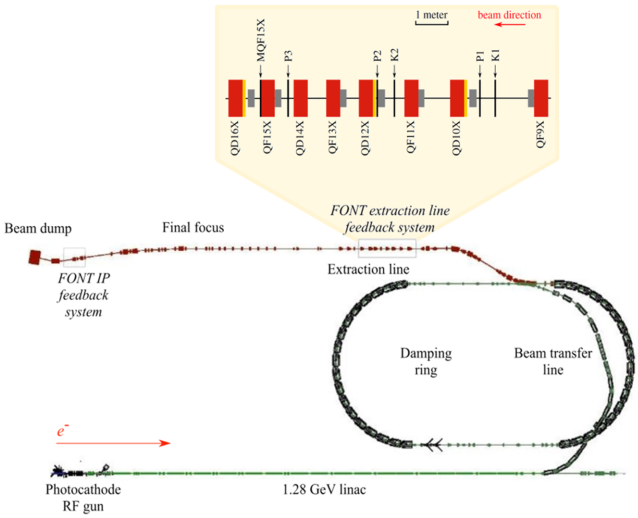

Figure 2: Schematic of the ATF2 with the FONT extraction-line feedback system highlighted, showing BPMs P1, P2 and P3 and kickers K1 and K2 [8].

FONT EXTRACTION LINE SYSTEM

Stripline BPM

The stripline BPMs in the ATF2 extraction-line comprise two electrodes of length 120 mm and separation 24 mm, mounted on the inside of the beam pipe [6]. The signals V_T and V_B from the top and bottom electrodes of the stripline BPM respectively can be written as [9]

$$V_T(t) \propto \left(1 + \frac{2y}{R}\right)\rho\frac{dq}{dt}, \quad V_B(t) \propto \left(1 - \frac{2y}{R}\right)\rho\frac{dq}{dt}, \qquad (1)$$

where y is the vertical position of the beam relative to the BPM's electrical centre, q is the charge, R is the BPM inner radius and ρ is the impedance of the electronics. Sum (V_Σ) and difference (V_Δ) signals can be constructed as

$$\begin{aligned} V_\Sigma(t) &= g_\Sigma(V_T(t) + V_B(t)) \propto 2g_\Sigma\rho\frac{dq}{dt}, \\ V_\Delta(t) &= g_\Delta(V_T(t) - V_B(t)) \propto 4g_\Delta\rho\frac{y}{R}\frac{dq}{dt}, \end{aligned} \qquad (2)$$

where g_Σ and g_Δ are the gain factors of the respective signals. The beam position can be determined from the 'difference over sum' signal, $V_\Delta/V_\Sigma = ky$, where k is the BPM position calibration constant.

Prototype Processor

The prototype processor, illustrated in Fig. 3, uses diodes to measure the signal amplitude from the stripline BPM electrodes. Microstrip 1.1 GHz low-pass filters (LPFs) before the diode were used to smooth the sharp peaks of the stripline signals, so as not to damage the diodes. 360 MHz LPFs on the output of the diode signal serve to reduce the AC components that would be introduced by the CLIC high-frequency bunch repetition rate. The processor outputs are sent through two ZX60-4016E amplifiers.

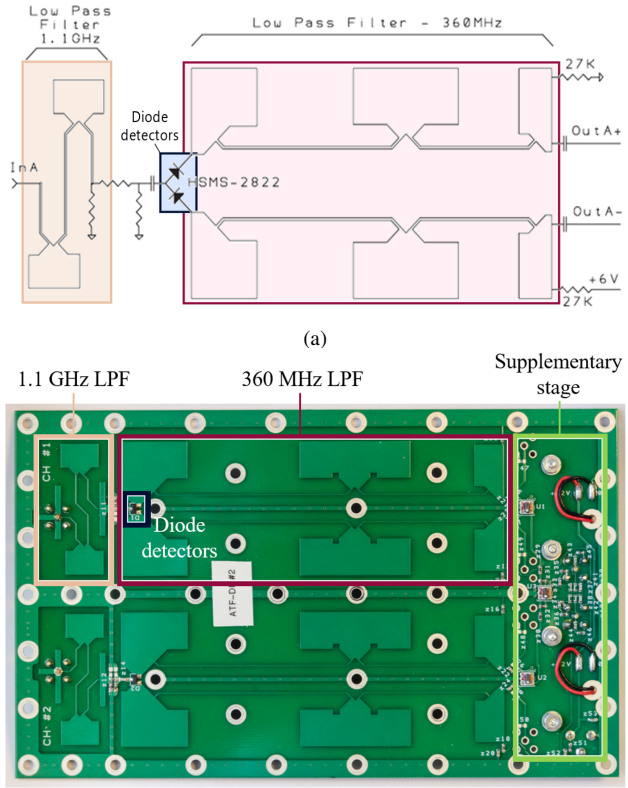

Figure 3: (a) Schematic and (b) photograph of the processor with the diode detectors and LPFs highlighted. (b) also shows the supplementary stage required to interface the processor with the ATF2 FONT system.

Supplementary Stage

For the ATF2, a supplementary stage of processing is required to interface the prototype processor and the FONT5A board [7] used to digitise the BPM waveforms. On the processor board, 180° combiners were added to form the difference (V_Δ) and sum (V_Σ) signals from V_T and V_B. The FONT5A board sampling rate of 357 MHz would be unable to handle the processor's narrow output pulses and, consequently, two 145 MHz LPFs were used to broaden the V_Σ and V_Δ pulses. External to the board, an amplifier was added to match the FONT5A board digitiser sensitivity and additional 145 MHz LPFs were included to further broaden the output peaks and to reduce out-of-band noise from the amplifier.

RESULTS

Latency

With a CLIC bunch spacing of 0.5 ns, it is critical to minimise the latency from all components in the intra-train IP feedback system, including the BPM processor. The prototype processor tested at the ATF2 included the components relevant for CLIC and also supplementary components to make the processor compatible with the ATF2 FONT con-

ISBN: 978-3-95450-208-0 doi:10.18429/JACoW-IPAC2019-WEPGW092

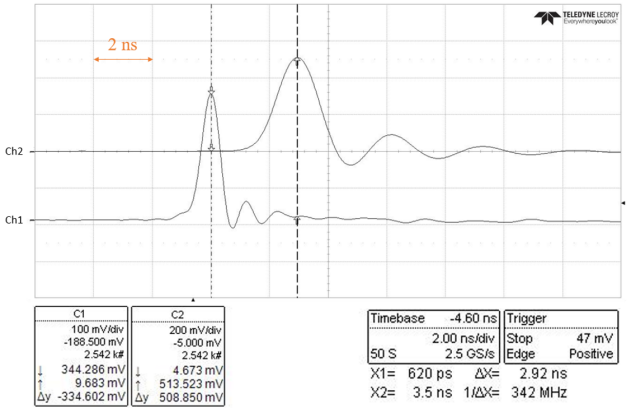

Figure 4: Oscilloscope waveforms from a testbench setup without (Ch1) and with (Ch2) the prototype processor.

figuration. In a testbench setup the prototype processor was measured to have a latency of ∼3 ns, as shown in Fig. 4. This would be expected to scale to ∼1 ns for a CLIC version of the processor.

Resolution

Position measurements from the three BPMs, P1, P2 and P3, are required to estimate the system resolution. Conventional processors were used for P2 and P3 and the prototype processor was instrumented on P1. Beam position measurements at P2 and P3 were used to predict the beam positions at P1 and the difference between the measured and predicted values were calculated for many consecutive pulses. The beam position at P1, $y_{\mathrm{P1}}^{\mathrm{pred.}}$, was predicted using a linear combination of the measured positions $y^{\mathrm{meas.}}$ at P2 and P3,

$$y_{\mathrm{P1}}^{\mathrm{pred.}} = \mathrm{A}_{12} y_{\mathrm{P2}}^{\mathrm{meas.}} + \mathrm{A}_{13} y_{\mathrm{P3}}^{\mathrm{meas.}}, \tag{3}$$

where A_{12} and A_{13} are coefficients obtained using a least-squares fit. The distributions of measured and predicted bunch positions at P1 are presented in Fig. 5.

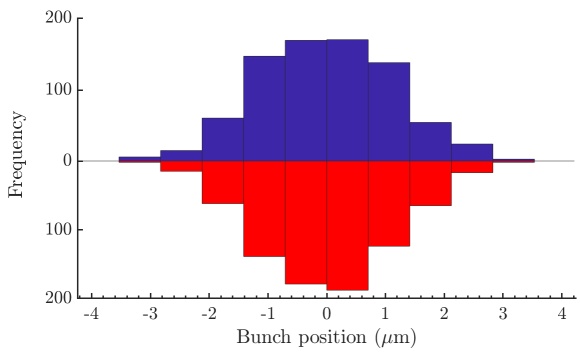

Figure 5: Measured (blue) and predicted (red) bunch positions at P1, with standard deviations of 1.16 µm and 1.10 µm respectively.

Each measured position will have an associated error, ϵ. The 'residual' is defined as $R_{\mathrm{P1}} = y_{\mathrm{P1}}^{\mathrm{meas.}} - y_{\mathrm{P1}}^{\mathrm{pred.}}$ so that

$$\begin{aligned} R_{\mathrm{P1}} &= y_{\mathrm{P1}}^{\mathrm{meas.}} - \mathrm{A}_{12} y_{\mathrm{P2}}^{\mathrm{meas.}} - \mathrm{A}_{13} y_{\mathrm{P3}}^{\mathrm{meas.}}, \\ &= \epsilon_{\mathrm{P1}} - \mathrm{A}_{12}\epsilon_{\mathrm{P2}} - \mathrm{A}_{13}\epsilon_{\mathrm{P3}}. \end{aligned} \tag{4}$$

The resolution, σ, is defined as std(ϵ). The errors ϵ_{P1}, ϵ_{P2} and ϵ_{P3} are assumed to be uncorrelated random variables and therefore

$$\begin{aligned} (\mathrm{std}(R_{\mathrm{P1}}))^2 &= \sigma_{\mathrm{P1}}^2 + \mathrm{A}_{12}^2\sigma_{\mathrm{P2}}^2 + \mathrm{A}_{13}^2\sigma_{\mathrm{P3}}^2, \\ \sigma_{\mathrm{P1}} &= \sqrt{(\mathrm{std}(R_{\mathrm{P1}}))^2 - \mathrm{A}_{12}^2\sigma_{\mathrm{P2}}^2 - \mathrm{A}_{13}^2\sigma_{\mathrm{P3}}^2}. \end{aligned} \tag{5}$$

To calculate σ_{P1}, the resolution with the conventional processors (σ_{P2} and σ_{P3}) must be estimated. These studies were performed at a charge of $0.65 \times 10^{10}\, e^-$/bunch for which the resolution with three conventional processors was previously measured as ∼200 nm [10]. By assuming $\sigma_{\mathrm{P2}} = \sigma_{\mathrm{P3}} = 200$ nm, the prototype processor was estimated to have a resolution of ∼325 nm. We would estimate that the best and worst plausible values for the conventional processor resolution were 150 nm and 250 nm respectively, which would correspond to upper and lower limits on the prototype processor resolution of ∼350 nm and ∼275 nm.

CONCLUSIONS

The design for a prototype processor constructed using diode detectors has been described. The processor was tested at the ATF2 but would be suitable to be scaled to satisfy higher CLIC frequencies. The processor is able to operate in high magnetic fields and is radiation-hard. The processor was demonstrated to have a latency of ∼3 ns which is expected to scale to ∼1 ns for CLIC. The processor was implemented on a stripline BPM and estimated to have a resolution of ∼325 nm.

OUTLOOK

For the ATF2 prototype processor, silicon Schottky diodes in large SOT23 packages were used; to scale this for the higher frequency CLIC beam, they would be replaced by GaAs diodes in smaller packages. The 1.6 mm FR4 board would also be replaced by a ∼0.8 mm RF substrate board. The CLIC processor outputs are envisaged to be input into differential amplifiers on a custom GaAs Monolithic Microwave Integrated Circuit.

ACKNOWLEDGEMENTS

We would like to thank KEK for providing the beam time for these experiments, as well as the ATF2 staff and our collaborators for their support and guidance. This work was supported by the UK Science and Technology Facilities Council, CERN, and the European Commission's Horizon 2020 Programme through the Marie S.-Curie RISE project E-Jade, Contract No. 645479.

ISBN: 978-3-95450-208-0 doi:10.18429/JACoW-IPAC2019-WEPGW092

REFERENCES

[1] J. Resta Lopez *et al.*, *Journal of Instrumentation*, vol. 5, p. 09007, 2010.

[2] A Robson *et al.*, The Compact Linear e^+e^- Collider (CLIC): Input to the European particle physics strategy update on behalf of the CLIC and CLICdp collaborations, December 2018. https://indico.cern.ch/event/765096/contributions/3295978/attachments/1785331/2906390/CLIC-AcceleratorDetector.pdf

[3] R. Bodenstein *et al.*, in *Proc. IPAC'16*, paper WEPOR009, pp. 2683-2686 (2016).

[4] M. Aicheler *et al.*, CLIC conceptual design report, CERN-2012-007, 2012.

[5] J. Alabau-Gonzalvo *et al.*, ATF2 Summary and Status. ICFA Beam Dynamics Newsletter, vol. 54, pp. 62–80.

[6] R.J. Apsimon *et al.*, *Phys. Rev. ST Accel. Beams*, vol. 18, 032803 (2015).

[7] B. Constance, Ph.D. Thesis, Oxford University, 2011.

[8] G. White *et al., Phys. Rev. ST Accel. Beams*, vol. 112, p. 034802, 2014.

[9] N.B. Kraljevic, Ph.D. Thesis, University of Oxford. (2015).

[10] N.B. Kraljevic *et al.*, in *Proc. IPAC'17*, paper TUPIK110, pp. 1979–1982.