Development of a DLLRF using commercial uTCA platform

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RF&Linac Section - ALBA Accelerators Division

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Outline

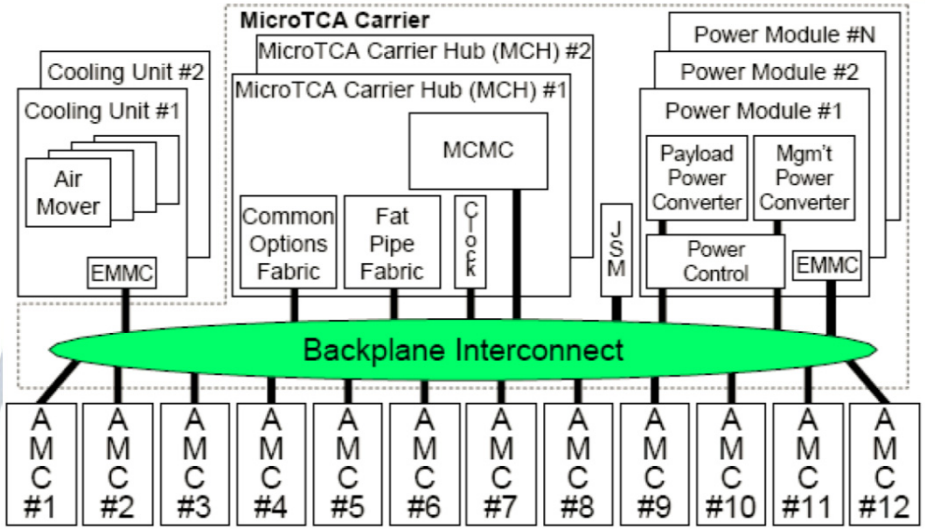
- ✓ Motivation
  - Why uTCA?
  - Why commercial?
- ✓ Implementation of Digital LLRF of ALBA
  - Comparison between old and new LLRF platforms
  - Main functionalities
  - Extra Utilities
- ✓ Conclusions

Motivation

Motivation

Why uTCA?

- ✓ Open standard developed by PICMG for building high performance switched fabric computer system
- ✓ More than 100 vendors offer different HW boards
- ✓ Modular system (flexibility)
- ✓ Point-to-point, dual and mesh topologies for GigE, Fibre Channel, PCIe, SRIO
- ✓ Standard HW platform in several labs: DESY, ESS, Diamond, Sirius



Common uTCA carrier

- Up to 12 AMC boards
- Backplane interconnect between all boards
- Power and cooling modules

Motivation

Why commercial?

- ✓Support from Industry
- ✓Lower development costs

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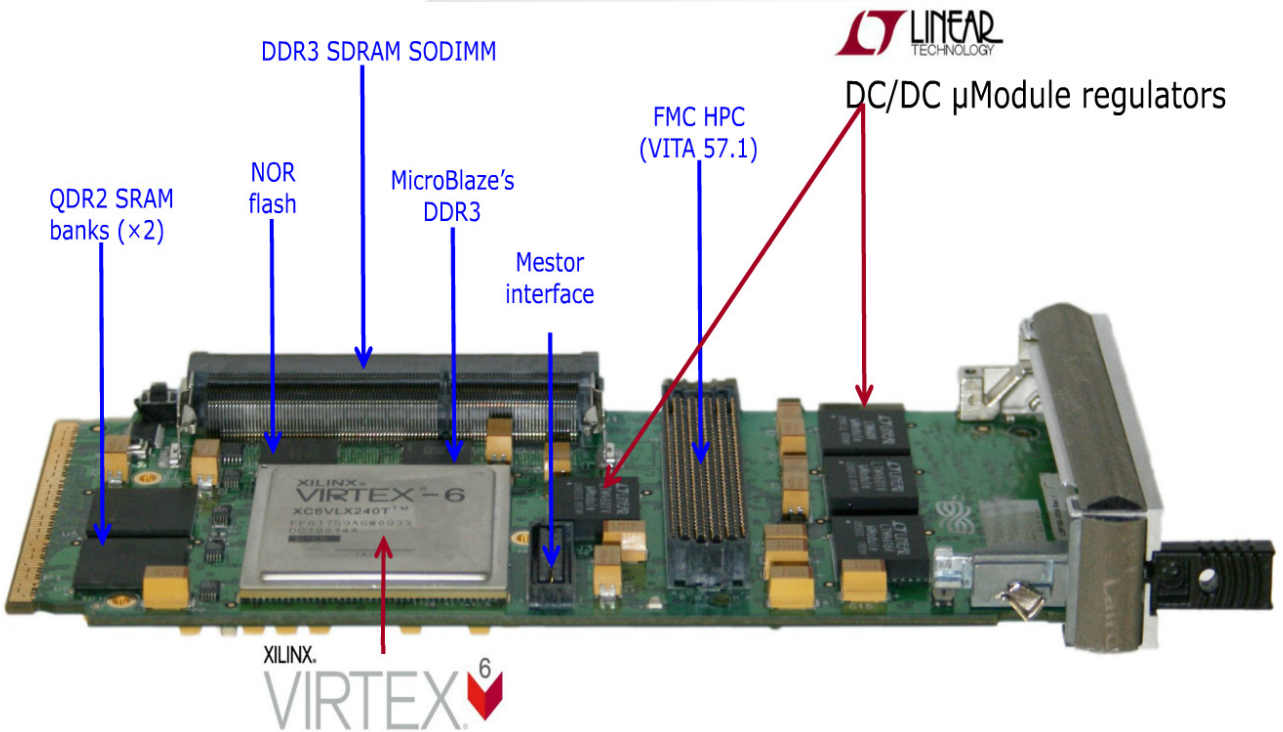
- ✓Support from Industry
- ✓~~Lower~~ development costs: Shared by multiple customers
- ✓~~Lower~~ development time
  - In-house: specs defined and later development started
  - Commercial solution: specs defined and looked for an already implemented solution

- ✓ Convenient when manpower resources are limited and timelines adjusted
- ✓ Nowadays state-of-the-art HW available in industry

New ALBA LLRF based on uTCA

Commercial Solution : AMC Perseus 6010 from Nutaq

- ✓ Compliant with technical and economical requirements of ALBA
- ✓ FW included with communications protocol embedded
- ✓ SW migration from old to new system: 4 weeks work



Implementation

ALBA LLRF requirements

Loops Resolution and bandwidth (adjustable parameters)

	Resolution	Bandwidth	Dynamic Range
Amplitude Loop	< 0.5 % rms	[0.1, 50] kHz	30dB
Phase Loop	< 0.5 º rms	[0.1, 50] kHz	360º
Tuning	< ± 0.5º	--	< ± 90º

Present (old-2006) LLRF Main Characteristics

- ✓ cPCI board with Virtex-4 FPGA
- ✓ Digital IQ demod
- ✓ Main FB loops: Amplitude, phase and tuning
- ✓ Board drivers: WXP

Digital board: VHS-ADC from Nutaq

Upgrade needed for LLRF collaborations with Diamond, Sirius and Maxlab

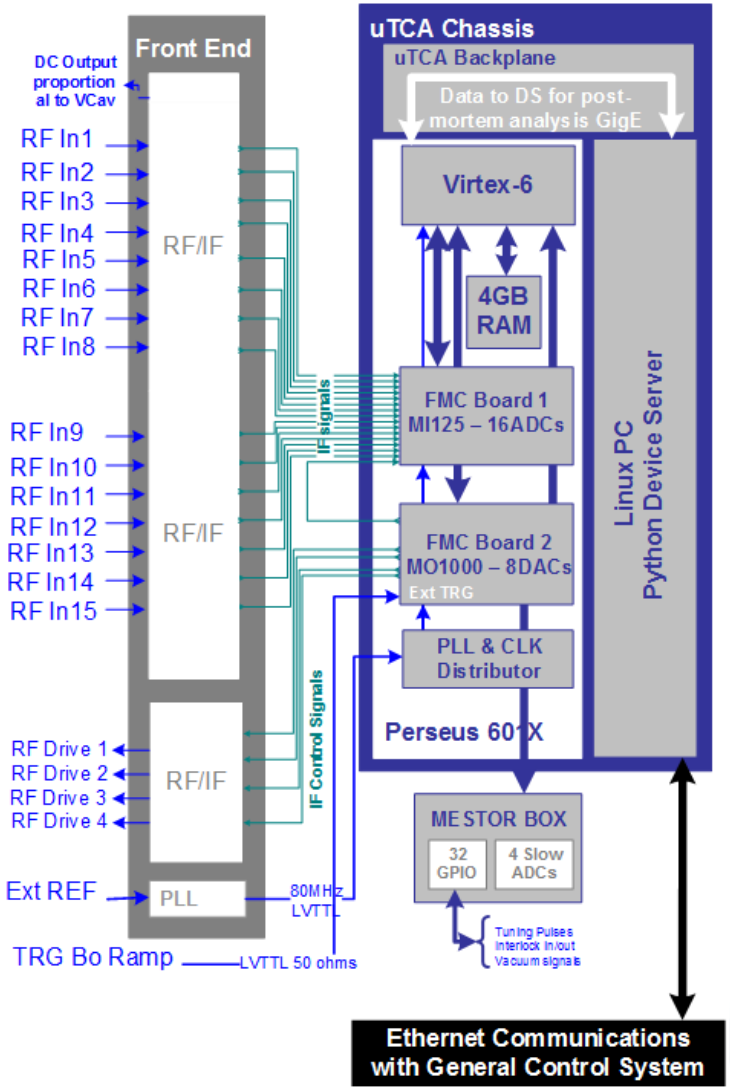
New ALBA LLRF based on uTCA

Main Characteristics

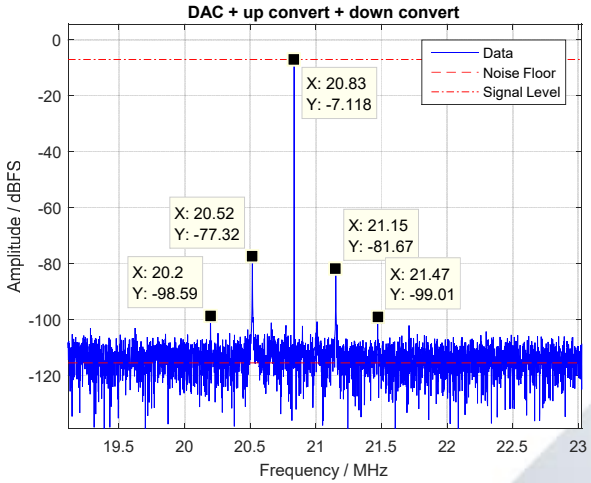
- ✓ AMC Board with Virtex-6 FPGA + 2FMC boards with 16ADCs and 8 DACs
- ✓ Board drivers: Linux
- ✓ Loops: similar resolution and BW
- ✓ Control of 2 cavities included in one FPGA Board

Further utilities implemented

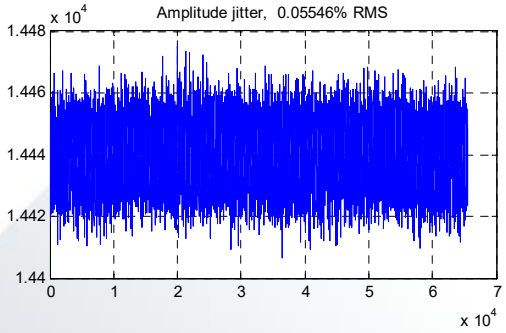
- ✓ IQ loops and Polar Loops implemented
- ✓ Several cavities configuration implemented
- ✓ Interlocks handling
- ✓ Automated processes

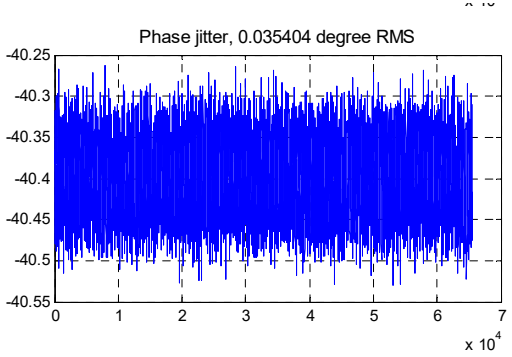


uTCA LLRF performances



Data from DIAMOND LLRF: Poster THPAB152





ADCs Resolution

Amplitude	< 0.06% rms
Phase	< 0.04º rms
Signal to Noise Ration (SNR)	70 dB

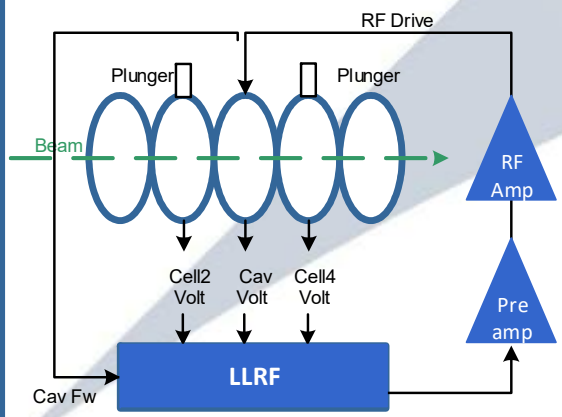
Loops Resolution @ 80MHz

Amplitude	0.18% rms
Phase	0.1º

3 Cavities Control Configuration

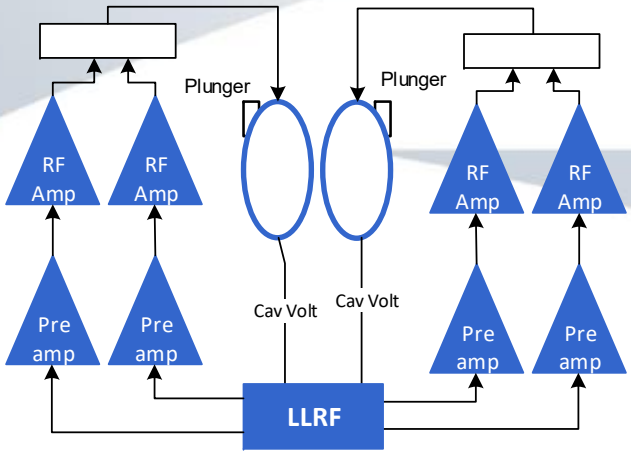
Booster Cavity

- ✓ 5-Cells Cavity
- ✓ Ramping
- ✓ 2 Plungers control



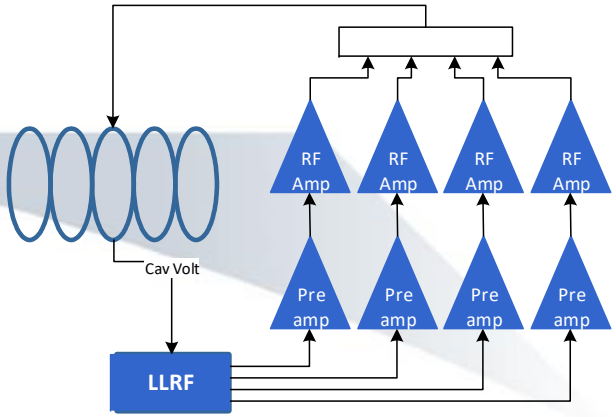
Normal Conducting

- ✓ 2 Cavities independently controlled
- ✓ 2 Drivers per Cavity
- ✓ 2 Plungers control



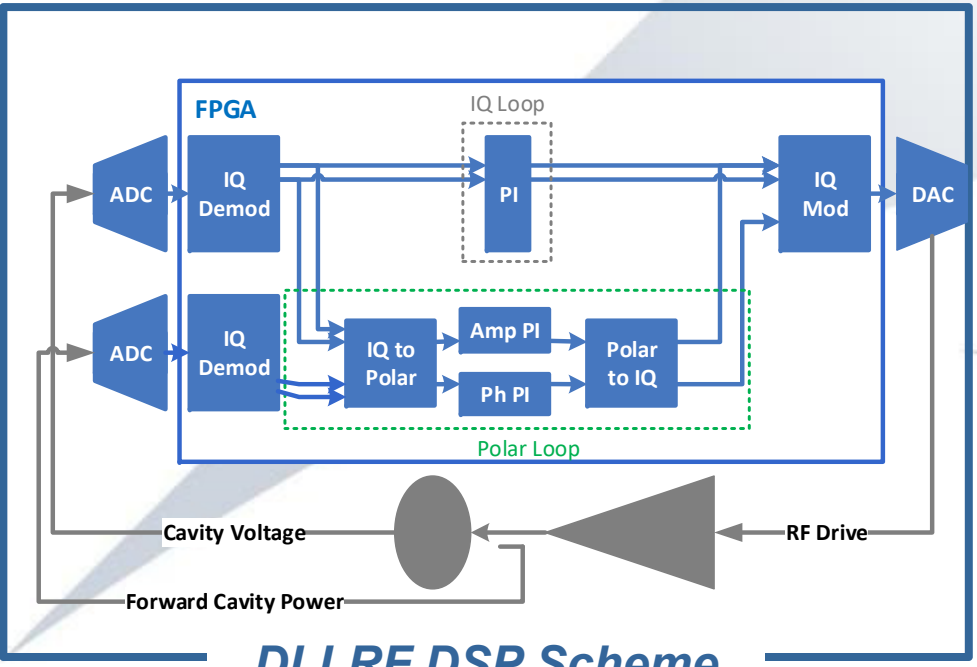
Super Conducting

- ✓ 1 Cavity driven by 4 Amplfiers
- ✓ Amplitude and phase balance compensation independently applied to each drive

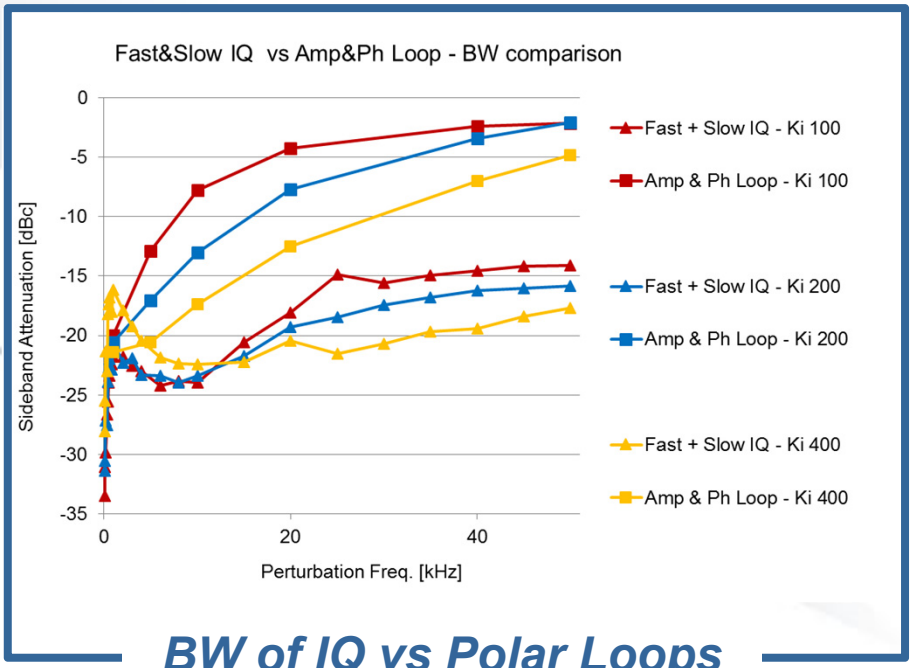


IQ vs Polar Loops

- ✓ IQ Loops: Smaller group delay → higher BW
- ✓ Polar Loops:
  - Allows setting different BW for Amplitude and Phase loops
  - **Low BW Amplitude loop** can be set to control cavity voltage with no interference with synchrotron tune
  - **High BW Phase loop** can be set to remove ripples of PS of RF amplifier



DLLRF DSP Scheme



BW of IQ vs Polar Loops

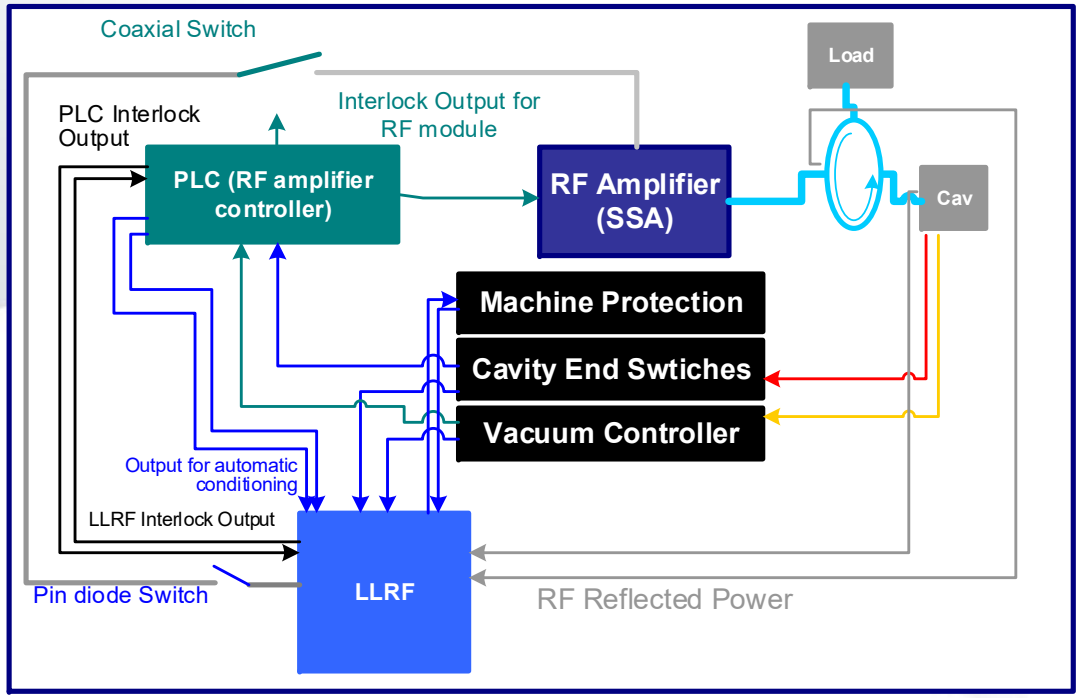
Fast interlocks

Interlocks inputs

- ✓ Reverse Power interlocks: adjustable threshold
- ✓ Digital interlock inputs: arc detectors, vacuum, MPS and others

Interlock Outputs:

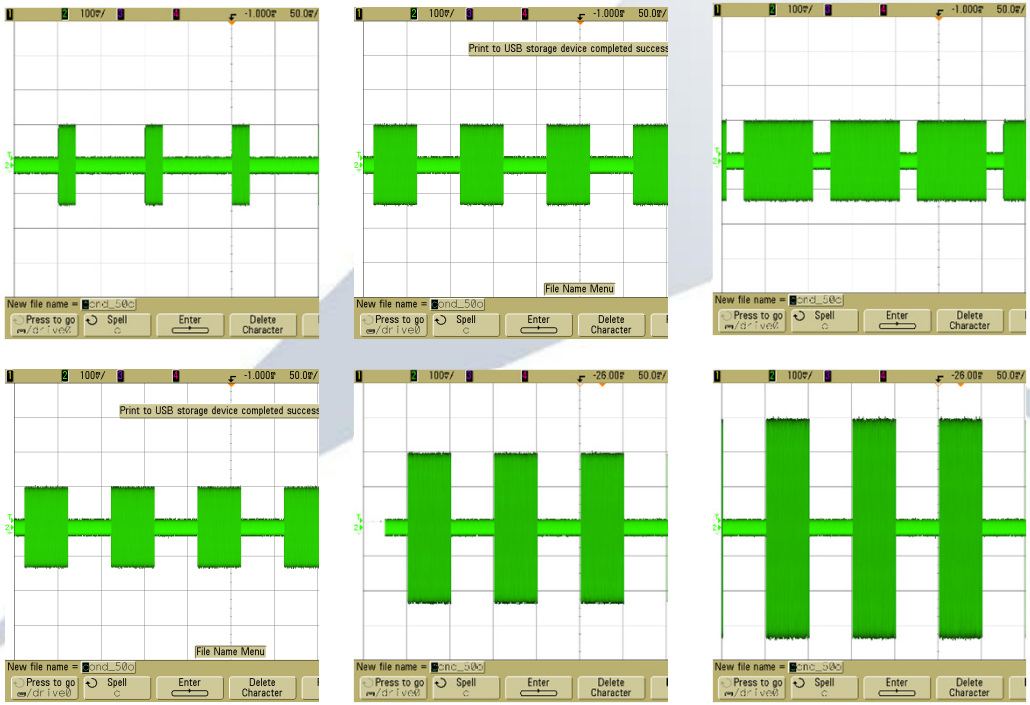
- ✓RF Drive cut in less than 10 us (pin diode switch)
- ✓Trigger to FDL and MPS
- ✓Trigger to Tx PLC
- ✓LLRF loops set to STBY



Manual Conditioning

RF Drive square modulated

- ✓Duty Cycle of pulses adjustable (1-100%)
- ✓Amplitude adjustable
- ✓Time between pulses = 100ms (10Hz)
- ✓ Tuning Loop only enable at top of the pulses



Drawbacks

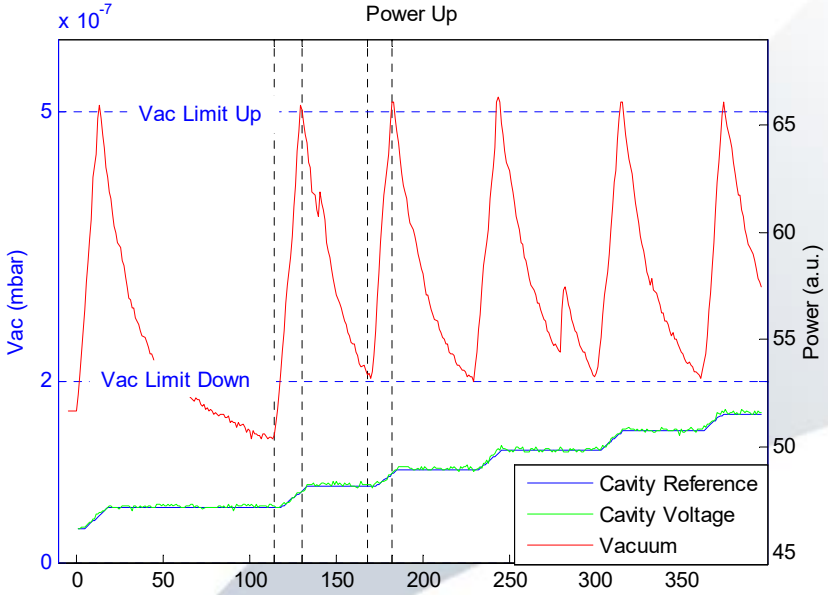
- ✓ Vacuum levels not considered by LLRF → frequent interlocks

Automated Conditioning

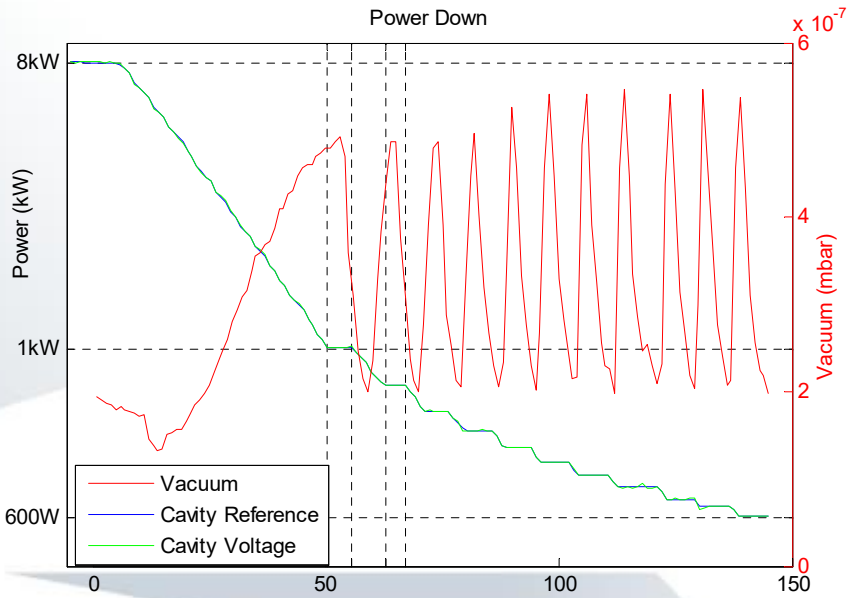
Vacuum signal connected to LLRF

✓Amplitude and duty cycle increase depending on vacuum levels

✓Amplitude increase rate (slope): adjusted by operator



Voltage Increase rate set to 0.03mV/s

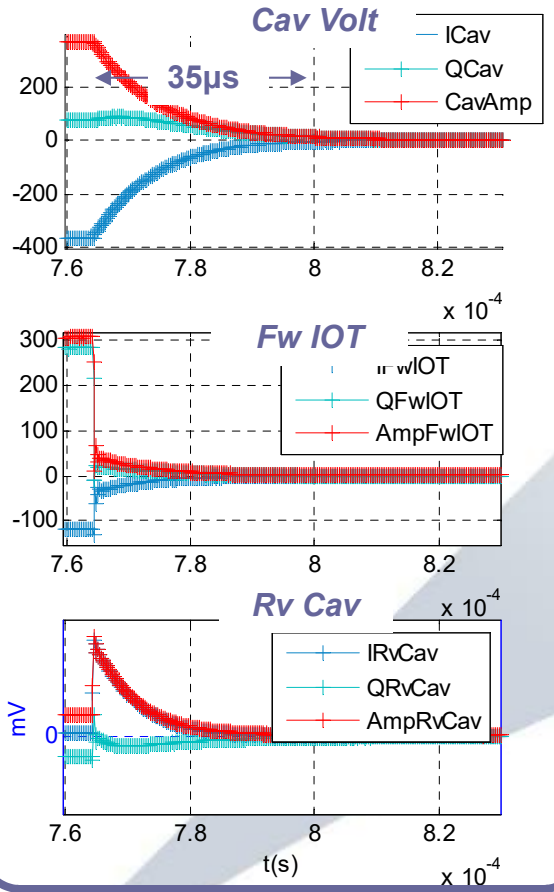


Voltage Decrease rate set to 1mV/s

- Vacuum < Limit Down → Voltage Amplitude Increases/Decreases
- Vacuum > Limit Up → Voltage Amplitude remains constant until vacuum is below limit down

Fast Data Logger for post-mortem

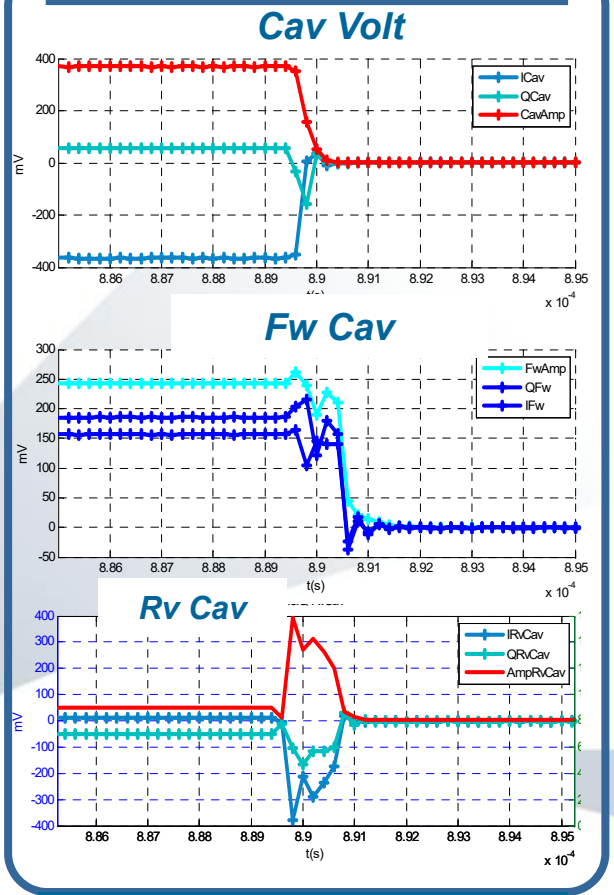
Vacuum Trip at 47kW



Cavity Discharged in 35 µs

Full reflected power AFTER Pin diode opening

Reflected Trip at 35kW

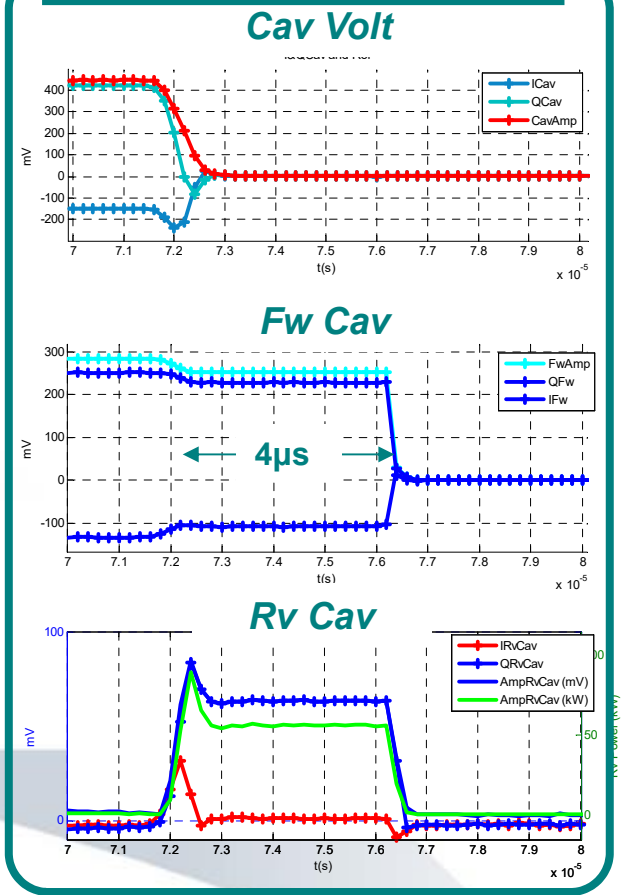


Cavity Discharged in 0.8 µs

Short-circuit in the cavity

Pin Diode opened in less than 1.5µs after interlock detection

Arc at 41kW



Cavity Discharged in 1.2 µs

Full reflected power during 4µs until arc occurs and Pin Diode gets opened

Extra features

Automatic startup for fast cavity recovery

Feed-forward loops for beam stability

- ✓ FF loops for RF trip compensation
- ✓ FF loops for beam loading compensation

Slave loop for power unbalance compensation

Tuning based on Freq modulation

…

Summarizing:

Commercial FPGA boards offer specs and flexibility which allows adapting your control loops to the evolving needs of machine operation

Summary and Conclusions

✓ Commercial uTCA Boards:

- Standard widely used in industry and accelerators
- Great variety of uTCA products in market to match your requirements

✓ LLRF Capabilities

- FB loops for Amp, Ph control and tuning
- Control algorithms can be easily adapted to different machine needs in one single system
- FPGAs increasing processing resources allows integrating further utilities in LLRF:
  - Automatic conditioning
  - Automatic startup
  - Interlocks handling

Thanks for your attention

Questions?