DESIGN AND SIMULATION OF VOLTAGE MULTIPLIER COLUMN OF A 300 keV, 10 mA PARALLEL FED COCKCROFT WALTON ELECTRON ACCELERATOR FOR INDUSTRIAL APPLICATIONS

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Abstract

In this article a 300 keV, 10 mA multiplier column has been designed for a parallel fed Cockcroft Walton electron accelerator for industrial applications. The parallel fed Cockcroft Walton multiplier is a capacitive coupling multiplier with diode rectification which can convert an input RF voltage to a low ripple output DC voltage. In this research has been tried to get a low ripple (300 keV output) dc voltage. At first, the voltage multiplier column was simulated with PSpice simulation software. After doing the PSpice simulations, optimum value of different parameters was determined.

INTRODUCTION

In this article the performance of a parallel fed Cockcroft Walton accelerator is described by focus on the multiplier column. This type of accelerators are being made in energy range from 0.1 MeV to about 7 MeV for industrial, medical and research applications. The low ripple and stable voltage of this accelerators is a good feature for sensitive and precise ion beam applications [1]. In this accelerators a filtered DC input power is being applied to an oscillator unite and the oscillator converts it to a sinusoidal RF (~100 kHz) voltage. Produced RF voltage amplitude is being in-creased to several kilo volts by a step up air core RF transformer [2]. The output of secondary of the RF transformer is being applied to a capacitive coupling multiplier column with diode rectification to convert the RF voltage to a low ripple DC voltage. There are three ways to produce higher levels of DC voltage: 1) increasing the input RF voltage to the multiplier column, 2) increasing number of the rectification stages and 3) regulating of the capacitances of the multiplier column [3]. The output DC voltage of the multiplier column can be calculated from the following formulas [4].

$$U = \frac{NU_0}{k} - U_{droop} \pm U_{ripple} \quad (1)$$

$$U_{droop} = \frac{I(N-1)}{fC_{se}k} \quad (2)$$

$$U_{ripple} = \frac{I}{2fC_{se}} \quad (3)$$

$$k = 1 + 4\frac{C_{ca}}{C_{se}} \quad (4)$$

In these equations U_0 is the amplitude of input RF to the multiplier column, N is number of stages, I is beam current, f is the RF frequency, k is coupling coefficient, C_{ca} is shunt capacitance and C_{se} is coupling capacitor [5]. In the no-loud condition that the beam current is zero, the terms of droop voltage and ripple voltage are also zero.

MULTIPLIER COLUMN CIRCUIT PSPICE SIMULATION

The multiplier column circuit consists of, rectifier diodes, resonant selves, two support selves at the ends and four types of capacitor. Figure 1 shows a part of simulated circuit and its components by PSpice software.

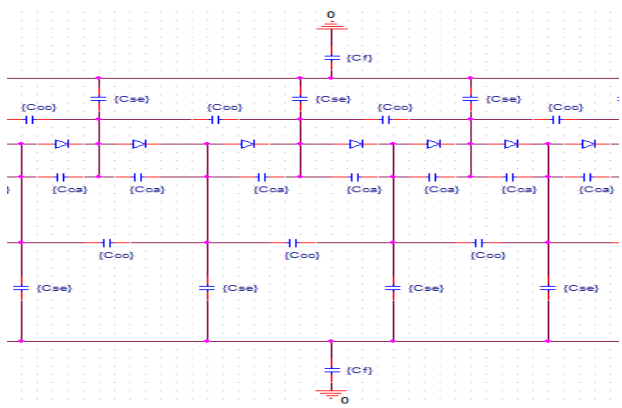

Figure 1 : simulated multiplier column circuit.

With respect to the formulas of (2) and (3), the terms of U_{droop} and U_{ripple} are adversely related to input RF voltage frequency. Therefor the frequency range is an important factor in this circuit. Figure 2 shows the effect of the frequency range (simulated from 100 kHz to 200 kHz) on the ripple and the level of output DC voltage.

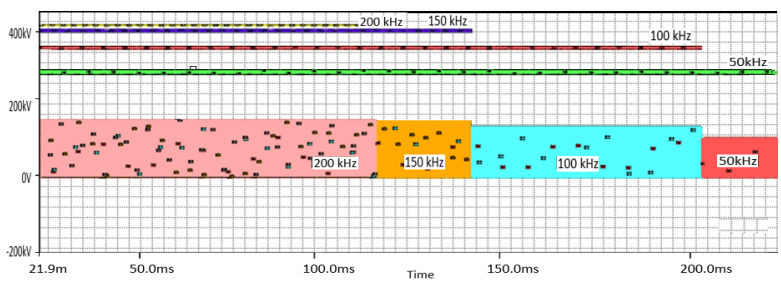

Figure 2 : frequency sweep with PSpice software.

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According to the figure 2, the upper frequencies cause the lower voltage ripple and the higher DC voltage level. In equal condition, Green curve (50 kHz) shows about 300 kV output DC voltage while blue curve (150 kHz) shows about 400 kV output DC voltage. Also the voltage ripple of the green curve is more than that of the blue curve. Also the wide curves with zero baseline, show the difference potential across one diode stack in different frequencies. These curves show that by increasing the frequency, also the difference potential across diode stacks increases. Therefore this simulation shows that RF voltage frequency is an important factor for optimum performance of this circuit. With respect to dependence of the diode stacks reverse recovery time, power loss of RF transformer and some other components to voltage frequency, the suitable frequency range in Practice is being constrained to 100 kHz-150 kHz. For example in this frequencies the reverse recovery time of the diodes should be lower than 100 ns.

CALCULATION OF NUMBER OF STAGES OF MULTIPLIER COLUMN

At first the equations of (1), (2), (3) and (4) should be solved for a 300 keV, 10mA electron beam to calculate the number of stages. The earned optimum values of PSpice simulations for capacitances of $C_{ca}$and $C_{se}$are respectively 3 pf and 12 pf. Now the coupling coefficient can be calculated from equation (4):

$$k = 1 + 4\frac{C_{ca}}{C_{se}} = 1 + 4\frac{3}{12} = 2 \quad (5)$$

Also with respect to given values of different parameters in table 1, ripple voltage, droop voltage and the number of stages can be calculated.

Table 1 : Parameter Values

parameter	value
f	100 kHz
C_{se}	12pf
k	2
I	10mA
U_0	50kV
U	300kV

The droop voltage is:

$$U_{droop} = \frac{I(N-1)}{fC_{se}k} = \frac{10\times10^{-3}(N-1)}{100\times10^{3}\times12\times10^{-12}\times2}4.16 \times 10^{3}(N-1)$$

And the ripple voltage is:

$$U_{ripple} = \frac{I}{2fC_{se}} = \frac{10\times10^{-3}}{2\times100\times10^{3}\times12\times10^{-12}} = 4.16kV$$

Calculating number of stages:

$$E = \frac{NU_0}{k} - \frac{I(N-1)}{fC_{se}k} \rightarrow 300\times10^{3} = \frac{N\times50\times10^{3}}{2} - 4.16\times 10^{3}(N-1) \rightarrow 300 = 25N - 4.16(N-1) \rightarrow 295.84 = 20.84N \rightarrow N = 14$$

COMPARISON OF PSPICE SIMULATION RESULTS WITH THEORETICAL CALCULATION RESULTS

After replacing the parameter values in the simulated circuit in the PSpice, the output results for DC voltage and beam current were earned. The output DC voltage curve has been shown in Figure 3.

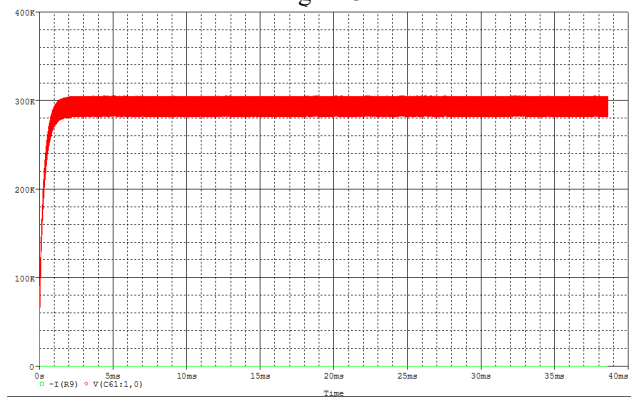

Figure 3 : PSpice result for output DC voltage.

According to figure 3, the PSpice simulation shows the same result as the theoretical calculations. Also according to equation (3), the ripple voltage is independent of number of stages. The transient time for reaching to the flat aria of the output voltage is less than 2ms. Also the output beam current curve has been shown in Figure 4.

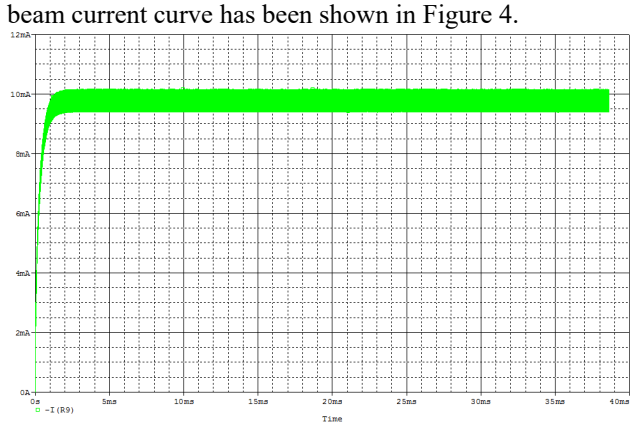

Figure 4 : PSpice result for output beam current.

Also according to this curve the output current is 10 mA. In this simulations the loud current was 30 MΩ and the number of stages is 14 as calculated by formula in the last part.

DESCRIPTION OF THE MULTIPLIER COLUMN STRUCTURE

The multiplier column of the parallel fed Cockcroft Walton accelerator is a mechanical structure. In this structure the capacitances are being made amongst metallic electrodes (corona rings and RF electrodes). This electrodes are being made by stainless steel and sometimes by aluminium. Another components such as the diode stacks, electron gun and accelerating tube (more information about the electron gun and the accelerator tubes for this type of accelerators has been reported respectively in

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references of [5] and [6]) are connected amongst this structure. This structure should be housed in a pressure vessel and the pressure vessel can be filed by insulator gases (such as SF_6).

CONCLUSIONS

The parallel fed Cockcroft Walton accelerators has a low ripple output DC voltage that is suitable for industrial applications. According to equation (3), the ripple voltage is independent of number of stages and this is a special feature for this type of accelerators. The RF frequency range is an important factor for optimum performance of multiplier column.

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