DIGITAL LOW LEVEL RF SYSTEMS FOR DIAMOND LIGHT SOURCE

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Abstract

Analogue low level RF (LLRF) systems have been used to date for Diamond storage ring and booster RF cavities. They have been in operation for more than ten years without major problem. However, digital LLRF can offer new desirable functionalities such as fast data logging, "probe blip" blockage and automation of routine tasks. Better performance is also envisaged with up to date hardware. A digital LLRF system has been developed with Alba Synchrotron as a common platform for the storage ring and booster, including superconducting and normal conducting RF cavities. The new digital LLRF is based on Virtex6 FPGA and fast ADCs and DACs. One system has been built and verified in the Diamond booster with beam. The design will be implemented for all other Diamond RF cavities.

INTRODUCTION

The analogue LLRF systems have been in operation for more than 10 years. Due to their age, most of the components are or will be obsolete. The booster and storage ring RF system are both running at 499.7 MHz, but they are not derived from the same design. They also lack the flexibility and other desirable functionalities that the digital LLRF can offer. Furthermore, Diamond storage ring RF will be upgraded to hybrid operation of normal conducting RF cavities and superconducting RF cavities [1]. As a result, new LLRF systems need to be developed for the normal conducting RF cavities. Based on all these impending requirements, we decided to develop a new digital LLRF (DLLRF) as a common platform for the booster RF cavity, storage ring superconducting RF cavities and normal conducting RF cavities.

ALBA has been operating using DLLRF since 2008 [2]. The new DLLRF was developed based on ALBA's mature design using commercially available hardware. Classical digital IQ modulation and demodulation were used as the major algorithm. The new DLLRF is designed to achieve 0.1% amplitude stability and 0.1° phase stability under normal operating conditions.

DLLRF DESIGN

The new DLLRF was based on the Micro Telecommunications Computing Architecture (MicroTCA) standard. It was chosen for its reliability, modularity and scalability. Due to its highly modular construction, every component of the system can be replaced easily in the future when higher performance hardware is available. A commercial advanced mezzanine card (AMC), Perseus 601X with Virtex6 FPGA from Nutaq, is used as the core processor of the control algorithm. 16 Channel 14-bit ADCs and 8 channel 16-bit DACs FPGA mezzanine cards (FMC) are used for analogue input and out interface.

Hardware

The block diagram of one configuration of the DLLRF is shown in Fig. 1. The RF signal flow is shown in Fig. 2. The major hardware comprises clock and local oscillator (LO) generation, RF up-conversion front end, RF down-conversion front end, digital signal interface and MicroTCA system. There is a PC in the MicroTCA chassis running Linux and EPICS to integrate the DLLRF into Diamond control system.

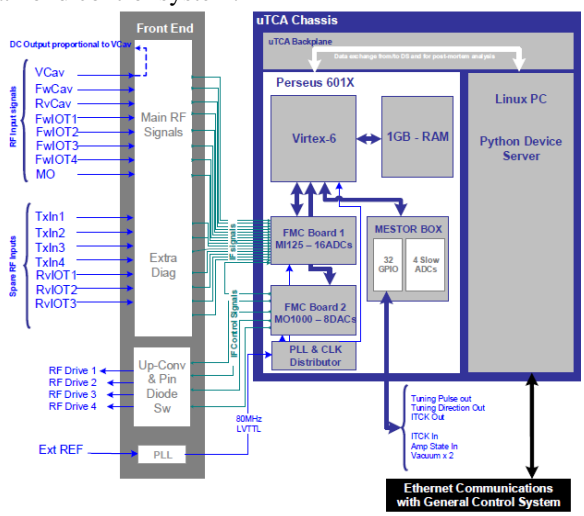

Figure 1: DLLRF block diagram.

Clock and LO Generation Two methods were tested to generate the clock and LO signal. The first method used CDC7005 PLL from Texas Instruments with an 80 MHz VCXO. The 80 MHz output fans out to provide up to 5 outputs. One output is divided by 4 to provide a 20 MHz intermediate frequency (IF) signal. This signal is mixed with the master oscillator (MO) to generate the 480 MHz LO. The 499.7 MHz MO was divided by 50 to provide a reference signal to the PLL so that the clock and IF signal are synchronized with the MO. The second method used frequency dividers to provide the IF and clock. One channel was the MO divided by 24 to provide IF signal. Another channel was the MO divided by 6 to provide the clock for both ADCs and DACs. The two methods gave similar performance. The second method was chosen due to its simplicity.

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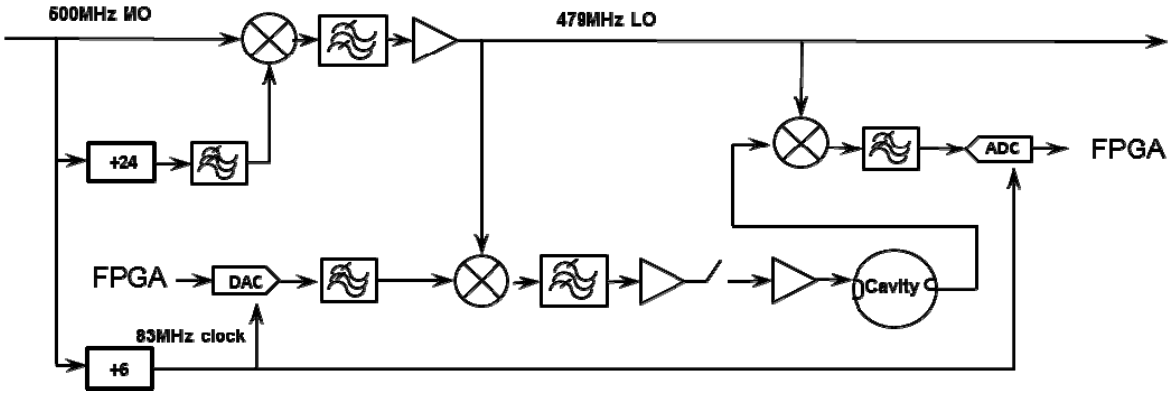

Figure 2: Schematic of RF signal processing.

Down-conversion and up-conversion of RF Signals During down-conversion, the RF signals are simply mixed with 479 MHz LO signal to generate 20.8 MHz IF signal. The IF signal is filtered before being sampled by ADC at 4 times the IF frequency. In the up-conversion chain, the DAC directly generates 20.8 MHz IF signal, which is mixed with LO, filtered and amplified. There is a PIN switch in the up-conversion unit that can be triggered by an interlock. A schematic of this process is presented in Fig. 2.

Firmware

The schematic of the firmware is shown in Fig. 3.

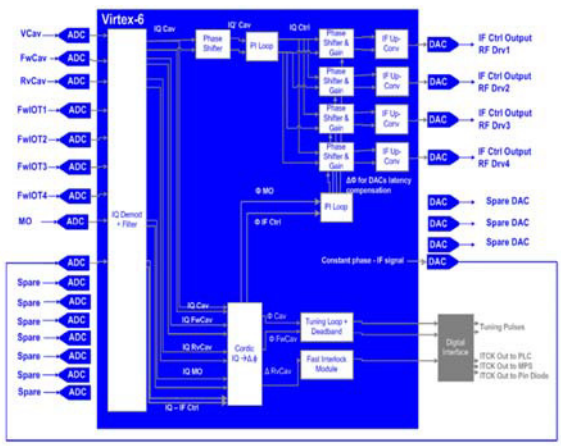

Figure 3: DLLRF firmware schematic.

The following functionalities are built into the FPGA firmware:

- IQ or polar PI loops of the cavity field to control amplitude and phase.
- Cavity tuning.
- Fast interlocks handling.
- Automatic start-up of the system.
- Automatic conditioning of the cavity
- Monitoring of RF signals.
- Recording of main digital processing signals for post-mortem analysis.

The sampled IF signal is demultiplexed into IQ components and filtered. A software counter controller by the MO phase is used to control the demultiplexer. This enables the user to choose the sample to start with. Software phase shifter was implemented for each signal to keep the control loops stable. The firmware can be configured to run either in IQ PI loop or in polar PI loop mode. In the IQ loop mode, the phase set point and open loop measured phase should be in the same quadrant to keep the loop sable. In the polar loop mode, the CORDIC algorithm is used to translate IQ components to amplitude and phase before comparing them with the set points. The CORDIC algorithm is also used for the cavity tuner loop.

The DLLRF can be configured to run 3 modes, namely the normal conducting booster cavity mode, superconducting storage ring cavity mode and normal conducting storage ring cavity mode. In the booster cavity mode, cavity field ramping and tuning of the multi-cell cavity field flatness are also implemented.

The 16 channel ADC FMC enables the monitoring of most of the RF signals in the RF chain for diagnostics. The 4GB ram is used to store the ADC data. This data can be retrieved after an interlock trigger or by a software trigger.

DLLRF TESTS

The DLLRF was tested after the firmware and hardware were completed. The tests went through several stages, namely low power test, high power test, test in the booster with beam. All the major functionalities were verified during the test.

ADC Test The raw data from ADCs were retrieved using the fast data logger. Performance was consistent with the specification of the ADC. A 70 dB signal to noise ratio (SNR) was achieved. This can be seen in the FFT of the raw data shown in Fig. 4. A phase measurement result from the raw data without any filtering is shown in Fig. 5.

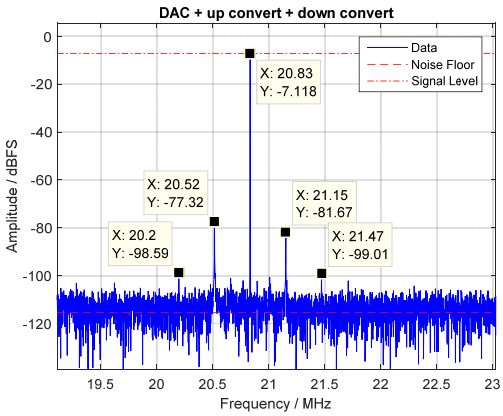

Figure 4: FFT of raw ADC data.

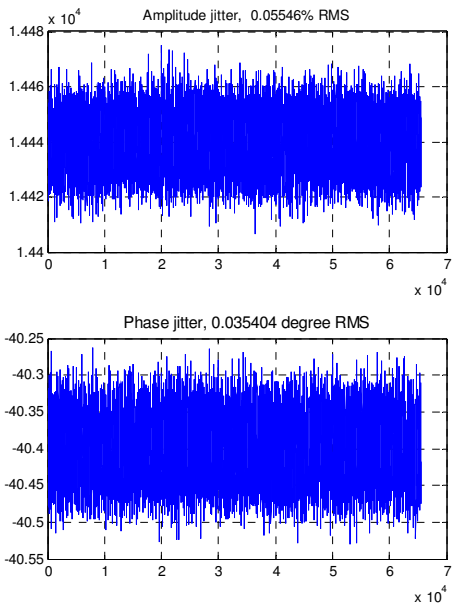

Figure 5: Amplitude and phase measurement.

High Power Test The new DLLRF was installed in the booster RF system and was connected to the high power amplifier and cavity. The system parameters were measured at high power. The group delay of the DLLRF was 2.2 µs. Rectangular and polar loops have similar bandwidth values when using similar proportional gain and integral gain values. 30 kHz bandwidth can be achieved setting high gain values.

Test with Beam After all the functionalities had been verified at high power, the DLLRF was tested with beam. An RF ramp was generated by the DLLRF and beam was successfully captured in the booster at 100 MeV and ramped to 3 GeV. The screen shot of the ramping RF cavity field on the oscilloscope and the accumulated beam is shown in Fig. 6.

CONCLUSION

A new DLLRF has been developed for Diamond Light Source 500 MHz RF systems. All major functionalities have been tested and verified. Measurements showed it achieved the specifications required. DLLRF systems will be built based on it and optimized for the booster RF cavity, storage ring superconducting RF cavities and normal conducting RF cavities. Other desirable functionalities, such as the probe blip blockage, will be developed in the future.

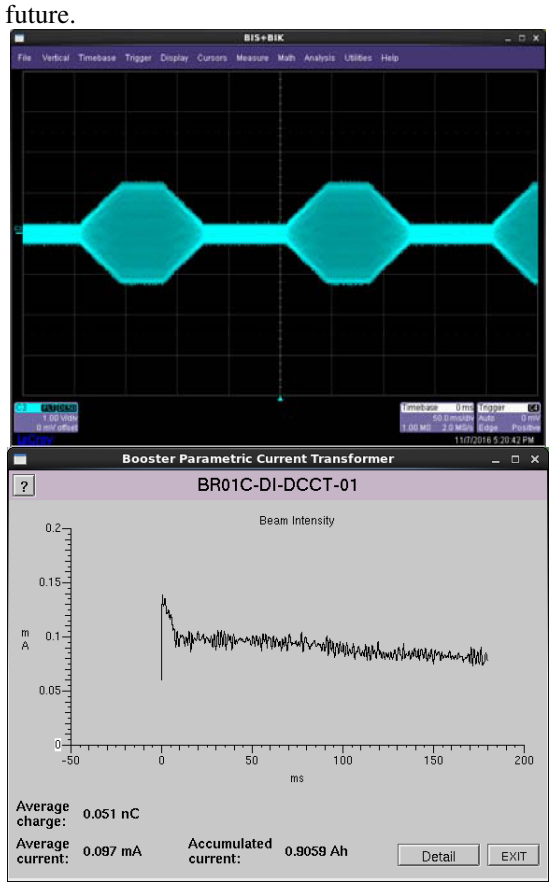

Figure 6: Beam test of the DLLRF. Upper image is an oscilloscope trace of the field in the RF cavity and lower image shows the current of the captured and accelerated beam in the booster.

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