# SUB-FEMTOSECOND JITTER ULTRA HIGH PERFORMANCE OSCILLATORS FOR ACCELERATOR TIMING

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*Abstract*

Extremely stable RF-sources are at the heart of Electron Beam Accelerators and impact beam quality and beam energy. Jitter requirements on those sources are extremely tight and linked to the quest for ever decreasing (XFEL) laser pulse length, currently in the tens of femtoseconds.

For the Pohang Accelerator Laboratory in Korea, a 2.856GHz phase-lockable oscillator with a jitter performance of 0.8fs in the offset-frequency range between 10kHz and 10MHz was developed and deployed, together with a master oscillator that supplies rubidium-stabilized 476MHz for synchronization.

Using the same technology of a *dielectric resonator oscillator* (DRO), a 3.9GHz source was developed for the European XFEL at DESY/Hamburg, achieving 0.3fs (10kHz-10MHz). Phase noise levels are down to -125dBc/Hz@1kHz and -175dBc/Hz@100kHz offset, with a noise floor of -180dBc/Hz.

The strategy of designing ultra low phase-noise (PN) oscillators with dielectric resonators is outlined, and challenges and limitations within the oscillator design, but also measurement technology are presented.


## PHASE NOISE AND JITTER

Building an oscillator requires a resonator to set the frequency and an amplifier to compensate for the resonator's losses. For low noise (low jitter) oscillators, both building blocks must be as low-noise as possible.

The famous PN-model of Leeson [1]

$$L(f_m) = 10\log\left[\frac{1}{2}\frac{FkT}{P_R}\left(\left(\frac{f_0}{2Q_L f_m}\right)^2 + 1\right)\left(\frac{f_C}{f_m} + 1\right)\right] \qquad (1)$$

relates the single sideband (SSB) PN $L$ (in dBc/Hz) as a function of the offset frequency $f_m$ around center frequency $f_0$ to four important parameters. To minimize noise, this model dictates:

- Maximize S/N by maximizing the output power of the resonator $P_R$ with respect to noise power $FkT$ (F: noise factor of amplifier).
- Maximize the loaded Q $Q_L=f_0/BW_{3dB}$ of the resonator.
- Minimize the amplifier's flicker corner frequency $f_c$.

Figure 1 shows a number of simulated PN diagrams and the influence of those four parameters. Clearly, optimising $Q_L$ is of most efficiency, as it enters (1) squared. Less obvious, the highly device technology dependent $f_c$ can have a huge impact, as it is not unusual to find GaAs devices to have 100 times higher 1/f-noise corner frequencies than their silicon counterparts.

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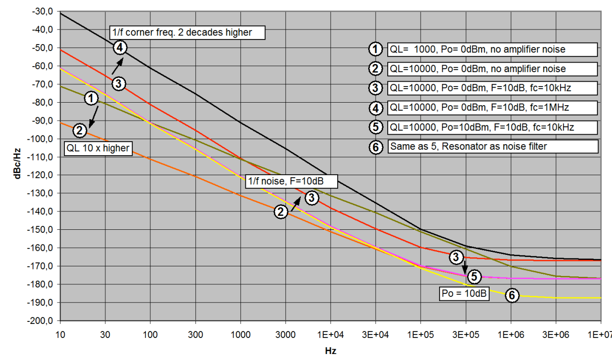


Figure 1: Oscillator PN from (1) with varying parameters.

Phase jitter of the oscillator, the measure of the output waveform zero-crossing's time deviation, is computed by integrating PN over a certain offset frequency range.

$$J = \frac{1}{2\pi f_0}\sqrt{2\int_{f_1}^{f_2} L(f_m)\,df} \qquad (2)$$

Comparing jitter numbers is therefore only meaningful, when the integration bounds are known and compare.

Typical integration intervals for this type of free-running sources are 1kHz .. 10MHz or 10kHz .. 30MHz, with the upper bound reflecting the envisaged processing bandwidth of the system. The higher $f_2$, the more advantageous is a low oscillator noise floor. With $f_2$ = 100MHz, a noise floor of -160dBc/Hz collects 7.9fs of jitter, whereas at -180dBc/Hz only 0.79 fs accumulate. Taking the lower integration bound $f_1$ to offsets below 1..10kHz is usually not mandated, as the oscillators will most likely be locked to a low-noise reference that determines PN and jitter close to the carrier.

## OSCILLATOR TOPOLOGIES

Most oscillators use the "reflection" type topology (negative resistance oscillator), e.g. [2]. This topology, albeit simple, has the drawback that a number of important parameters like resonator loading, output power and amplifier compression are tightly coupled and hard to control separately.

For narrowband sources, the topology of a transmission type oscillator (Fig. 3) gives much better control of the critical parameters, is widely used [3-5] and chosen here.

The next important design decision is, at which point to tap into the loop to extract the output power. Placing the coupler at the output of the amplifiers maximizes output power. However, taking the power from the resonator reuses this element as a filter to suppress the amplifier's broadband noise outside the resonator's passband [4,6].



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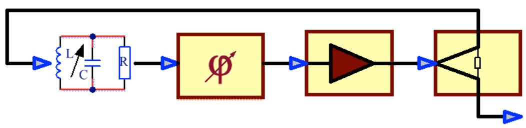
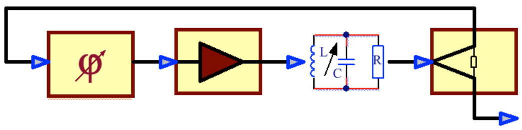
Using this topology is the key to achieving low noise floors of -180dBc/Hz and below (Fig. 1, trace 6).



(a) Power taken from the ***Amplifier***



(b) Power taken from the ***Resonator***

Figure 2: Transmission oscillator.

## OSCILLATOR OPTIMIZATION

### *Resonator Q, Unloaded / Loaded*

For single-frequency oscillators, dielectric resonators placed inside a metallic cavity offer the highest $Q$ and for the frequencies discussed here, resonators with unloaded $Q$ ($Q_U$) of 30.000 at 2.856GHz and 25.000 at 3.9GHz were obtained.

Coupling to the resonator (loading it) reduces $Q$ to $Q_L$ and [7] established that optimum coupling should occur at $S_{21}$ = -6dB, where $Q_L = 1/2\ Q_U$. This coupling factor, leading to $Q_L$ of 15.000, was used for the 2.856GHz-design.

For 3.9GHz the reasoning in [7] was questioned, as with the topology of Fig 2.(b) 2dB better PN can be obtained by looser coupling with a resonator insertion loss of 9dB. The necessary increase of amplification and output power by 3dB also increases the amplifiers output noise power by 3dB, but that increase gets suppressed by the resonator's filtering action. Despite the lower $Q_U$, with the above choice the 3.9GHz-design was also realized with a $Q_L$ of 15.000.

### *Amplifier Optimization*

The most crucial design decision in the amplifier electronics involves selection of the active device. Here, bipolar silicon transistors should be preferred to ensure low $f_c$. Also designing for high output power pays off, as it lowers the noise floor. Finally, as with all oscillator designs, the device's transition frequency should be as low as practically possible for building an amplifier with the appropriate gain.

That gain should be some dB above the losses in the loop, to accommodate variations over temperature and account for the resonator's amplitude response over the tuning range. Finally, the occurring gain compression must not lead to instabilities of the amplifier.

Low noise device biasing was added to the amplifier design, employing ultra low noise LDOs [8] in a two tier regulation scheme that virtually eliminates frequency pushing.

## ADD-ONS

No oscillator is complete without a buffer amplifier that isolates the oscillator sufficiently from the load. For both designs, double stage buffers were built, reducing pulling to < 1ppm with a fully reflecting load over all angles, while keeping the noise floor at -180dBc/Hz.

Also an ALC was added to stabilize output power to < 0.1dB, helping reduce phase drifts, due to (tuning induced) amplitude changes. A slight draw back of the ALC circuitry is some additional AM-noise at carrier offsets below 100Hz.

## CHALLENGES

### *Temperature Stability*

Figure 2 shows that frequency tuning can be done by tuning the resonator or varying the phase in the loop. Most all high performance DROs [2-5] and the designs presented here provide a mechanical coarse tuning of the resonator (some MHz) and use the phase-shifter (PS) for electronic tuning. Electronic tuning of the resonator, though possible [9], risks to degrade Q, as it involves coupling to varactor diodes that have much higher losses.

The available frequency shift from an in-loop PS, however, is confined to the resonator bandwidth (-2dB-points in this case). With a $Q_L$ of 15.000, the tuning range amounts to ±25ppm. This poses a problem, when the temperature coefficient (TC) of the resonator assembly becomes too high with respect to the targeted temperature range. On top, metallic enclosure (cavity) and dielectric resonator (puck) have different TCs with, even worse, different time responses [4,10].

With the aluminium cavity at -1ppm/K and the 2.856GHz resonators at +1.5ppm/K, both TCs cancel well enough, such that this DRO design has no problem to safely operate over a 0°C/50°C temperature range, more than adequate for the highly temperature controlled accelerator environments.

The -3ppm/K TC of the 3.9GHz resonators, however, adds to the cavity's TC and allows for just +/-6°C of temperature variation that can be compensated with the electronic tuning. As this was felt to be insufficient, a mild sort of oven was incorporated, heating and keeping the assembly at +35°C for safer operation.

As the problem of temperature drift mounts with rising $Q_L$ it will be even more pronounced at 1.3GHz, where $Q_L$ may increase to 30.000 or more, leaving 25ppm or less to be electronically compensated. Meeting this challenge either requires further oven control and thermal insulation or alternative means of electronically tuning the resonator.

### *PN Measurement*

The PN of the realized oscillators is, at most offsets, decades below the intrinsic noise of most measurement systems. Such low noise sources can only be measured using cross-correlation, where two test-channels allow the test-set's noise to be averaged out over time [11-13].

Yet, the required sources to compare the DRO against must be as low noise as possible, to not overburden the cross-correlation capabilities, bearing in mind that every 5dB of necessary test-noise reduction require a 10-fold measurement time.

PN test-sets that allow for *external* sources [11] have a clear advantage and yield the fastest measurement time, when two more oscillators with similar PN are available for use.

## RESULTS

Figure 3 shows two measurement results of the 2.856GHz DRO. The upper plot, taken with [12] and maximum measurement time (several days) still shows insufficient sensitivity between 100kHz and 1MHz, as well as artefacts around 30kHz. The lower plot, taken with [11] benefits from external reference sources (two more same-design DROs) and gives a more trustworthy result after about 40 minutes.

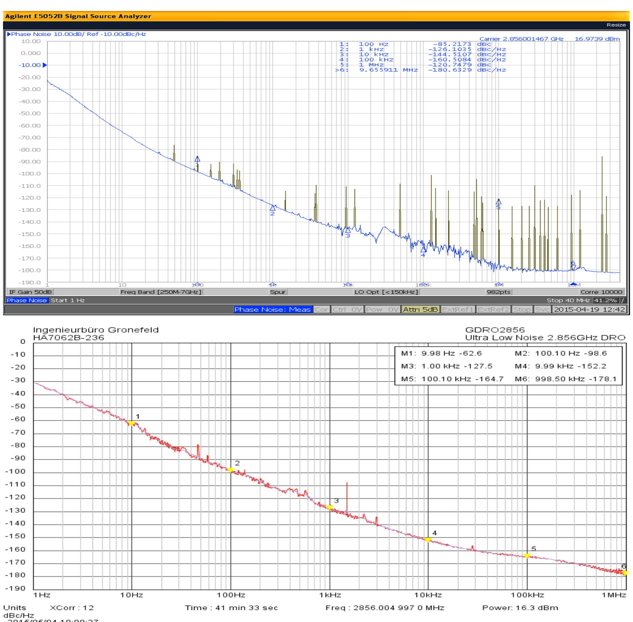



Figure 3: Phase Noise of free-running 2.856GHz DRO.

The result of the 3.9GHz design (taken with [13]) is shown in Fig. 4.

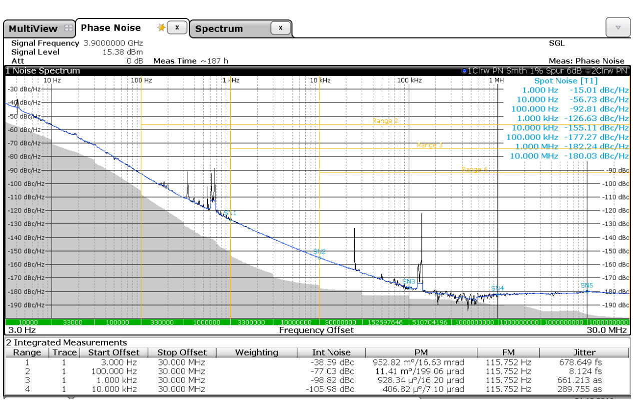



Figure 4: Phase Noise of free-running 3.9GHz DRO.

## CONCLUSION

Sub-femtosecond jitter microwave sources that rival the performance of optical oscillators were developed for two of the relevant frequencies in linear electron beam accelerators.

None of the critical design decisions taken is novel, but rather adhere to long known principals. Use of modern, low noise components and techniques, as well as careful optimisation of all building blocks was key to the achieved performance.

It should be pointed out that the resulting designs are stable and reproducible commercial products, with typical noise data not differing by more than a few dB.

## ACKNOWLEDGMENT

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