DEVELOPMENT OF A DIGITAL BEAM SIGNAL PROCESSOR TEST SYSTEM BASED ON MATLAB AND SCPI*

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Abstract

The SXFEL (Soft X-ray Free Electron Laser) and DCLS (Dalian Coherence Light Source) have been under constructions since 2015. To satisfy the huge demands of digital beam position monitor processor, we batch produced over 200 sets of DBPM processor. This paper describes a high automatic test platform based on MATLAB and SCPI, used for the device acceptance test and performance evaluation. The simulation beam signals generated by the Agilent signal source MXG N5181A, connected to a 4-way power splitter. The network control system based on the architecture of the client and server mode, integrated instruments test commands and experimental data transferred via a Mercury router. Using EPICS LabCA realized the data acquisition channel access interface. The platform has been successfully used for the Dalian Coherent Light Source (DCLS) devices acceptance testing, the noise level, crosstalk between channels, amplitude frequency response and SNR test reports automatic generation under test.

INTRODUCTION

The DBPM processor system played a vital role in beam diagnostics system. The BI group of SSRF developed a new type of DBPM processor to handle the BPM data acquisitions and the position calculations. Since 2015, DCLS and SXFEL have been under constructions, dozens of strip line BPMs and cavity BPMs are planted along the LINAC accelerators and the undulators. Under the circumstances, over 200 sets of independently developed DBPM processor have already been batched producing. In order to efficient achieve the device acceptance and evaluate the performance and stabilization of the DBPM processor, we developed an automatic test system based on MATLAB and SCPI.

One of the key challenges of the test system is to find a suitable protocol which could connect the principal computer with DUT (Device Under Test) and signal generator, in that case, we could integrate the test configure command and data acquisition command in the principal computer. We consider several general bus we could use in our system, based on easy connection and configuration consideration we choose TCP/IP protocol at last.

Both the DCLS's and the SXFEL's control system based on Experimental Physics and Industrial Control System (EPICS), so we could use labCA, which is an EPICS channel access interface for MATLAB developed by SLAC.

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PERFORMANCE CHARACTERISTICS

The DBPM processor signal front-end processing part mainly consists of radio frequency signal conditioning (RF) module and analog to digital converter (ADC) module. The pre-processing signal conditioning is used to handle the RF signal with centre frequency of 500MHz, bandwidth about 10MHz. The amplifiers and the digitally controlled attenuators could provide 60dB dynamic rang [1,3].

In order to meet all requirements for the DBPM processor. The following tests should take in the laboratory to realize the devices acceptance testing and evaluate the percision and stabilization of the DBPM processor.

Frequency Response

The DBPM processor work in the mode of RF bandpass sampling. The RF frequency of SSRF is 499.684 kHz, so the ideal working frequency of the DBPM is 500MHz, the ideal band pass section from 490MHz to 510MHz. The frequency response test set the test zone from 485MHz to 515 MHz and the step size set 0.5MHz.

SNR

ADC module realize the signal change from analog quantity to digital quantity. The conversion accuracy of ADC is crucial for the higher resolution of the DBPM processor. And signal-to-noise ratio determines the precision of DBPM processor. We focus on the RF frequency at 500MHz. In order to test the full comprehensive SNR performance at 500MHz. Both the input signal power and attenuator are changed to simulate different beam status.

Attenuation Setting Linearity Coherence

During the machine study and normal user operation, the BPM could detect a variety of signal amplitudes, in order to take full use of the ADC's significance bit, the amplifiers and the digitally controlled attenuators in the radio frequency signal conditioning module work on the acquisition signal to suit for the ADC range. Test the attenuation setting linearity coherence among four channels can check the stabilization of DBPM processor.

ARCHITECTURE

A central element of the test system is the signal generator, which should provide suitable signal to simulate the beam signal in order to test the DBPM. Since both the DBPM processor and the signal generator have the internet access, we choose TCP/IP protocol based on client/server framework to construct test platform.

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The architecture is described below. A high level overview is provided of the hardware, embedded software, and control system.

The control system for the DCLS under construction at Dalian uses the EPICS, so the DBPM embedded EPICS IOC, running Linux operation system, are dedicated devices for BPM data acquisition and process [2].

Since we choose the Agilent MXG N5181A as the signal generator, the SCPI is ideal for program-controllable instruments [4].

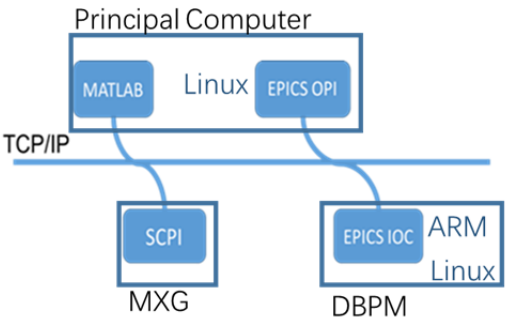

Figure 1: The overview architecture of the test system.

HARDWARE DESIGN

The hardware architecture of the system is shown below. The system consists of five main components: principal computer, interchanger, 4-way power splitter, signal generator and DBPM. The Agilent N5181A MXG signal generator output 1 channel RF signal, the signal through cable to Mini-Circuits 4-way power splitter divide into 4 channels to simulate 4 channels beam signal detected by BPM. The Mercury interchanger connect the signal generator, DBPM and principle computer by net wire.

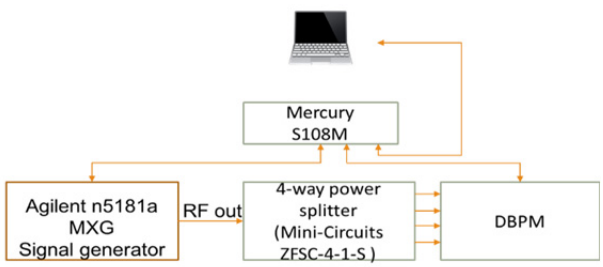

Figure 2: Hardware architecture.

SOFTWARE DESIGN

The DBPM embedded EPICS IOCs, running Linux operation system. The soft IOC has good real-time performance, portability and extensibility. DBPM IOC collects beam position data from four channels. As shown below, the EDM panel consists of two main parts: one is display windows, and the other is parameter setting and readout through EPICS IOCs.

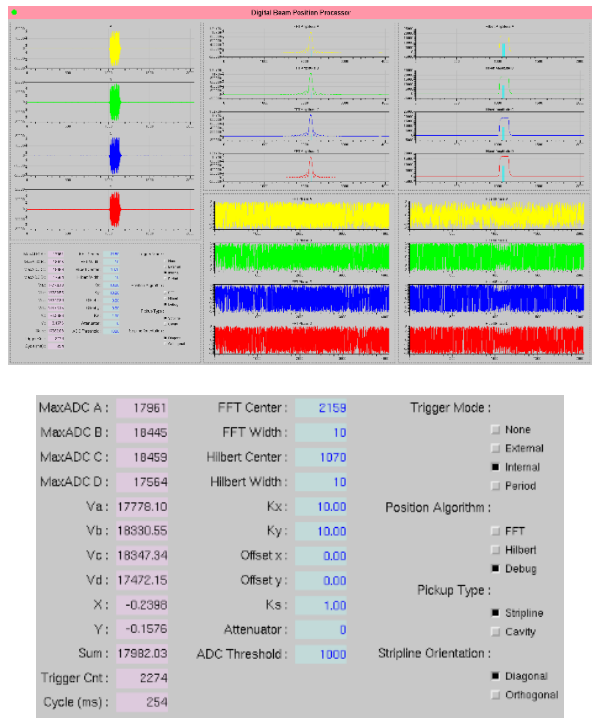

Figure 3: digital beam position processor EDM panel.

MATLAB gets PVs from DBPM processor via labCA. We designed a dedicated algorithm to realize device acceptance test and performance evaluation. The algorithm flow is shown as below.

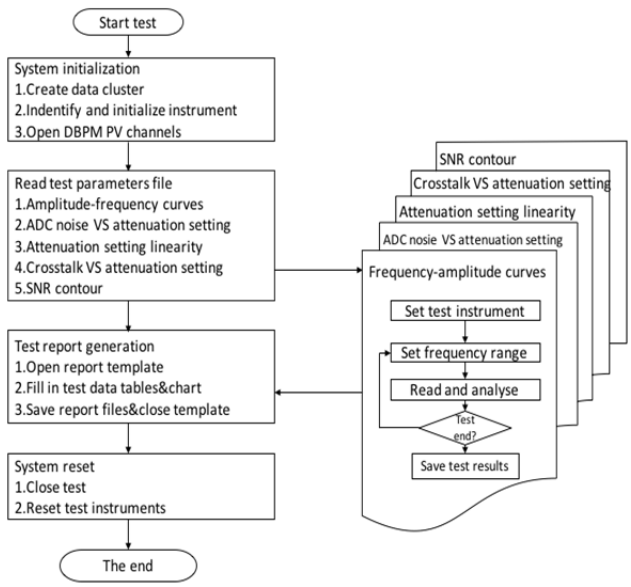

Figure 4: Algorithm flow pattern of test system.

LABORATORY TEST

Test Platform

Figure 5: photo of platform in laboratory.

The test system has already set up in the laboratory as the photo shown above. The platform followed the principal of compact.

Test Results

The test system automatic get data extraction includes four channels raw ADC data simultaneously from DBPM processor. The MATLAB could process data directly and generate the test reporter.

The platform have succeed testing over 100 sets of DBPM processor, only tiny minority has problems and has already countermand from the manufacturer. Figure 6 shows a typical performance test reporter of the DBPM processor.

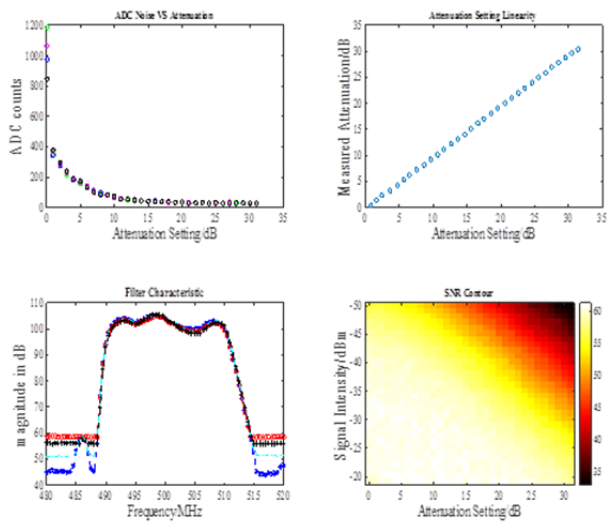

Figure 6: Test reporter of DBPM UD-BI:CBPM-DA-6

We also summarize and analyse all sets of DBPM processor in order to compare and evaluate. The results are shown in Fig. 7.

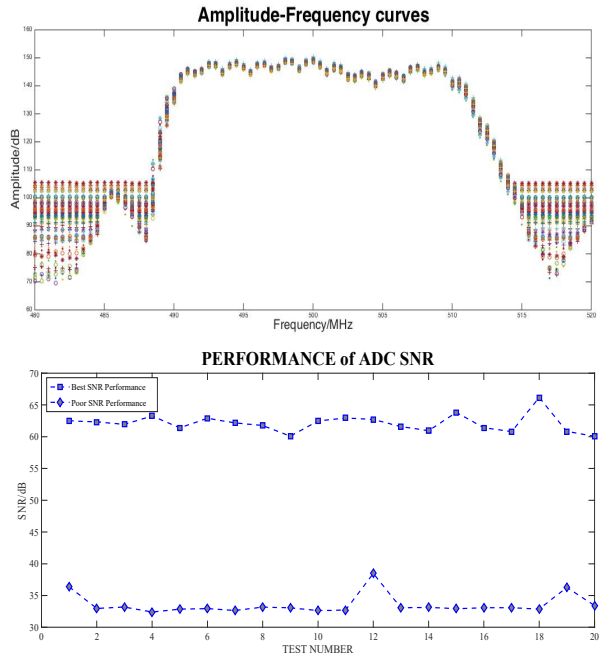

Figure 7: amplitude-frequency curves and SNR performance of 20 sets DBPM processor.

CONCLUSION

The paper has shown the DBPM processor test system in terms of hardware, firmware and software. The system is based on MATLAB and SCPI, both are widely used, so it can easily transplant in other Digital BPM processor devices, such as Libera which has been proved. Its complete integration into the EPICS based control system allows other extension applications which could be further development.

ACKNOWLEDGEMENT

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