

- ❑ Performances of accelerators are strongly dependent on the beam parameter measurement accuracy and on the capability of controlling/stabilizing those parameters (current, size/emittance, position, losses...):
 - ✓ **Common methods have emerged for beam diagnostics and control at accelerator facilities.**

- ❑ Efficiency of the instrumentation and feedback algorithms relies on electronics:
 - Performances
 - Availability
 - Management
 - Maintenance
- ✓ **Standard modular crates are extensively used for acquisition electronics**

- ❑ Scope of this presentation is voluntary **limited to**:
 - **Diagnostics** even if other systems have to be considered for a global implementation of electronics standards (RF, control, interlock systems,...).
 - **Non exhaustive selection of commonly used systems and methods.**

- ❑ Beam control methods, associated instrumentation and requirements for the electronics
 - Beam current
 - Beam size
 - Beam position

- ❑ Electronic standards presentation
 - NIM
 - VME
 - Compact-PCI
 - μ TCA.4

- ❑ Electronic standards in particle accelerator instrumentation
 - Survey
 - Considerations for a global implementation

Beam Control Methods and associated Instrumentation

- ❑ Charge/Current monitoring is based either on:
 - Shot by shot measurement (linear accelerator)
 - Averaged measurement over several turns (circular machines)

- ❑ Measurement of interest:
 - The **bunch charge/current**
 - The **total current**
 - The **purity**: electron ratio between a (filled) high current bunch and its (empty) following bucket.

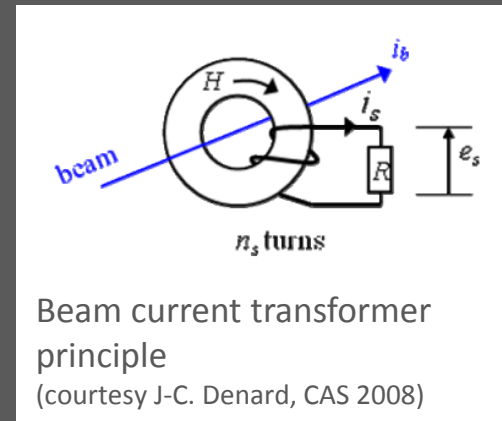
- ❑ Wide range of beam charge /current monitors:
 - Destructive
 - Faraday cup
 - Non destructive
 - Wall current monitors
 - **Current transformers**
 - **Pick-up monitors**
 - **Photodiodes**
 - Cavity monitors

□ Current transformers:

- Based on transformer principle.
- Declined on three main types:
 - Fast Current Transformer (FCT):
High frequency measurement -> bunch shape
 - Integrating Current Transformers (ICT):
Medium frequency measurement -> bunch charge
 - Direct-Current Current Transformer (DCCT)
DC measurement -> beam current
- Dedicated frontend electronics provides an analog voltage that is proportional to the beam current.

□ Acquisition electronics

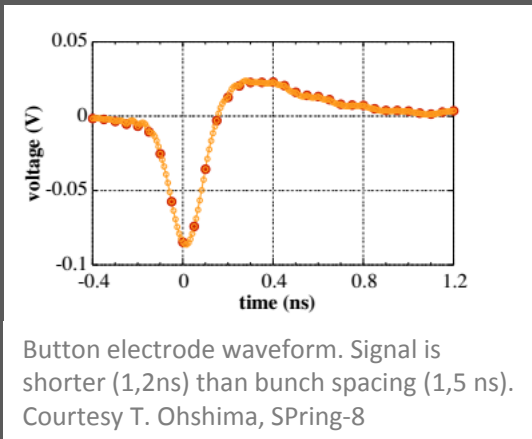
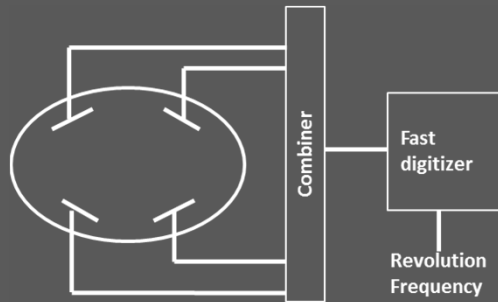
- Varies from:
 - High bandwidth/sampling rate oscilloscopes for FCT
 - Usual 16 bits, 1 Msamples/s ADCs for ICT
 - High resolution (24 bits) multimeters for DCCT (important for accurate lifetime measurements)
- Available in the main electronic standards.



☐ Relative bunch current measurements:

▪ **Pickup current monitors**

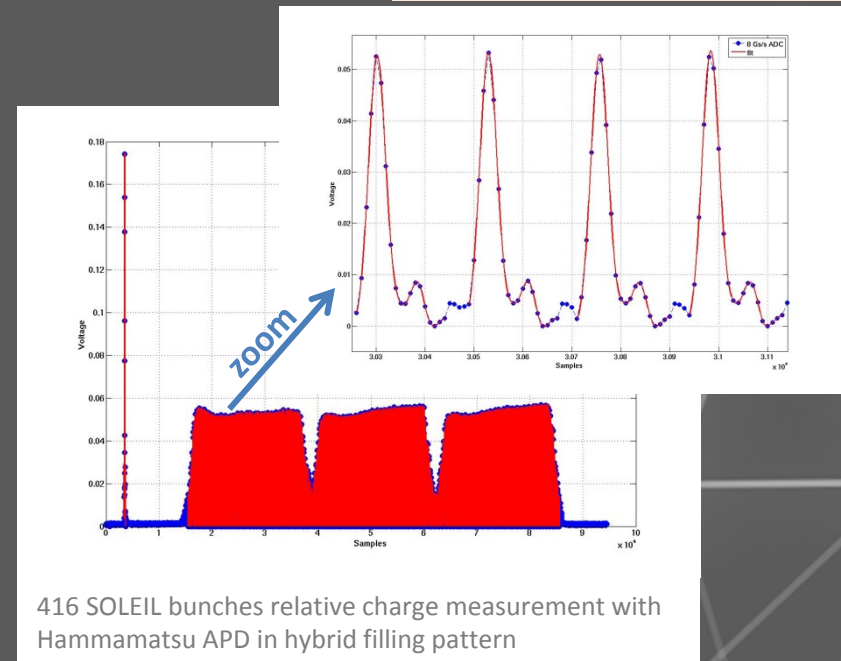
- Sum of the 4 button BPM signals



▪ **Photodiodes based current monitors:**

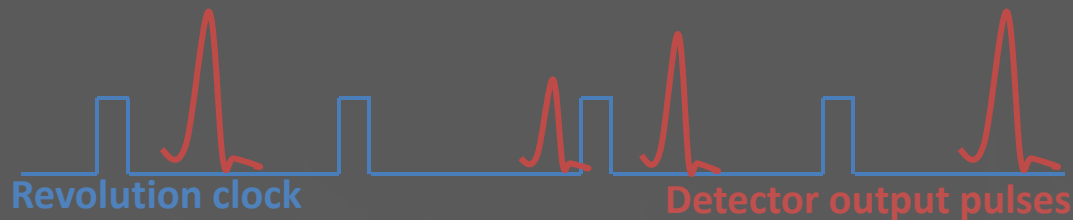
- Avalanche photodiode (APD)
- Synchrotron radiation (visible)

B. Kalantari, V. Schlott, T. Korhonen,
“Bunch Pattern Control in Top-Up Mode
at the Swiss Light Source”, EPAC 2004.



- ✓ Acquisition with a high bandwidth (\sim GHz) and high sampling rate (20 GS/s) **oscilloscope**. Additional fitting algorithm required.

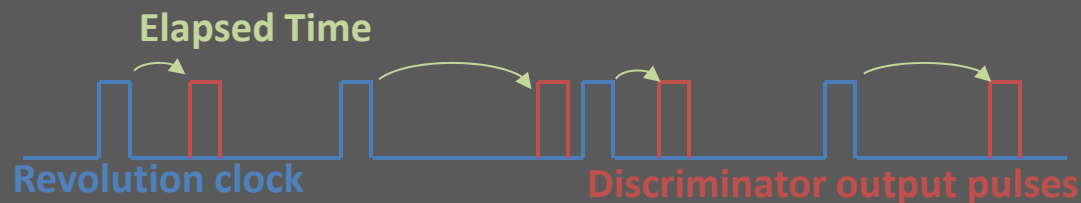
- ❑ Bunch **purity** measurement:
 - Electron ratio between a (filled) high current bunch and its (empty) following bucket.
 - Time resolved experiments on light sources may be sensitive to 10^9 purity
 - Required dynamic range can not be addressed by classical detector and acquisition methods.
- ❑ Statistical method called **Time Correlated Single Photon Counting (TCSPC)** is applied:
 - Detector (X-ray APD, PMT, SPAD) is configured (Bias voltage) to produce (only) one pulse (from one photon) per turn: **each photon has the same probability to be detected** whatever the electron/bunch it originates



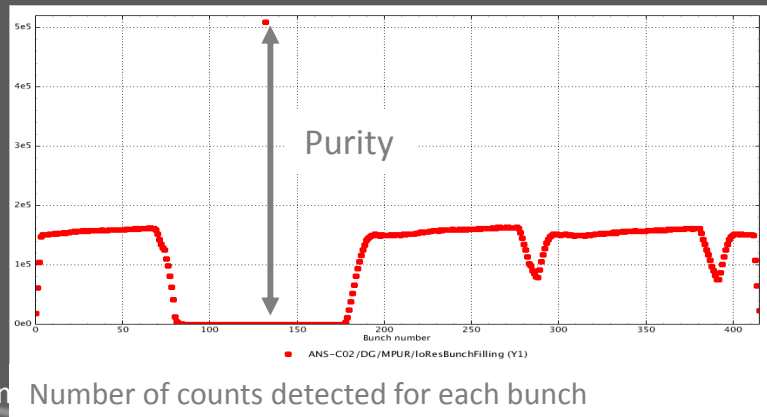
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 - Pulse sorting depending on their arrival time with respect to reference clock
 - > **Time to Digital Converter (TDC)**



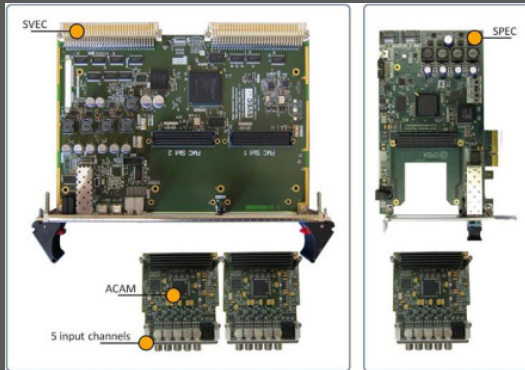
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 - Pulse sorting depending on their arrival time with respect to reference clock -> **Time to Digital Converter (TDC)**
 - Dynamic range depends only on integration time



Beam Charge Monitors (purity)

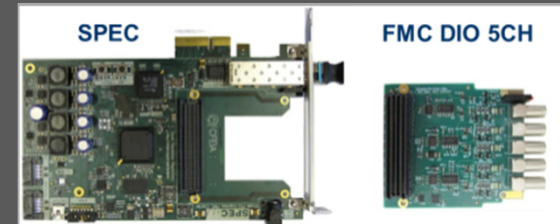
TCSPC Implementation examples:

- TDC on mezzanine card on VME or PCIe carrier:



TDC chip on FMC
Available on CERN, Open Hardware repository

- TDC on PCIe card:



TDC IP in the FPGA (SOLEIL)
Available on CERN Open Hardware repository

- TDC on CompactPCI card:



Commercial product
from
Keysight

- Standalone TCSPC module:



Commercial product from Picoquant

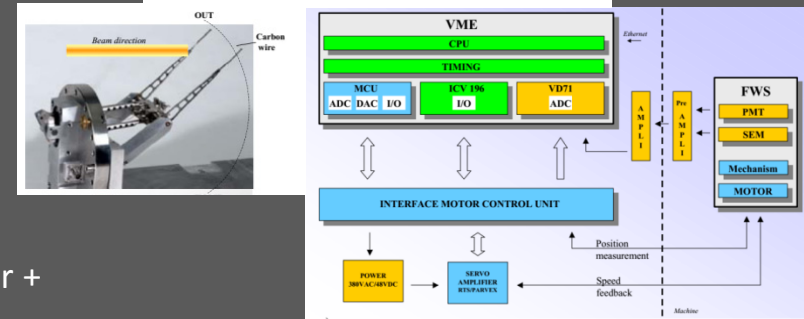
Beam Size Measurement:

- **One dimensional sampling** (beam profile measurement)
 - Wire scanner:
 - Secondary electron emission -> **ADCs**
 - Secondary particle emission -> Scintillator + Photomultiplier + **ADC**
 - Ionization profile monitors
 - Acquisition of signal collected on electrodes -> **ADCs**
 - Acquisition of image (**camera**) from multichannel plate + screen

- **Two dimensional sampling** (2D imaging)
 - Radiative screens (OTR, scintillator...)
 - Synchrotron radiation
 - Visible light: double slit interferometry
 - X-rays : pinhole cameras

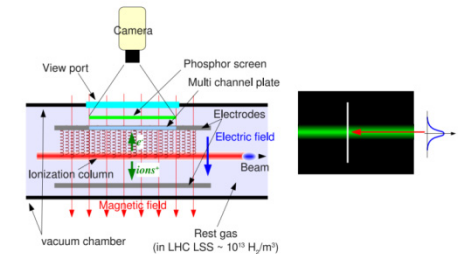
✓ **CCD/CMOS cameras: Gigabit Ethernet standard is now very popular: easy integration into any accelerator control system.**

CERN PS Booster Fast Wire Scanner



Courtesy S. Burger (S. Burger, et al. "The PS Booster Fast Wire Scanner", DIPAC 2003).

Ionization Profile Monitor example (CERN)



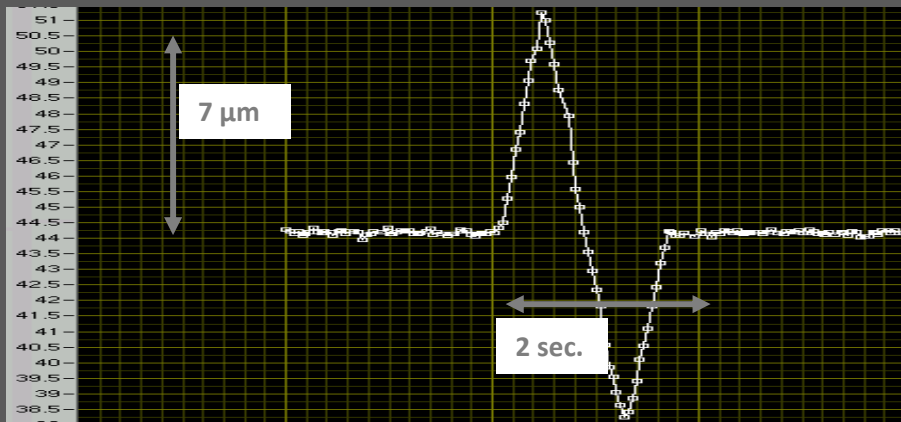
Courtesy E. Bravin (Transverse Beam Profiles, CAS 2008)



Gigabit Ethernet camera (Basler scout example)

□ Beam Size Control:

- Generally a slow process (few seconds)
 - Algorithm embedded in high level applications
- In synchrotron light sources
 - Compensate for coupling variation caused by integrated skew gradient from insertion devices
 - Acting on skew-quadrupoles
 - Keeping the vertical emittance constant
 - Varying the pure vertical dispersion amplitude
 - Requirement for faster switching configuration of IDs in the future



Example of beam size perturbation when switching electromagnetic insertion device main power supply at SOLEIL (feedback OFF).

- ✓ High speed (100 Hz) image processing using higher performance implementation (FPGA) to be considered

- ❑ Beam position stability is a key parameter for:
 - Collider: to maximize the luminosity / safety (LHC)
 - Light sources:
 - To stabilize the photon beam size
 - Keep the overlap between electron beam and emitted radiation (FEL)

- ❑ Very tight requirement, generally set at 10% of beam size/divergence, but some kind of experiments are actually more sensitive.
 - Sub $\mu\text{metre}/\mu\text{rad}$ stability is required over a large frequency range (DC- few kHz)

- ❑ Beam position monitors rely on **stable/low-noise electronics**

- ❑ Automatic beam position **feedback methods have been developed** and improved.
 - Global orbit/trajectory feedback:
 - Uses all BPM and correctors
 - Repetition rate from few Hz to 10 kHz
 - Intra bunch feedback:
 - Uses few BPMs and kickers
 - Repetition rate up to 500 MHz

- ❑ A large number of beam position monitor types:
 - Shoebox
 - Stripline/buttons
 - Cavity BPM

- ❑ BPM Electronics
 - Different possible processing scheme (broad-band, log-ratio, narrowband)
 - **High level of complexity:**
 - Combination of analog and digital processing
 - Filtering
 - Down mixing
 - Parallel treatment (up to 4 channels)
 - Automatic gain control
 - High-speed/ high resolution digitization (typically ~100 MHz/14 bits)
 - Multiple data flow possible (single pass, turn by turn, low latency short term averaged data @~10 kHz, long term averaged data@~10 Hz)
 - **Synchronization capabilities**
 - High number of I/Os (RF signals, timing, data distribution, interlock, post-mortem...)
 - **Tight requirements on stability:**
 - Low noise
 - Low drifts (multiplexing / Pilot Tone for permanent calibration)

Implementation examples:

- A large number of BPM electronics run on **standalone crates**:
 - Difficulties to find commercially available standardized electronics boards that fit the BPMs requirements
 - Easier collaboration between institutes since no more electronics standard dependent.
 - For industrials: bigger market for a custom development.
 - Interface with the control system based on Ethernet fieldbus



NSLS2 BPM (courtesy O. Singh)



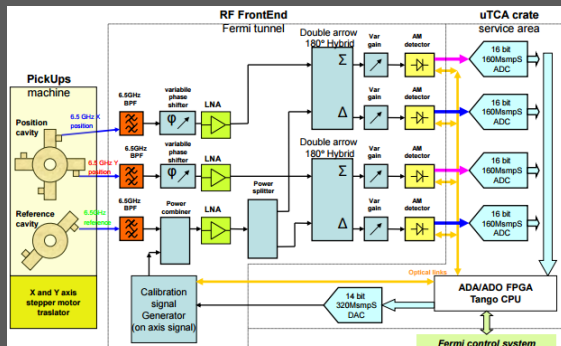
Libera module (courtesy Instrumentation Technologies)



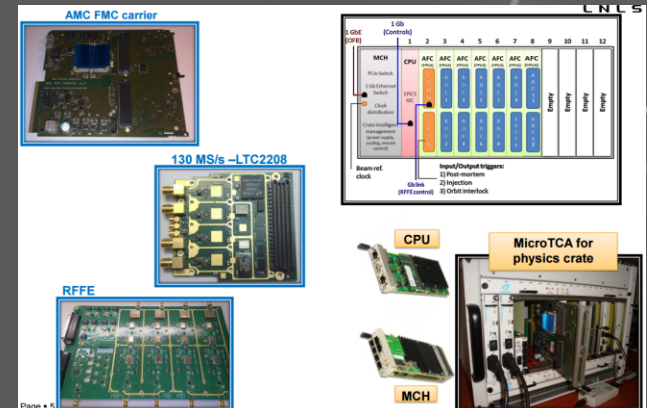
XFEL/PSI Modular BPM Unit for both button and cavity BPMs. (courtesy B. Keil)

hybrid solutions also exist:

- RF Front-end as standalone electronics
- ADCs and digital processing in standardized crates



FERMI@Elettra cBPM system (courtesy R. De Monte)



SIRIUS BPM Electronics (courtesy S. Marques)

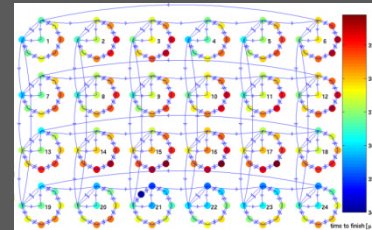
Global Orbit feedback:

- Relies on the BPM response matrix (+SVD inversion method)
- All BPM data have to be distributed to feedback processor(s)
 - Real time communication using Multi-Gigabit SFP transceivers connected to FPGA:
 - Reflective memory
 - Serial point to point links (GbE or custom protocol)
- Processing run on DSP/FPGA boards.
 - May be hosted in a standard electronics crates.
 - Requires high enough bus speed for monitoring purposes (position and set points): ~640 kbits/sec/BPM at 10 kHz

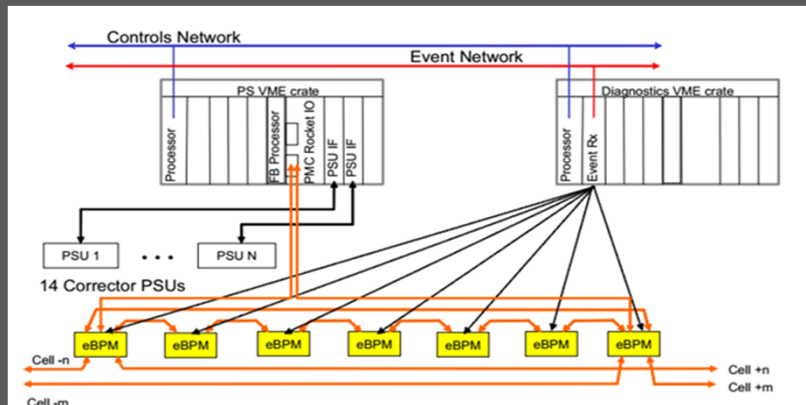
$$\begin{matrix} \text{Inversed Response Matrix} \\ \left[\begin{array}{c} \text{row 1} \\ \text{row 2} \\ \vdots \\ \text{row M-1} \\ \text{row M} \end{array} \right] \\ M \times N \end{matrix} \times \begin{matrix} \text{Orbit Error} \\ \left[\begin{array}{c} \Delta U_{\text{BPM}1} \\ \Delta U_{\text{BPM}2} \\ \vdots \\ \Delta U_{\text{BPM}N-1} \\ \Delta U_{\text{BPM}N} \end{array} \right] \\ N \times 1 \end{matrix} = \begin{matrix} \text{Correctors Delta} \\ \left[\begin{array}{c} \Delta I_{\text{CORR}1} \\ \Delta I_{\text{CORR}2} \\ \vdots \\ \Delta I_{\text{CORR}M-1} \\ \Delta I_{\text{CORR}M} \end{array} \right] \\ M \times 1 \end{matrix}$$



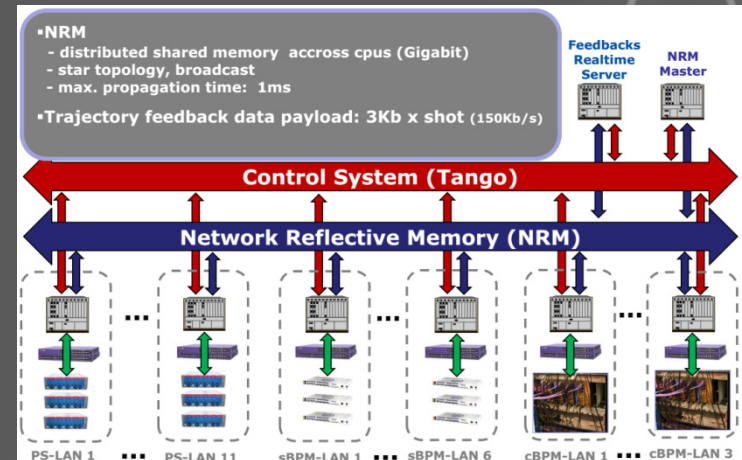
Example of Diamond FMC SFP module (MicroResearch).



Diamond BPM data distribution network for FOFB (courtesy I. Uzun)



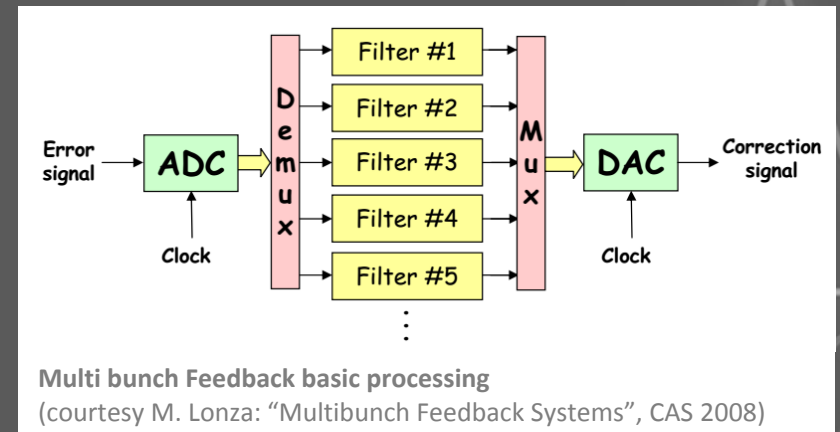
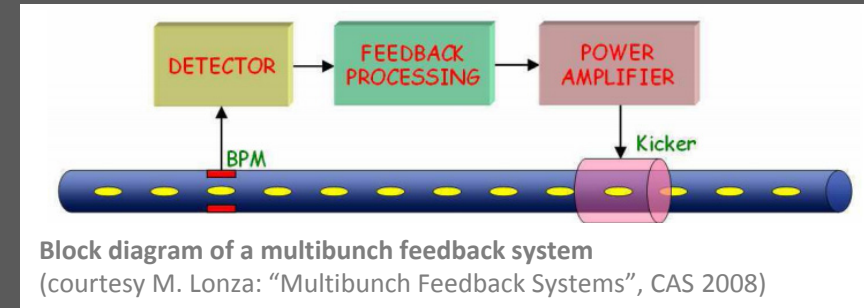
Point to point communication at Diamond Light source. Processing is implemented in VME racks (courtesy I. Uzun)



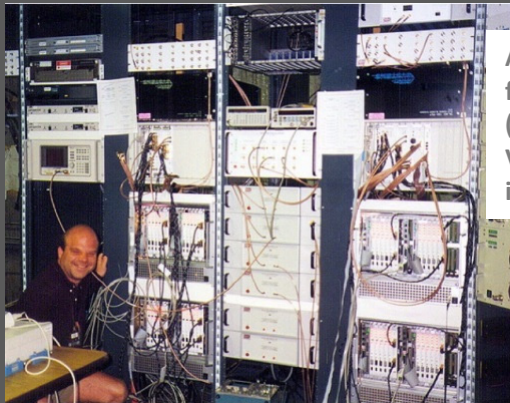
Reflective memory based implementation. and FERMI@Elettra trajectory feedback network layout (courtesy G. Gaio)

Multi bunch feedback:

- Coupled-bunch instabilities damping in storage rings
- Acts on each bunch individually (typically 500 MHz repetition rate)
- Use of one BPM and one kicker/cavity per plane
- Analog frontend:
 - BPM button balance to suppress closed orbit offset
- Digital Electronics
 - Real time low latency digital systems
 - Typically 500 MS/s -12/14 bits ADC/DAC



- ❑ Multi bunch feedback system implementations:
 - Integrated in **standard crates**:

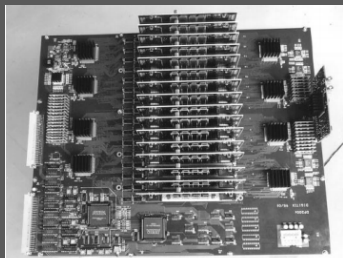


ALS/PEP-II/DAΦNE longitudinal feedback
(Adopted at SPEAR, Bessy II and PLS)
VXI (ADCs and DACs) and VME (DSPs)
implementation



Elettra (SLS) longitudinal and transverse processors:
VME implementation

- As **standalone electronics**:



KEKB longitudinal and transverse feedback system



Spring-8 transverse feedback processor (adopted by TLS, KEK-Photon-Factory and SOLEIL)



ESRF, Diamond, Alba, NSRRCC, CLS, ANKA, ALS longitudinal/transverse feedback processor (Libera bunch by bunch by Instrumentation Technologies)



DAΦNE (transverse), KEK-Photon-Factory (longitudinal), ALS, DELTA, Indus-2, NSLSII, SPEAR3 feedback processor (iGp by Dimtel)

ELECTRONIC standards

□ Electronic standards

- Define modular electronic crates
 - Mechanical shape
 - Backplane connectors
 - Protocols for data transfer between cards on the backplane bus
- Host electronic cards used for:
 - Data acquisition
 - Signal processing
 - Timing system
- Provide the power-supply voltages (12V ,5V ,3V...)
- Share common resources (CPU, PSU, Fans)

- Widely used in large accelerator facilities

□ Pros:

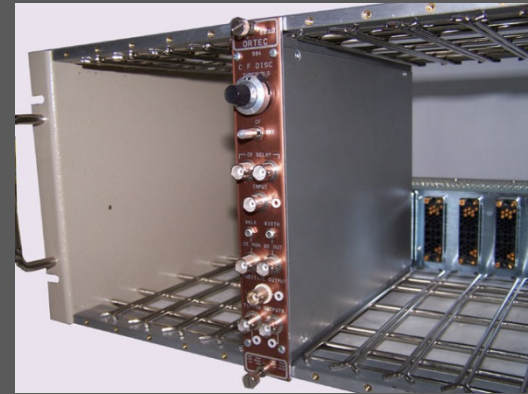
- Integration
- Maintenance and long term support
- Management and control
- Availability from industry
- Standard boards: CPU, ADC, power supplies.
- Wider user community (possible collaborations)
- Reliability (if mature): long MTBF
- Modularity: small MTTR
- Redundancy (if supported by the standard)
- Cost

□ Cons:

- Volume and cost for small application
- Performances (bandwidth, bus speed sometimes limited for older standards)

□ NIM: Nuclear Instrument Module

- Created in 1969
- First and simplest standard
- Define:
 - Modules mechanical dimensions
 - Connector: 42 pins used for power supplies and logic
 - Negative current based logic (also called fast logic standard)
 - 0= 0A
 - 1= 16 mA (-0,8V into 50 ohms termination)
- Old fashioned, but still alive
 - Logic definition well adapted for fast signals
 - > Discriminators
 - Programmable logic with embedded FPGA



□ Pros:

- Simplicity

□ Cons:

- No communication between module through the backplane
- Phased out

❑ VME: Versa Module Europa bus

- Combination of:
 - the **Versa-bus specification** (started in 1979 by Motorola engineers and quickly adopted by other company).
 - **Euro-Card format**
- Officially standardized as ANSI/IEEE 1014 in 1987. Developed and supported by the VME International Trade Association (**VITA**)
- Multi-processor bus, communication priority being controlled by the arbiter module in slot 1
 - Asynchronous signaling scheme (not tied to the timing of a bus clock)
 - DMA transfer
 - Interruption mechanism
- **Bus (parallel) speed** limited to 40 MB/s in its first definition but more recent evolutions (VME64 , VME64X, VME320) offer improved bus speed, up to **320 MB/s**.



 Pros:

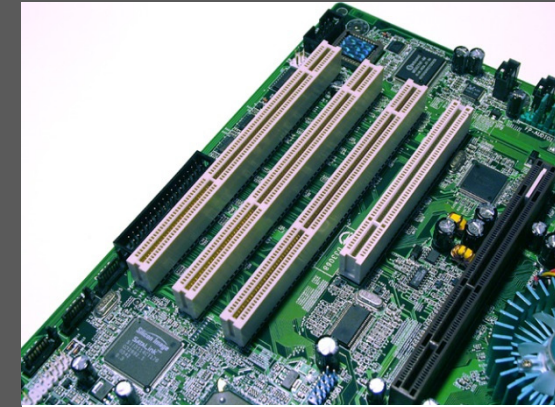
- Huge market (massive use in military and aerospace industry)
- Wide community of users and developers
- The most widespread standard in accelerator community at the moment
- Large range of COTS available modules (ADC, TDC...)
- Long term support still good
- Mechanical robustness

 Cons:

- Bus speed can be a limitation for diagnostic high bandwidth applications
- Unclear lifetime (coming to the end of its life?)
- Innovative products are difficult or impossible to source

□ PCI: Peripheral Component Interconnect

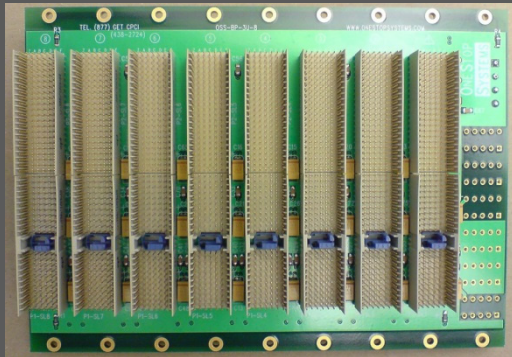
- Standard PC peripheral bus
- Originally developed by Intel, standardized in 1991
- Synchronous bus:
 - Data and addresses are time multiplexed on the same lines
 - Maximum bus speed from 132 MB/s (for 32 bits, 33 MHz version) up to 528 MB/s (64 bits, 66 MHz)
 - Limited physical length of the bus (4 slots) since electrical reflection on unterminated lines are exploited to increase the wavefront voltage.
- 3,3V or 5V power supply (keying connectors to prevent any wrong insertion)



PC motherboard with 64 bits /3,3V and 32 bits/5V PCI
(courtesy M. Joos: "Modular Electronics")

❑ CompactPCI: compact Peripheral Component Interconnect

- Standard for PCI-based industrial computers
- Form Factor based on standard Eurocard dimension (like VME)
- Extended bus length with 8 available slots
- Hot swapping is mechanically possible (power is applied before bus signals at insertion thanks to staged pins)



❑ Pros:

- Mass market product with widely used and debugged drivers
- Cost effective solution
- No timing/synchronization signal distribution (addressed by PXI standard)
- CompactPCI serial declination replace old parallel bus by point to point serial links (PCIe, STA,...)

❑ Cons:

- No real time operating system
- Unclear lifetime

□ μ TCA (MTCA) basics

- Emerged from the ATCA (Advanced Telecommunication Computing Architecture) standard, established by/for telecommunication industry.
- Simplification of ATCA by suppressing big carrier boards. μ TCA allows direct connection of AMC (Advanced Mezzanine Cards)-functional modules to the backplane.
- Scalable form factor: up to 12 slot single or double size
- **Crate management** (Intelligent Platform Management Interface)
- **Redundancy** (power supplies, fans)
- Point to point serial lanes on the backplane for **high speed data transfer** (>400 MB/s on 4 lanes PCIe)

P. Gessler et al: "Next Generation Electronics based on μ TCA for Beam-Diagnostics at FLASH and XFEL," DIPAC2011 proceedings, Hamburg, Germany.



5 slots single size



5 slots double size

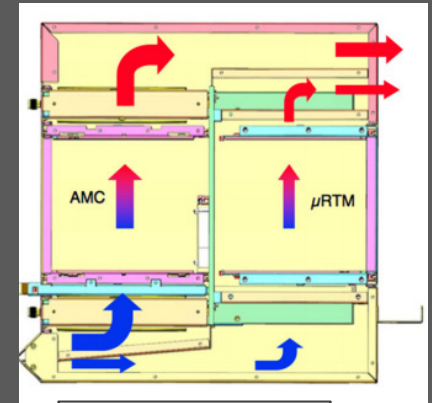


12 slots double size

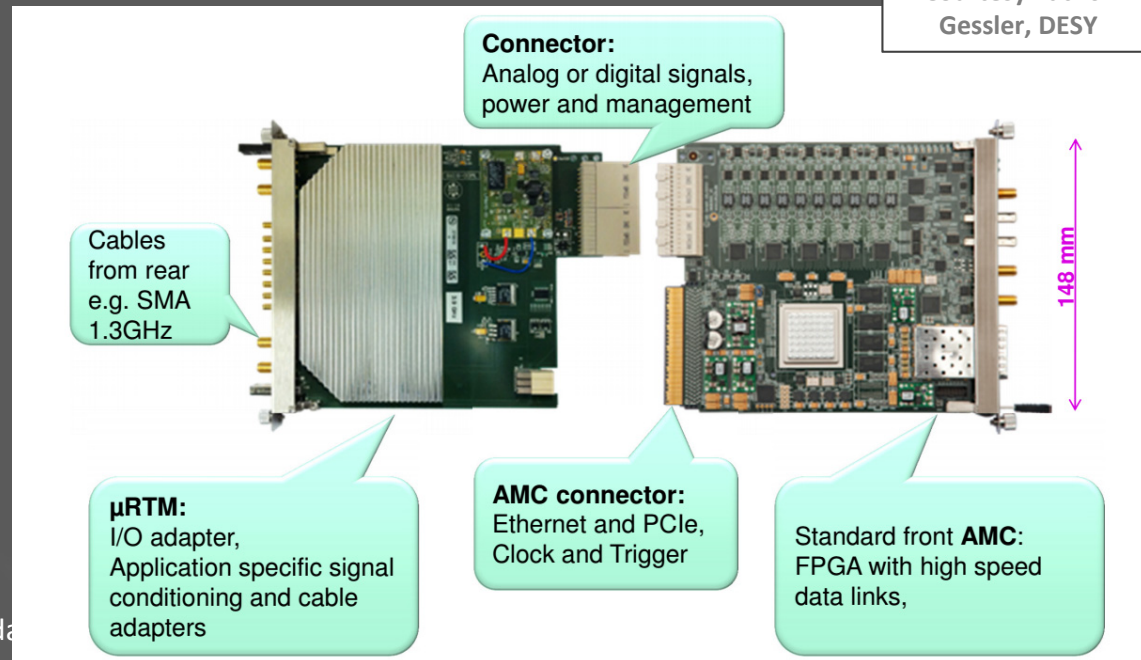
Courtesy Patrick Gessler, DESY

□ μTCA.4

- Specifications from xTCA for Physics working group (2009):
 - 6 labs (SLAC, DESY, FNAL, IHEP, IPFN, ITER) and 38 industrials
- Distribution on the backplane of timing signals (clocks, triggers, interlocks...)
- Definition of the **Rear Transition Modules (RTMs)**
 - Signal conditioning and conversion
 - Application specific I/Os

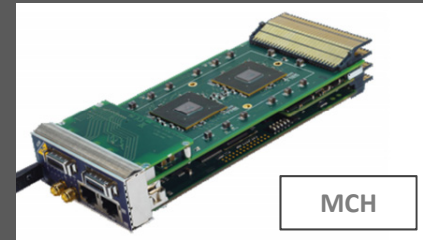


Courtesy Patrick Gessler, DESY



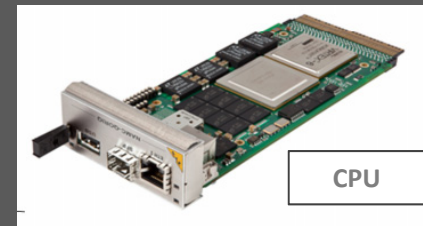
□ μTCA.4 common AMC modules

- Management Carrier Hub (MCH)
 - Management (cooling, power-supply, hot-swap, remote access, alarms...)
 - Switch for PCIe and Gb Ethernet
 - Clock distribution
- Central Processing Unit (optional)
 - Data concentration and additional processing
 - Archiving on hard disk
 - Ethernet connection to control system
- Timing modules
- ADCs
- Signal processing boards
- Multi purpose boards (I/Os + FPGA) to be combined with specialized RTM or FMC boards



MCH

Courtesy Patrick Gessler, DESY



CPU



Timing module

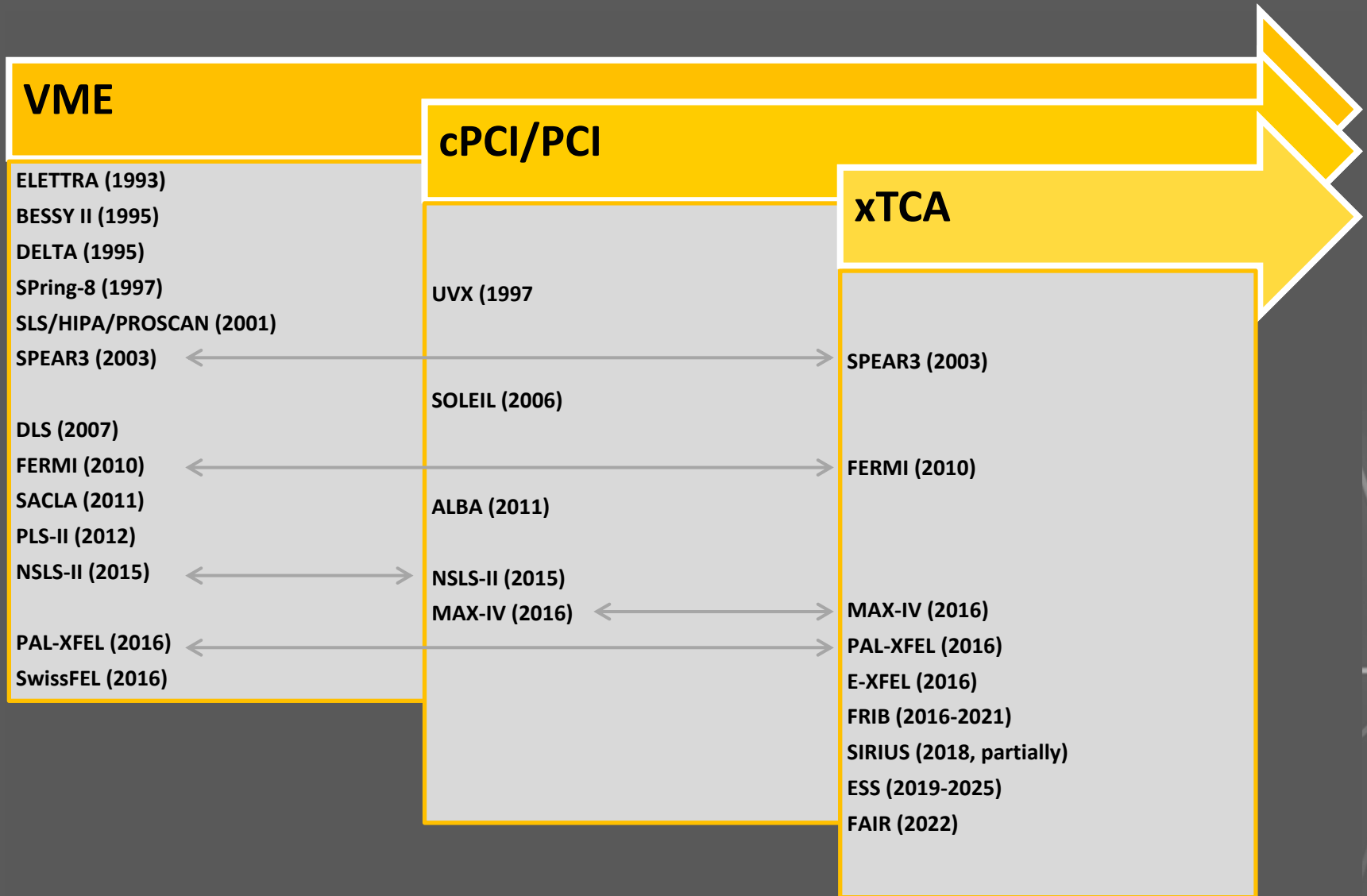
□ Pros:

- Adapted for physics instrumentation
- Fully open standard
- High performances
 - ✓ Fast data transfer
 - ✓ Low jitter timing distribution included
 - ✓ High analog signal processing (differential links only)
- Management capabilities
- High availability (redundancy, hot-swapping)
- COTS solutions already available on the market
- Open hardware μTCA designs already available in the CERN Open Hardware Repository
- User community is increasing.

□ Cons:

- Still a young standard
- Lack of references or manufacturers for specific (compact) crates
- Some incompatibilities between manufacturers (IPMI)
- Level of expertise for its implementation
- Expensive

Electronic standards in particle accelerator instrumentation



- ❑ Some considerations before choosing a standard:
 - Which systems plan to use the standard? Standardization of hardware platforms for different systems are possible? This can considerably improve reliability and long term support needed.
 - Who will provide **the long term support** for the standard platform? **Resources available to design** the systems (hardware, firmware and software).
 - **Cost**
 - **Redundancy** (none, partial or full) and **reliability**
 - **Synchronization** –Timing needs for clock and trigger distribution. Some standards does not provide real time synchronization.
 - **Data bandwidth** – Data transmission between the CPU and FPGA needed by the systems.
 - **Data distribution** between crates and **latency**. For some application it is really important to consider this (fast orbit feedback example)

- ❑ **Global implementation in accelerator laboratories**
 - Pretty rare to have all electronics following same standard
 - Custom standalone electronics (BPMs, feedback processors)
 - μ TCA.4
 - A good candidate for high performance system
 - Oversized for simpler (low speed, low performance) systems?

Conclusion

- ❑ Beam instrumentation and beam control systems follows commonly used methods that rely on
 - Large diversity of electronics
 - Signal conditioning
 - Acquisition
 - Signal processing
- ❑ Standard electronics (crates and modules):
 - Massive use at accelerator laboratories and in particular for instrumentation (VME, PCI/cPCI and μ TCA.4)
 - Eases integration, implementation and maintenance of the systems
- ❑ Global implementation:
 - Direct impact on long term support, MTBF and MTTR
 - Difficult to achieve
 - Compromise using 2 standards (high and low performance systems)?

- Many thanks to all the people that contributed:
 - Dr Changbum Kim (PAL-XFEL)
 - Seunghwan Shin and Sung-Chul Kim (PLS-II)
 - Tobias Hoffman (GSI)
 - Guenther Rehm and Mark Heron (DLS)
 - Om Singh and Yong Hu (NSLS-II)
 - Jeff Corbett and Jim Sebek (SPEAR3)
 - Yuji Otake (SACLA, Spring-8)
 - Robert Lindvall (MAX-IV)
 - Gero Kube and Dirk Noelle (PETRA-III, E-XFEL)
 - Steve Lidia (FRIB)
 - Jens Kuszynski (BESSY-II)
 - Marco Lonza and Mario Ferianis (ELETTRA, FERMI)
 - Peter Hartmann (DELTA)
 - Rafael Baron, Andreas Jansson (ESS)
 - Kees Scheidt (ESRF)
 - Boris Keil (PSI)
 - Yves-Marie Abiven (SOLEIL)

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