NSLS-II ACTIVE INTERLOCK SYSTEM AND POST-MORTEM ARCHITECTURE*

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Abstract

The NSLS-II at Brookhaven National Laboratory (BNL) started the user beam service in early 2015, and is currently operating 13 of the insertion device (ID) and beamlines as well as constructing new beamlines. The fast machine protection consists of an active interlock system (AIS), beam position monitor (BPM), cell controller (CCs) and front-end (FE) systems. The AIS measures the electron beam envelop and the dumps the beam by turning off RF system, and then the diagnostic system provides the post-mortem data for an analysis of which system caused the beam dump and the machine status analysis. NSLS-II post-mortem system involves AIS, CCs, BPMs, radio frequency system (RFs), power supply systems (PSs) as well as the timing system. This paper describes the AIS architecture and PM performance for NSLS-II safe operations.

INTRODUCTION

NSLS-II storage ring (SR) completed commissioning in 2014 [1-2], and started operation and user beam service in 2015. In 2016, up to 16 insertion devices were installed as well as the user service with two superconducting RF cavity and 250 mA stored beam current. The active interlock system is one of the major machine protection systems from the synchrotron radiation. The main purpose of AIS is to protect the insertion device vacuum chamber and the storage ring vacuum chamber from mis-steered synchrotron radiations from IDs and Dipole magnets radiation. The required active interlock insertion device (AI-ID) system response time is maximum < 1 ms, because through 1 ms duration damping wiggler (DW) aluminum vacuum chamber will increase the surface temperature to 100 C at 1.5 mrad vertical angles. For the storage ring bending magnet protection, which is called the active interlock bending magnet (AI-BM), the response time is 10 ms. Allowance envelop defined for protecting the device and configured offset is xy=+/-0.5 mm, and the angle is xy=+/- 0.25 mrad. This paper will present the AIS hardware configuration, FPGA internal functions, global PM hardware configuration and internal timing diagrams. NSLS-II operation status and the future plan.

SYSTEM DESCRIPTION

NSLS-II AIS showed robust and stable performance during operation, and lots of flexibilities for implementing machine protection from the synchrotron radiation and critical machine faults. One of the benefits is the real-time offset/angle calculation, and all of the decision engines are located at the central FPGA core, which is called C31. The AIS hardware layout is shown in Fig.1, and more details of the system and each device regarding characteristics and functions are described in [1-2].

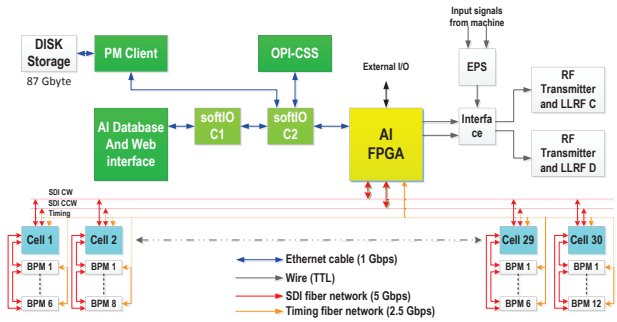

Figure 1: Layout of the active interlock system for NSLS-II fast machine protection (Details of hardware configuration presented at [1]).

Table 1 shows the numbers of installed devices and the communication speeds. Total 30 of Cell controllers are involved in the fast orbit feedback and global BPMs packet communication.

Table 1: Installed System Units

Device	Quantity	Communication
RF-BPM	180	Fibre 5 Gbps
ID-BPM	25	Fibre 5 Gbps
Cell controller	30	Fibre 5 Gbps
AI	1	Fibre 5 Gbps
FE PLC	16	Ethernet 100 Mbps

FPGA Internal Block Diagram

Fig.2 shows an AIS FPGA function blocks for the data handling and calculation. It is designed by Verilog hardware description language and modular concept. Microblaze CPU 32-bit soft-code is used for the system management and TCP/IP communication with EPICS IOC.

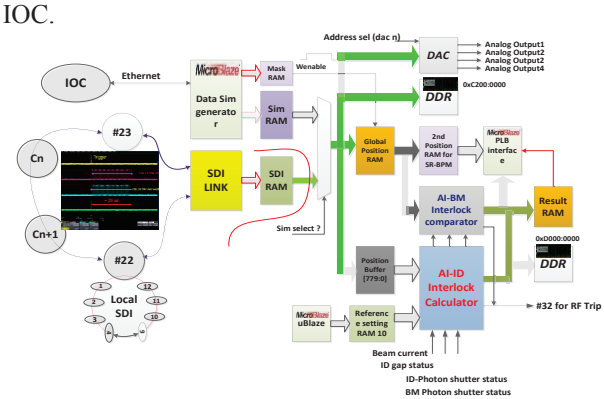

Figure 2: FPGA internal functional diagram.

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PM Trigger Structure

PM trigger and the data capturing time are synchronized for the entire storage ring system during beam dump as shown Fig. 3. The AIS generates a global PM trigger signal and PM reset signal that are distributed through the EVG timing system. EVG assigned two event codes for PM: one for a trigger event, and another for reset trigger event. Post Mortem data are stored in hardware ddr-3 memory and used to provide diagnostics for failure analysis and event analysis. Table 2 shows each system file size and sampling rate and the time it takes by PM client software when beam dump.

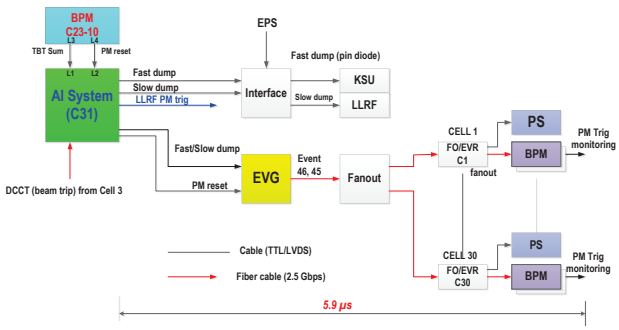
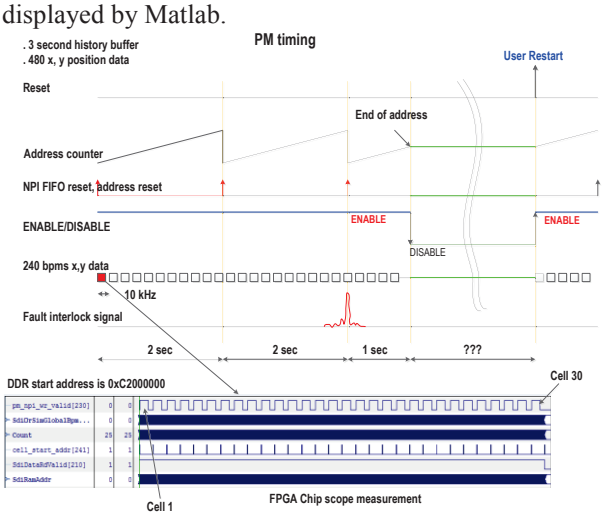


Figure 3: Diagram of the global PM configuration (Total latency is 5.9 μs).

Table 2: PM File Size from Client Computer Every Trip

Device	Size(Mbyte)	Time sec (fs)
AI	31.7	2 (10 kHz)
BPM-TBT	82.6	0.086 (378kHz)
Cell controller	57.6	3 (10 kHz)
Power supply	794	10 (10 kHz)
RF	272	0.25(4 MHz)

AIS PM waveform implemented total 3 seconds 10 kHz data saved to DDR-3 memory. Each cell has eight BPMs cells with total 240 PVs available in 30 cells. Single waveform size is described in table 2. Fig.4 shows timing diagram of the PM logic and real PM waveforms displayed by Matlab.



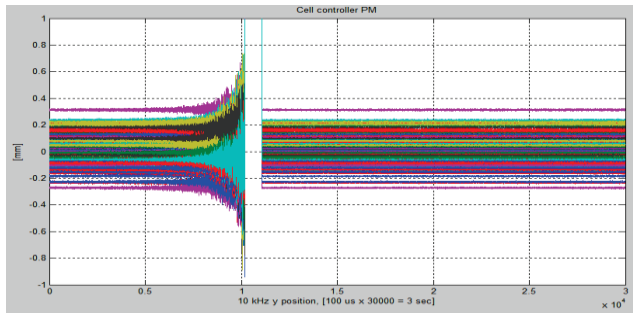


Figure 4: PM trigger timing and 10 kHz waveform captured waveform: (upper) FPGA implemented timing (bottom) PM FA waveform read using the Matlab plot.

AI FPGA also implemented archiving PM waveform during beam dump, and even when serial data interface (SDI) glitch. Here are PM trigger conditions and distribute event through timing system:

- AI-BM/AI-ID dump
- External device failures
- Global communication glitch detected

The fail-safe function is added to protect the system from unexpected faults condition.

- AIS Timing trigger error
- Cell controller timing error
- BPM fault condition (PLL unlock and ADC saturation, ID bpm, and BM bpm)
- PLC heartbeat status fault (1 Hz)
- DCCT system fault
- DCCT PLC heartbeat status (5 Hz)

If the timing system fails at any points in the AIS (BPM, Cell controller or Cell 31) data sent out on the SDI link is frozen. At each cell controller, this can be detected. If the local, BPM, SDI link fails to update the cell controller, it will send a fault condition to cell 31 and activate the interlock. If the global SDI communication link fails, the Cell 31 controller will detect error status and cause beam dump by the AIS. Also, the control room alarm indicates this failure for the reminder to operators.

OPERATION

During the commissioning period, we found out several different fault types such as RF failure Power supply failure, BPM failure (saturation), SDI communication glitch as well as equipment failures. The most serious fault is SDI glitch because this signal is unexpected condition and FOFB feedback caused short, and big (~ 100 μm) spike this problem caused just a few times during commissioning. We continued observing this kind of faults during operation. AI system has SDI data glitch ignoring function which means that if a single cycle point jumps to a sudden value, AI system assumes that it is a glitch, if two consecutive cycle's data is out of the free defined range, it is considered a real beam motion. During the machine study, we have an unexpected fault status like a glitch pattern. For example, it is possible that during injection the RF system-caused unstable condition beam motion which is frequently a single pulse out of

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range. Fig.5 shows 10 kHz x and y position closed orbit waveform with beam current 234 mA. Fig.6 shows AI system total status page for monitoring machine status. Fig. 7 shows aligned RF, BPM data based on PM waveform for investigating each system.

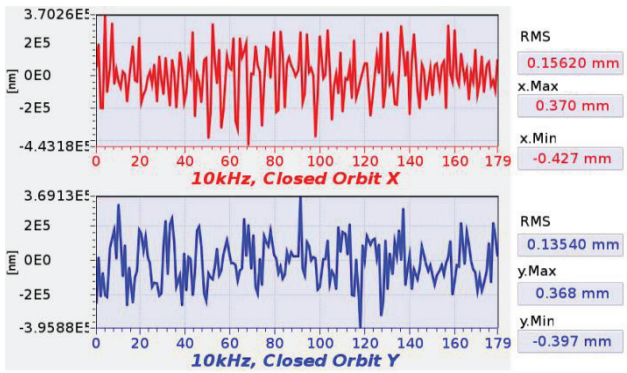

Figure 5: 10 kHz closed orbit (Top-off, beam current 234 mA, Life time 9.47h, Injection efficacy 94.5%)

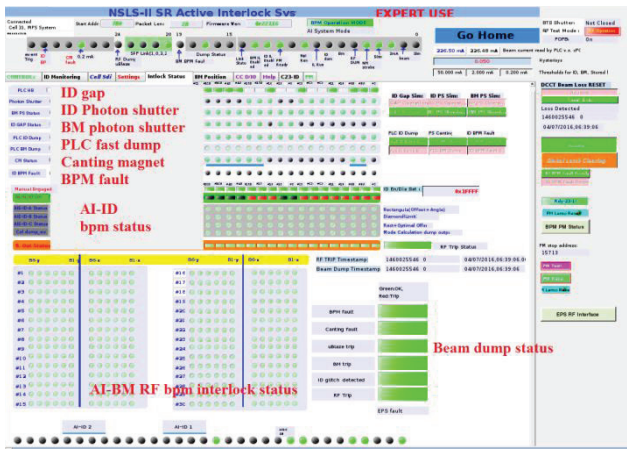

Figure 6: AI system expert page for monitoring all of the AI system status monitoring.

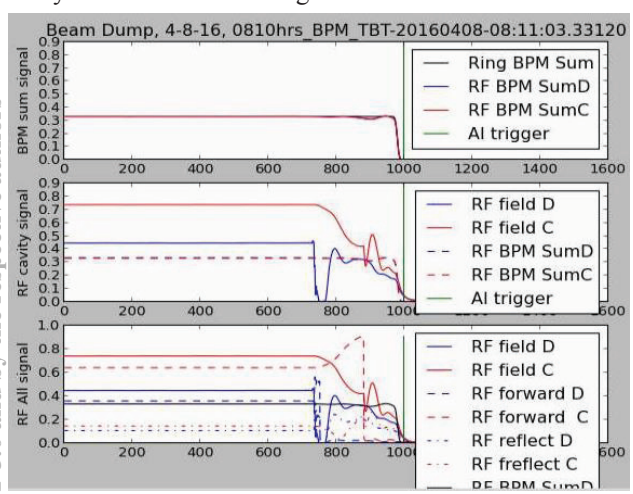

Figure 7: PM waveforms align during beam dump (Beam dump caused before AI trigger it means the first source is external system).

Beam Dump Sources

During the operation, we learned and experienced about beam dump status. There are several different types of beam dump sources. First, AIS internal error caused beam dump, especially the SDI glitch was detected. Second, the RF system faults caused beam dump, which has happened more frequently since the beginning of 2016, after 2nd SRF cavity was installed and served operation beam current is 250 mA. During the operation, we observed RF system instability and power line noise from the beam. Third, the EPS detected machine fault status such as water flow and IDs system error. Fourth, BPM and cell controller hardware included timing and PLL failures as well as ADC saturation. Lastly, Power supply faults caused kicking beam and AI system calculated out of the envelope and dumped beam.

Future Plan

We consider a new AI system based on Zynq-based development, which is capable of more advanced functions for NSLS-II control system.

CONCLUSION

In 2016, NSLS-II is operating 13 beam lines for user service and will continue constructing more than 60 beamlines until 2020. During operation since 2015, we found several unexpected issues and upgraded the firmware several times case by case. The system is works stable. One of the problems was on the global SDI single cycle glitch. We added a single cycle glitch ignoring function, and it works stably since then. The 250 mA beam operation has shown that was an AI system works stable as design requirement and fail-safe function working well. One of useful functions is PM, which works well and is very helpful for each system diagnostics. We will increase beam current to 400 mA, and AI system will be much more important for machine protection from the synchrotron radiation.

ACKNOWLEDGMENT

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[2] S. Seletskiy *et al.*, "Commissioning of Active Interlock System for NSLS II Storage Ring", TUPMA057, in *Proc. of IPAC15*.