# **DEVELOPMENT OF PAL-XFEL MAGNET POWER SUPPLY \***

K. H. Park<sup>#</sup>, S. H. Jeong, Y. G. Jung, D. E. Kim, H. S. Suh, H. G. Lee, S. B. Lee, B.G. Oh, W. S. Choi and I. S. Ko, PAL, POSTECH, Pohang, Korea

## Abstract

All magnets and magnet power supplies (MPS) for PAL-XFEL had been installed at the XFEL site. The MPSs have been testing with the installed magnets. The total number of assembled MPSs was amounted to 624. The 391 MPSs among them were for corrector magnets. The design configurations of the corrector MPS were explained. Various performance examinations were carried out to confirm weather them satisfied the specifications such as short term stability, linearity, repeatability so on. The test results of the MPSs for corrector magnets were also described here.

# **INTRODUCTION**

This PAL-XFEL project aims at the generation of X-ray FEL radiation in the range of 0.1 to 10 nm for users. The machine consists of 10 GeV linear accelerator and hard and soft X-ray undulator beamlines [1]. The PAL-XFEL was in commissioning mode now after all equipment had been installed.

The total 624 of magnet power supplies (MPS) were installed at the linear accelerator, beam transfer line and undulator section. The 391 among them were corrector power supplies (CPS) that were divided into four groups by the output current, output voltage and required stability. The four CPSs were assembled in a 3 U shelf. Two of them were paired to share the Ethernet and AC power. Two pairs were completely isolated not to interfere each other. The performances of all CPSs were examined at the company. After installation, CPSs have been operating mode and go smoothly now without any critical problems.

This paper describes some design schemes that was implemented into the CPS. And this paper showed some performance test results of the CPSs.

# SYSTEM CONFIGURATION

The CPS has requirements of comparatively low current and voltage limitation up to 15 A and 12 V. The Fig. 1 showed the shelf of the assembled CPSs. Two CPSs were paired to consider that the corrector magnet was designed to have both vertical and horizontal coils in a magnetic core generally. A paired CPS shared the one UC5282 board. The four MPSs were assembled in a shelf of 3 U height. There were no connections between pair of CPSs completely not to affect each other while operation. A fan shelf unit of 1 U was assembled under the CPS shelf for air cooling. Four vacuum fluorescent displays were assembled on the front panel which has 2 lines by 16 characters. It displayed the output current, voltage and the other status of the CPS. The 8 LEDs were showed the

\*Work supported by Ministry of Science, ICT & Future Planning #pkh@postech.ac.kr

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simple status of the CPS. A BNC per each CPS was fabricated on the front panel, which was the buffered output signal of the DCCT for easy maintenance. And a console port, RS232, and an Ethernet port were on the front panel. A name plate per each CPS was mounted on the upper side of front panel for easy discrimination of the CPS while maintenance.



Figure 1: Block diagram of the magnet power supply.

The Fig. 2 showed the interfaces among devices of the CPS. The peripherals for the VFD, UC5282, console and EEPROM were connected to the DSP through the SPI, SCIs and multichannel buffered serial port (McBSP), respectively. There was a FPGA Spartan3 XC3S1200E from Xilinx. All ADC chips were connected to the FPGA through the SPI. The FPGA was interfaced with the DSP by the external interface by the 16-bit address and data bus, respectively. The DSP got the ADC data by the 25 KHz rate, which was the same as the switching frequency of the FET. The basic parameters such as the proportional gain and integral gain were written into the EEPROM. This was interfaced to DSP through the McBSP.



Figure 2: Peripheral interfaces among devices of the CPS.

A DCCT of CT-13-LP, PCB mount type, from the CAEN ELS was adapted for the sensing the output current. The temperature coefficient of the DCCT was less than 2 ppm  $^{\circ}$ C and non-linearity was also less than 5 ppm, respectively. The output current of the DCCT was converted to voltage by the high precision foil resistor from

the VISHAY. The temperature coefficient of the resister was ±2.0 ppm/°C from -55 °C to 125 °C. It showed the lowest resistance change about the 25 °C which was operating temperature of the MPS at the gallery.

The DSP board was fabricated a DSP. FPGA and some ADC chips. The DSP TMS320F28335 from TI Co was adapted to control the overall power supply system. It has six high resolution PWM outputs with 150ps micro edge position which is the absolutely required function to archive the ~10 ppm output stability for the CPS [2]. Three ADCs were assembled in the DSP board to convert the output current, output voltage and DC link voltage, respectively. The AD7767 from the Analog Device was adapted for those signal conversion. It is 24-Bit resolution, oversampled SAR analogue-to-digital converter [3]. It sampled the signal at 1 MHz rate, decimated to eight and sent to the DSP at a rate of 25 KHz. By taking oversampling method, it can reduce the noise energy in the There was another ADC for sensing the signal. temperatures of a heat sink and a DC link power supply.

The logic circuits of the interlock signals such as over current, over output voltage, under link voltage etc. were implemented. All external interlock signals, from machine protection system and personal safety system, were isolated by the CPC1907B, optically coupled solid state relay. If interlock was occurred, its state was displayed on the monitor screen and latched until handled by the operator and logged into the file by the MPS CSS.

The power board was fabricated with the four FETs, gate driver, LC filter and DCCT as in the figure 3. Four FETs were mounted to single heat sink. Gate drivers were photocouplers, HCPL-316J, which has driving current capability up to 2.5 A. The isolated DC voltage for the each gate driver was supplied by the small switching power supplies.



Figure 3: Power board. It included FETs, gate driver, output filter and DCCT.

The simulation for the output filter was carried out to confirm its frequency responses using the PSPICE. The first pole was located about 1 KHz and its cut off frequency was about 2 KHz. The major noise component was coming from the switching frequency. The simulation showed that the switching frequency component of 25 KHz was attenuated to -60 dB, which was reasonably small. The filter section was shown around the middle section in the figure 3. The equivalent output filter circuits were shown in the Fig. 4. It consisted of two stages of LC-damped filters [4].



Figure 4: Equivalent output filter circuits (upper) and its frequency responses (down).

#### EXPERIMENTAL RESULTS

An external DCCT of a MACC150 premium from HITEC was set up to measure the output current precisely. A DVM HP3458A was used to convert the output current to digital. The load magnets for MPS performance test was used the de-installed magnet from the PLS which has both similar inductance and resistance. And the other instruments were included in the test facility such as temperature sensors, oscilloscope, mega ohm tester etc.

Short term stability of the CPS was measured for 30 minutes. It satisfied the required specification of 10 ppmrms at its full output current. Minus full power also met the specification. Long term stability for eight hours was also measured. It showed less than 30 ppm-pp.



The repeatability of the MPS was measured. The current was set from 1 A to 12 A with five times repeat. It showed

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Figure 6: Test result of the repeatability at the full current.

The linearity of the CPS was examined with the external DCCT. The figure 7 showed the differences between set current and measured one. It were less than 20 ppm-rms in the full range from -12 A to 12 A.



Figure 7: Current difference between set and read-back.

Output voltage at the full current was measured as in the figure 8. It was about 200 mV which was within the specification. This voltage was heavily relying on the characteristics of the output filter.



Figure 8: Measured output voltage ripple at the full output current. It was about 200 mV.

Current profile for the demagnetization process was shown in the figure 9. Its current was decreased 10 % at each turns for ten times. The period was able to change for the different inductances of the magnets in order to optimize the working time. And the current amplitude was also variable that could be set by the MMI depending on the nominal operation current. This function was implemented into the DSP.



Figure 9: Demagnetizing current waveform. This function was implemented in the DSP.

The others tests such as interlock, zero-cross response, line voltage regulation, step response and etc. were also carried out before installation.

### CONCLUSIONS

This paper described the bipolar power supply for the XFEL corrector magnet. The installation of all CPSs was finished. After installation, the function and performance of the CPSs were examined again. The short term stability for 30 minutes was less than 10 ppm-pp, which was satisfied the required specification. The repeatability of the CPS was also tested, and it also showed less than 10 ppm. The linearity of the CPS was about 20 ppm-rms. And other functions of the CPS such as zero-cross response, line voltage regulation, step response etc. were tested. And found that those showed good responses. The output voltage was about 200 mV at the full current. The demagnetizing function also worked well. All MPSs were in the operation mode controlled by the beam dynamics group now.

#### REFERENCES

- Heung-Sik Kang, et al., "Current Status of PAL-XFEL Project", IPAC2013, Shanghai, May 2013, WEODB103, p.2074(2013)
- [2] Texas Instruments.,www.ti.com
- [3] Analog Co.,www.analog.com
- [4] WALTER F.PRAEG,"A high Current Low-Pass Filter for Magnet Power Supplies", IEEE Trans. On Electronics and Control Instrumentation, Vol. IECI-17, No.1, February 1970.

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