STUDY OF DIGITAL QUENCH DETECTION SYSTEM BASED ON SYSTEM-ON-CHIP TECHNOLOGY

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Abstract

Quench detection system is a key component of the quench protection system for superconducting magnets. According to operating experience of the quench protection system for BEPCII interaction region superconducting magnets and study in depth on the development process of System-on-Chip, we are establishing a set of digital quench detection system with high integration density and favourable portability by integrating IP cores, custom modules and developing embedded software on one piece of FPGA chip (Cyclone V SX SoC). The main components of this system are: 1.Hard processor system based-on ARM Cortex-A9 architecture integrated with embedded operating system (Linux).2.Floating point DSP based-on soft IP core.3.Function Module Portion designed for different functions such as communicating with front end ADC, timing control, etc. This paper introduces the research progress of the system.

INTRODUCTION

Quench detection system is an important support system for safe operation of the interaction region (IR) superconducting magnets in BEPCII. The one now running on BEPCII is introduced from BNL laboratory, U.S.A, which is designed for RHIC accelerator first [1]. The system is a cluster chain distributed system that is suitable for superconducting magnets with complicated structure in interaction region of BEPCII.

According to actual operation requirements of BEPCII and disadvantage of the old system that some devices are out of date and density of integration is very low, the research group have already developed a set of upgraded digital quench detection system. The whole system consisted of data acquisition cards, ADC and timing control card, DSP card, front-end computer running a real time operating system (Vxworks), upper monitor computer and database server. Figure 1 shows the system structure.

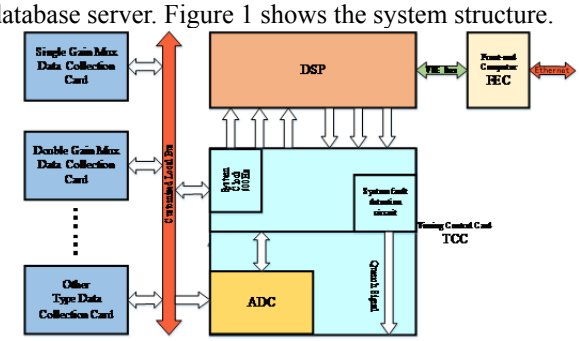

Figure 1: Former system structure.

The system includes several devices such as ADC/TCC card, DSP and single board computer. Cards communicate through different bus or port. In order to improve system integration degree and simplify communication mechanism between each module, we decide to develop a new quench detection system based-on System-on-Chip (SoC) technology to achieve all the functions of TCC card, DSP card and front-end computer of the original framework.

SYSTEM STRUCTURE

Figure 2 shows the frame of new system. The new quench detection system is developed following the universal hardware and software collaborative design method, to achieve top-down system functional division. The system is built on one chip through the way of integrating Intellectual Property (IP) cores, developing custom modules and designing corresponding embedded software.

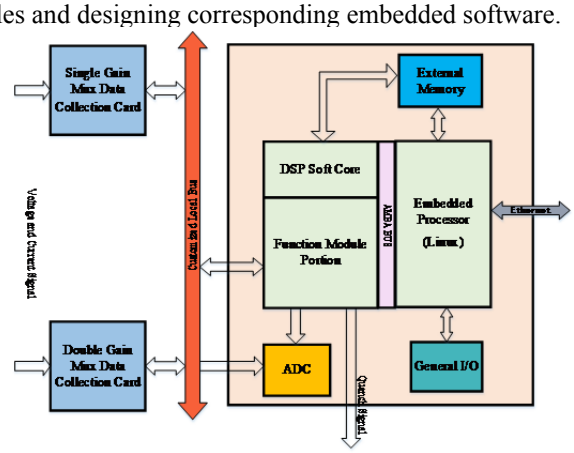

Figure 2: New system structure.

The quench detection working process is shown below:

Under the management of front-end data processing and timing controlling modules (also called Function Module Portion), the input signals are converted into digital signals in a certain sequence and stored in cache area. The DSP core reads the data and writes it into its memory, and then processes it according to the predetermined logic. When quench is determined, the DSP core sends quench alarm instructions to the front-end modules to decode the instructions to TTL signal and send it to quench protection circuit. Heartbeat as an inspection signal, which is generated by the software of the embedded processor, is transferred to each on-chip module by DSP core and monitored by Fault State Detection Module in Function Module Portion. Once the signal is disappeared, it's the sign that system software or hardware fault happens, the system will trigger quench protection circuit to implement protection operation. The Embedded Processor visits shared memory of DSP core through Avalon Bus, to update and implement DSP code parameter read acquisition data.

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EMBEDDED PROCESSOR AND OPERATING SYSTEM

The Embedded Processor as control core of the system and interacting platform between front-end and upper monitoring interface, completes updating the quench algorithm codes by visiting the shared memory of DSP core, and uploads data to the upper monitoring computer via Ethernet. Cyclone V SoC is a kind of Altera Corporation's FPGA chip, which contains two hard processors based-on ARM Cortex-A9 so that it's convenient for engineer to set up a customized embedded processor system. There is a Cyclone V SoC chip on Cyclone V SoC development board produced by Altera, so using it as a system development platform can meet the design tasks.

According to system requirement, the Embedded Hard Processor is built and configured in Qsys (Quartus II system architecting tool). Figure 3 shows the frame of the processor.

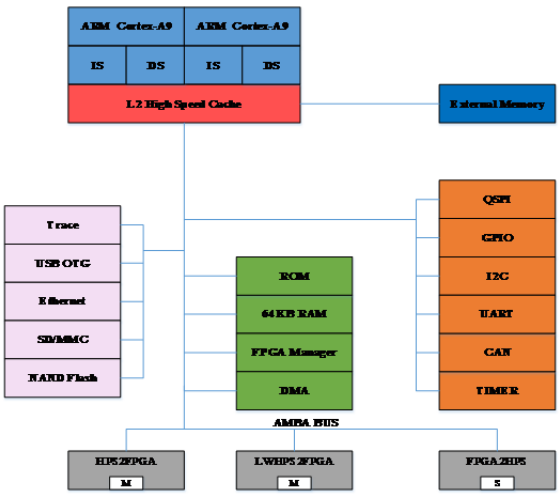

Figure 3: Frame of the processor.

Hard core processor and FPGA parts (including DSP soft core) communicates through ARM AMBA AXI bus. IP Bus Master of FPGA part can visit hard core bus slave via bridge (FPGA2HPS) which is configured 64-bit. Similarly, HPS bus master can visit bus slave of FPGA part via (HPS2FPGA) which is configured 64-bit, too. Both of the bridges support simultaneous reading/writing. Besides, processor can be used to configure FPGA frame through the specified 32-bit port (LWHPS2FPGA) under the control of procedure.

When construction of the project module is finished in the Qsys, the typical FPGA development process is launched to generate the chip configuration file. Host PC and development board communicate through a USB port to program the chip. Hardware can be detected via System Console. Figure 4 shows the test result.

After Embedded Processor is built, it's necessary to construct the underlying operating system development environment. The completed development flow is shown in Fig.5.

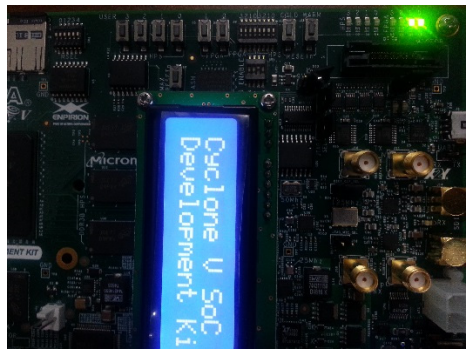

Figure 4: Hardware testing result (led blinking).

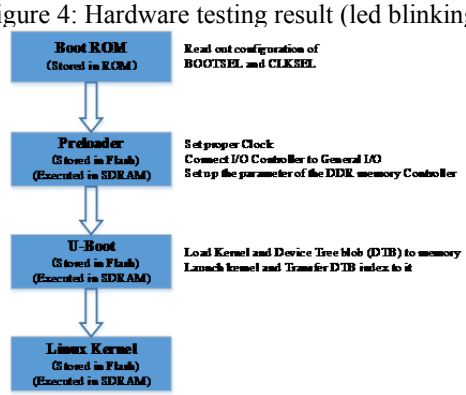

Figure 5: Processor launching flow.

A Linux system image file is installed in a SD card that can be loaded when the development board is power-on, and then the device tree blob file that contains the information about the data structure of hardware is analysed by the kernel.

FUNCTION MODULE PORTION

Multichannel digital signals collected by front-end of system need to be stored in memory medium as certain sequence and prescribed format, and then read by DSP core. At the same time, whether the whole system is working normally calls for a dedicated monitoring mechanism, therefore, it's necessary to develop some sub modules independently to achieve these functions. Figure 6 shows the frame of Function Module Portion.

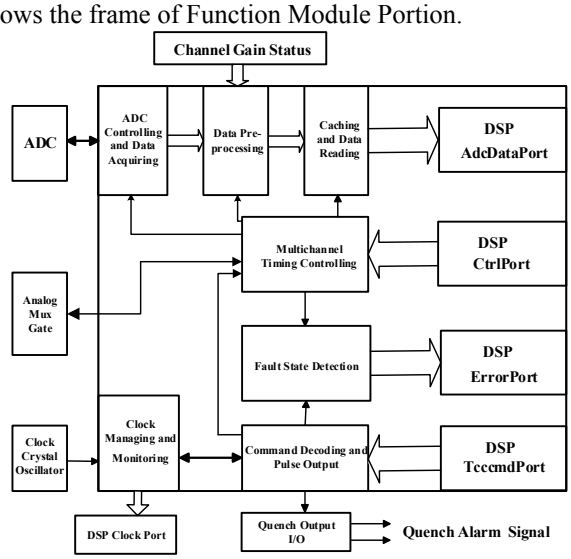

Figure 6: Frame of Function Module Portion.

Each module has its unique function as shown below:

1. ADC Controlling and Data Acquiring Module realizes the function that controls the ADC chip and reads out all the digital data.

2. Multichannel Timing Controlling Module that acts as the controlling centre mainly implements multi-channel choice of all acquisition channel, maintenance of synchronous sampling and polling sweep of data, etc.

3. Data Pre-processing Module undertakes the task that regrouping the read 16-bit digital data and state of each channel, and then making up required frame format to write it into FIFO waiting for DSP to read. The data requires regrouping includes 16-bit digital data got from ADC Controlling and Data Acquiring Module, identification numbers of data collection boards and channels, as well as the current channel code CH_SLOT from Multichannel Timing Controlling Module. The output data is 32-bit after regrouping and making up the frame as shown in Fig.7.

ADC Upper 8 bit	ADC Lower 8 bit	Channel States	CH_SLOT

Figure 7: Data format

4. Caching and Data Reading Module adopts asynchronous FIFO to store the data after regrouping and making up the frame, furthermore, to realize the function that DSP can control reading and writing with data. FIFO stores 32-bit restructured data of all channels in sequence, and the reading module generates memory read control signal to divide the 32-bit data into 4 bytes, and then output them to 8-bit port waiting for DSP to read. Figure 8 shows the frame of Caching and Data Reading Module.

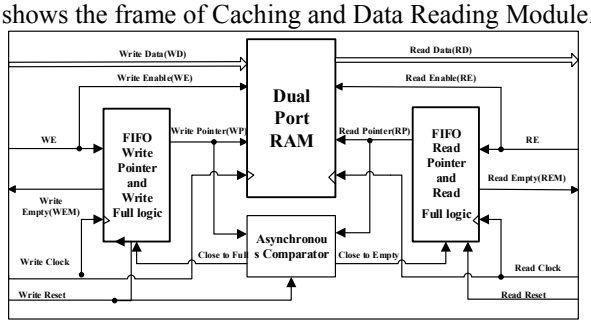

Figure 8: Frame of Caching and Data Reading Module.

5. Fault State Detection Module monitors and records key signals and flags of system real-timely such as FIFO memory unit, Heartbeat detection, 600Hz trigger pulse detection and ADC sampling conversion busy testing.

6. Clock Managing and Monitoring Module generates system sampling 600Hz clock, which is also the cycle frequency of the main program of the DSP data processing. Meanwhile, the module monitors and records the clock at any time.

KEY TECHNIQUES OF DSP

The DSP soft core which acts as main processor of digital signals, implements functions such as reading original collected data from FIFO in Function Module Portion, restoring, calibrating and digitally filtering the data, making floating point arithmetic and quench judgment according to the pre-set data processing algorithms. In addition, it realizes handshake and command response with Embedded Processor.

Equation 1 is the quench judgment formula:

$$Vq = V - L\frac{dI}{dt} - IR \quad (1)$$

The definition of each character is shown in Table 1.

Table 1: Definition of each character

Char	Definition	Remark
V	Voltage between two ends of coil	Calculated
I	Current in coil	Calculated
$\frac{dI}{dt}$	Change rate of current in coil	Calculated from current I
IR	Inherent resistance voltage drop	Eliminate effects by parameter adjustment software
L	Inductance of coil	

In this equation, Vq stands for change of voltage between both ends of the coil when quench happens, which is the basis of quench judgment and jumps out of the safe threshold range when quench occurs.

In every main cycle of quench judgment algorithms, firstly, the DSP core sends pulse command to launch next round of data collection and conversion. Secondly, it calls the data reading sub function to read in data from the last round and finish reduction, calibration and thermal drift correction of the data. Finally, the data after processing is compared with the set value of the threshold database, and then one cycle of quench judgment process is completed.

CONCLUSION

Nowadays, one development direction of integrated circuit technology is developing System-on-Chip (SoC), meanwhile, quench detection domain calls for more digital and intelligent products, thus, it's a forefront research topic to establish a quench detection system based-on SoC technology. So far, we have accomplished the task that setting up hardware framework of the embedded hard core processor and configuring the embedded operating system. On the other hand, the front-end data processing, caching, timing controlling and fault monitoring modules have been integrated, in the meantime, the implementation of DSP soft core and the development of its quench algorithm procedure is undertaken, too. Eventually, after developing the bottom drivers and control software based on EPICS framework, a set of digital quench detection system with standard performance, high integration and good portability will be implemented at the end of 2017.

REFERENCES

[1] D.F.Orris, S.Feher, M.J.Lamm, J.Nogiec, S.Sharonov, M.Tartaglia, J.Tompkins, et al.," A digital quench detection system for superconducting magnets", Proceedings of PAC'99, New York, 1999.

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