CONCEPTUAL DESIGN FOR THE HEPS POWER SUPPLY SYSTEM

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Abstract

The High Energy Photon Source (HEPS) requires more than 2000 power supplies with various kinds of power rating. The power supply system includes power supplies for the Booster, Transport, and Storage Ring. The power supply for the Booster is based on 2 Hz sinusoidal dynamic current output with 0.1% current tracking requirement. For all power supplies for the storage ring, the long-term current stability is required to be 10 part per million (ppm) which is much more rigorous than commercial products. The paper shows the conceptual design of the power supply system for the HEPS and possible solutions to critical technical challenges.

INTRODUCTION

For the HEPS planned to be built in Beijing, the storage ring consists of 48 hybrid seven-bend achromats which is proposed to reach emittance as low as 60 pm rad with a circumference of about 1296 m [1]. The stability of power supplies for the ring is required to be better than 10 ppm of the full scale of dipoles, quadruples, sextuples and normal corrector magnets. The fast orbit feedback system requires the small-signal bandwidth of fast corrector supplies up to greater than 5 kHz. For the Booster accelerating the beam energy from 300 MeV to 6 GeV, all main magnet power supplies are required to track the reference current waveform within the tolerance to promise the orbit stability.

BOOSTER POWER SUPPLIES

There are approximately 200 power supplies for the Booster with a circumference of about 432 m. The induced voltage is very high because of the 2 Hz dynamic current outputs. For example for one type dipole, totally there are 52 magnets connected in series, the output voltage is up to 12,000 V. Considering such high voltage, we separate the supply into two sets with 6000 V output each one. Figure 1 shows the waveform of calculated voltage and power based on the nominal current and parameters of each magnet. Table 1 shows the basic parameters of power supplies and magnets load [2].

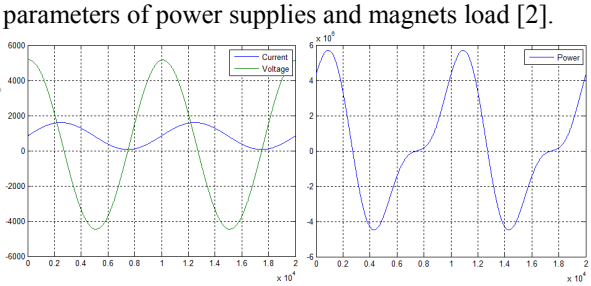

Figure 1: Calculated output of the Booster dipole PS.

Table 1: Booster Power Supplies Specifications

Type	Spec.	Nr.	Load(Ω/H)
Dipole	1600A/6000V	2	0.4/0.5
	1600A/1500V	1	0.08/0.12
Quad.	750A/4000V	1	1.2/0.5
	500A/70V	8	0.03/0.005
	500A/70V	16	0.05/0.012
Sext.	600A/2400V	1	1.5/0.16
	600A/1200V	1	1/0.13
	600A/400V	1	0.4/0.04
Corrector	±15A/±10V	168	

Modular-based switching mode power supplies will be used to achieve the high current and high voltage requirements. Figure 2 shows the block diagram of the topology. The booster circuit after the diode-rectifier is implemented to decrease the power fluctuation of the line.

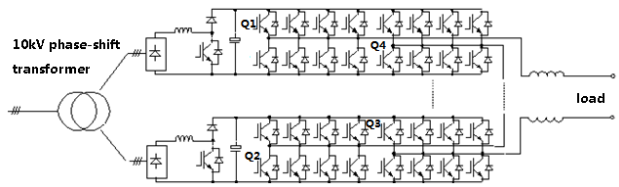

Figure 2: Block diagram of the Booster PS.

For Booster power supplies, it is important to promise the current tracking error within 0.1%. Figure 3 shows the block diagram of the tracking error control for each power supply based on the Digital Power Supply Control Module (DPSCM).

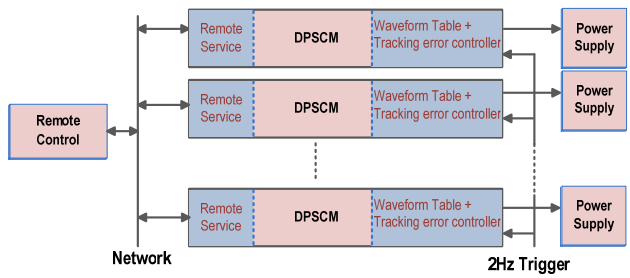

Figure 3: Block diagram of the tracking error control.

A 30 A/150 V fully digital controlled switching mode prototype has been designed and proved to be better than 0.1% tracking error with the digital "repetitive controller" embedded in the close-loop regulator.

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STORAGE RING POWER SUPPLIES

There are totally about 1900 power supplies for the storage ring. The following table shows the specifications, the quadrupoles and correctors are supplied separately. Except fast correctors, the others are required to be very high current stability of 10 ppm (vs. Imax)/12 h.

Table 2: Storage Ring Power Supplies Specifications

Name	Spec.	Nr.
Longitudinal Gradient Dipole	150A/800V	4
Dipole/Quadrupole Combined	200A/600V	6
Quadrupole	120A/25V	768
Sextupole	100A/600V	4
	80A/500V	1
Octupole	30A/250V	1
Normal Corrector	±15A/±10V	720
Fast Corrector	±15A/±50V	384

In order to make the design more flexible and self-customized, we prefer to purchase commercial voltage-source, not current source. Figure 4 shows the conceptual design of the power supply system. With the high precision current transducer DCCT and the self-designed digital power supply control module DPSCM, the voltage source can be easily transferred to a current-stable source, and the performance will be mostly determined by the DPSCM and DCCT. There is an additional option if the power part can interface with the pulse width modulation (PWM) signals directly. Here the PWM should be with high resolution up to a few tens picosecond.

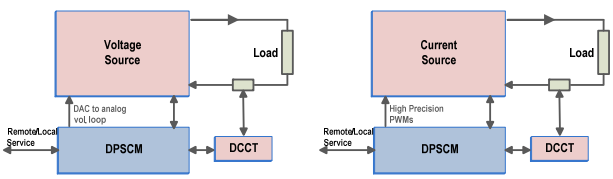

Figure 4: Conceptual design of the high precision PS.

We have designed a 300 A power module with relatively low voltage output. The current deviation is about 7 ppm peak-to-peak in 12 hours. The result is not good enough. There are two aspects to be improved, one is the temperature-stable control of the DPSCM analog part, and the other is the power part which should be designed to lower voltage ripple to promise short-term stability. Now the improvements of DPSCM and manufacture of prototypes for quadrupole power supplies based on the Fig. 4 block diagram are undergoing.

Considering the low power requirement of correctors and cost-effective design, the chopper-based design of corrector power supplies will be implemented. A few sets correctors will use a common DC-source and digital signal processing part, but the high frequency inverter and analog part of the digital control are independent for each power supply.

For the fast orbit feedback system, fast correctors with small-signal bandwidth greater than 5 kHz will be required. Now the magnets parameters are not determined yet, there is no accurate value of the calculated voltage output. Anyway the switching-mode topology will be given priority to be designed. With the preliminary magnet design parameter of Lm/Rm = 50 μH/190 mΩ, the power supply with 50 kHz switching frequency and with PWM multi-phase-shift up to 200 kHz, it is achievable to meet the requirement based on the simulation result.

POWER SUPPLY CONTROL MODULE

The digital power supply control module DPSCM is a very important part of the power supply system. The first generation DPSCM has been used for the power supply system of Chinese Spallation Neutron Source (CSNS). We are planning to produce the second generation DPSCM, named DPSCM-II to upgrade the hardware to meet the requirements for high precision power supplies for HEPS. Figure 5 shows the conceptual structure of the DPSCM-II.

The Altera Cyclone V FPGA will be chosen as the signal processing part. Not only protection logics, but also close-loop regulators such PID controller and repetitive controller will be implemented in the FPGA. With the method of System-on-a-Programmable-Chip (SOPC), a NiosII CPU with the real-time operation system uCOS-II will be embedded in the FPGA. All logics control and regulators are fulfilled by the hardware with the hardware description language.

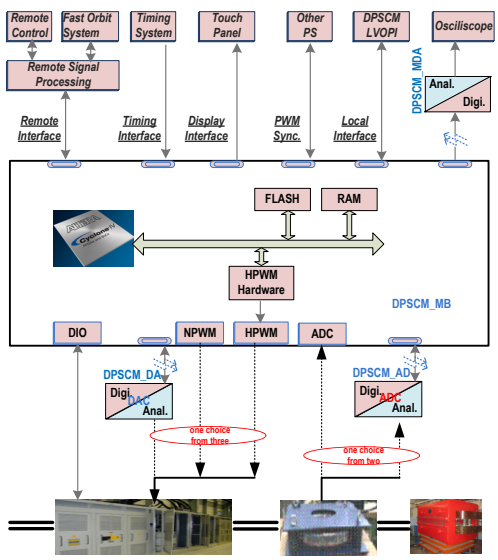

Figure 5: Conceptual design of the DPSCM-II.

The hardware of DPSCM-II composes of four parts, which are the main board DPSCM-MB, the high precision ADC board DPSCM-AD, the voltage source interfacing board DPSC-DA and the diagnostic board DPSCM_MDA.

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For different interfacing to the power part, there are three options. One is the normal PWM (PWM + PFM) which the precision of the PWM is processed by the digital algorithm. The second one is the high precision PWM which the PWM resolution is promised by a precision programmable delay circuit. And the other one is an isolated-controlled DAC that interfaces with the analog voltage loop of the commercial voltage-source.

There are 16-bit ADCs on the DPSCM_MB, for the feedback sampling of power supplies with the current-stability requirement lower than 50 ppm, such as supplies for the Booster and High/Low Energy Transport. The DPSCM-AD is a high precision, temperature-controlled board which takes an important part to assure the current stability of 10 ppm for the storage ring power supplies. Figure 6 shows the block diagram of the circuit [3].

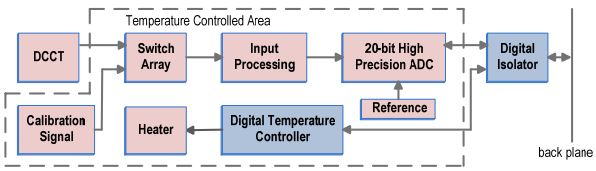

Figure 6: Block diagram of the DPSCM-AD circuit.

The remote control interface is now a part of the digital controller. There are two options, one is via Ethernet for supplies besides fast correctors, and the other one is Fiber-link based with 100 Mb/s communication speeds which can meet the requirement of 100 kHz reference refreshing ratio for fast correctors.

The interfaces between the DPSCM and the timing system is designed to trigger and recall the PS faults information reserved in the memory of the DPSCM-MB, and to synchronize the 2 Hz waveform of Booster PS.

Test points inside the digital controller can be monitored by the circuit DPSCM_MDA. It is very convenient to choose different digital sources and get a visual analysis on the oscilloscope via digital to analog converter on this board.

Because the algorithm implemented in the FPGA is based on hardware design, the final output of the digital controller is much higher than software-based processing. Table 3 shows the performance of the DPSCM-II.

Table 3: DPSCM-II Performance

Processing Delay	Calculating Cycle	PWM Freq.	Bandwidth
<= 7us	1us	0.02Hz~ 1MHz	10kHz

MEASUREMENT AND CALIBRATION

For the long-term current stability test, the measurement is based on the traditional way with the high resolution multi-meter such as Fluke 8508A. The test of current ripple is based on the dynamic signal analyser, which can show the result of spectrum analysis directly [4].

A platform of DCCT calibration system is now on the way of design. Figure 7 shows the block diagram, it is based on the commercial DCC and range extender to calibrate the analog output of the DCCT I/V conversion.

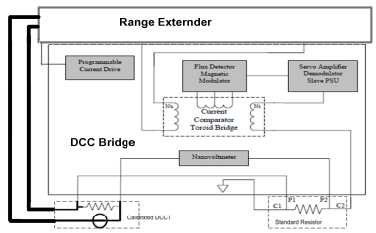

Figure 7: Block diagram of DCCT calibrating platform.

CONCLLUSION

The HEPS requires a large number of different specifications power supplies. For the storage ring power supplies are required to be 10 ppm long-term current stability. For the Booster dynamic current output with DC plus 2 Hz sinusoid current output is required with 0.1% tracking error to promise the orbit stability. And for fast orbit feedback, fast correctors should be designed as 5 kHz small-signal bandwidth. Now some power supply prototypes and improvements of the DPSCM are undergoing, and the specific test results will be shown in the near future.

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