DESIGN OF A HIGH-SPEED PULSED 324 MHz SOLID-STATE AMPLIFIER FOR USE IN A BEAM CHOPPER

Shane Dillon, Chris Schach, Brad Nobel, Tomco Technologies, SA 5069, Australia

Abstract

A 324MHz 30kW high-speed pulsed solid-state amplifier has been designed for use in a beam chopper at the Japan Proton Accelerator Complex (J-PARC). This paper discusses the various design challenges and presents the initial performance test results. In particular, the amplifier achieves pulse rise and fall times of less than 15 nanoseconds, is easily upgradeable in power, and withstands 100% power reflection without damage.

INTRODUCTION

An amplifier has been designed for use in a beam chopper at the Japan Proton Accelerator Complex (J-PARC). In general, beam chopping applications place some extreme technical demands on the performance of the RF amplifiers that drive them [1], [2]. In particular, such amplifiers must exhibit extremely fast pulse rise and fall times, very tight pulse-to-pulse repeatability and excellent ruggedness.

This paper will discuss the most challenging specifications of the amplifier, and the design solutions that were developed to meet them.

MAJOR SPECIFICATIONS

The J-PARC beam chopper is intended to decimate the beam into segments (called "micro-pulses") 278 nanoseconds in length, with 222 nanoseconds off-time between each segment. These micro-pulses occur in bursts of 1200, giving a total of 600 microseconds per burst. The burst repetition rate is 50pps (3% duty cycle).

The key specifications arising from these operational requirements are as follows:

- Pulse rise and fall times (10-90% voltage), less than 15 nanoseconds.
- Phase change during 600 microsecond pulse burst, less than 1.5 degrees p-p.
- Amplitude change during 600 microsecond pulse burst, less than 1.5% p-p.
- Phase and amplitude repeatability from micro-pulse to micro-pulse, less than 1.5 degrees and 1.5% p-p respectively.
- Output power of at least 30kW, easily upgradeable in the future.
- Must withstand 100% power reflection without shutdown or damage.

The amplifier uses the latest generation of high-voltage push-pull LDMOS transistors. It is based on a modular construction and is designed to be readily expandable to higher power levels. It uses standard 19" rack-mount dimensions, and is air cooled. See Figures 1 and 2.

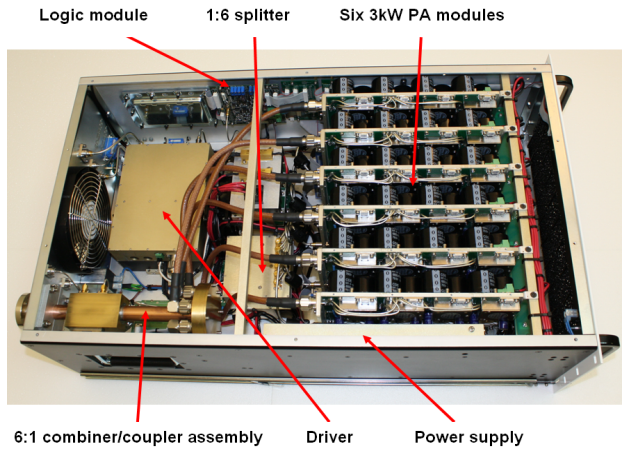

Figure 1: Internal layout of the power amplifier chassis (15kW, 324MHz). The amplifier output stage operates at approximately 68% efficiency, and is fan cooled.

MAJOR DESIGN CONSIDERATIONS

General

In order to achieve the required stability, linearity and ruggedness, it is necessary to ensure that the amplifier output transistors operate comfortably below their maximum power capability. The basic building block for the system is a 15kW amplifier chassis, consisting of six 3kW PA modules, each containing four 1kW transistors.

Minimisation of pulse rise and fall times requires several key design features:

The DC power circuit must be capable of extremely rapid rise and fall without producing AM artefacts.

The amplifier must have sufficient RF bandwidth to reproduce the fast edges. Within that bandwidth the amplifier must have a flat amplitude response and a constant group delay. Outside that bandwidth the amplifier must be well behaved and free of spurious responses and resonances.

DC Energy Delivery

Each PA module contains four 1kW LDMOS transistors. To allow for circulator and combiner losses, each module is designed to operate at approximately 3kW, or 750W per transistor. Therefore, with a 50V DC supply voltage and assuming a worst-case efficiency of 50%, each transistor draws a current of I = 750x2/50 = 30 amps during the pulse. In order to achieve the specified rise time, this means the current into each transistor must rise from zero to 30 amps in less than 15 nanoseconds. This current is delivered to the transistor through an inductance, L, which decouples the RF path from the DC

ISBN 978-3-95450-115-1

supply. Thus, the value of L is critical – it must be large enough to properly decouple the RF output from the DC supply, but small enough to permit the transistor current to reach 30 amps and the transistor drain DC voltage to stabilise within the required rise time. The optimum value of L was determined and implemented as a printed track on the PCB to ensure perfect symmetry and repeatability in manufacture. In addition, very careful selection and placement of bypass and storage capacitors was required to produce the minimum possible supply impedance from DC to larger than 100MHz. This wide-band supply bypass avoids any AM ringing or overshoot on the supply and hence on the RF pulse. A large bank of very low impedance electrolytic capacitors was fitted on a separate PCB mounted on the rear of the PA module, arranged so as to minimise the inductance between the energy storage and the transistors.

Printed "Marchand" baluns were used on the input and output of each amplifier channel to ensure tight coupling and repeatable manufacture.

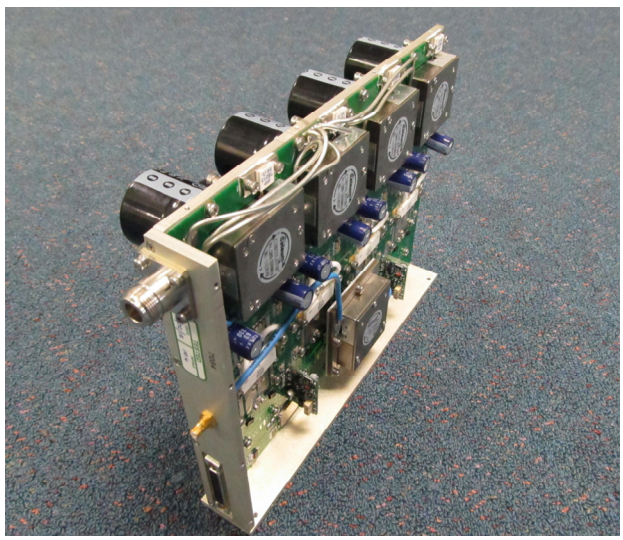

Figure 2: Internal layout of the 3kW power amplifier module, showing input and output circulators and quadrature hybrids.

After-pulse Ringing

The main type of problem encountered was low-level "ringing" and other artefacts that appear after the fast rising and falling edges. These artefacts were found to arise from various sources:

- Energy storage in inductances and capacitances throughout the amplification chain
- Unintentional RF feedback paths and earth loops
- Multiple reflections of the RF signal due to bandwidth limitations or imperfect matching between amplifier stages.
- Resonances anywhere within the bandwidth of the pulse.

The first two causes were minimised by extremely careful PCB layout, careful selection and placement of storage and decoupling components, and very careful shielding and separation of RF gain stages. Most of the power gain of the amplifier occurs inside the driver module, so this is built into a precision-machined multi-compartment screened enclosure.

The third cause was minimised by adding wideband ferrite isolators at critical points throughout the amplification chain, especially where multiple reflections could occur within coaxial cables. An isolator was placed at the output of the driver, and at the input of each PA module.

In addition to this, the power splitting at the input of each PA module uses wideband quadrature hybrids, which ensure a very high input return loss.

Bandwidth

The design of the 6:1 15kW radial combiner presented a challenge because a standard quarter-wave combiner would not fit within the depth constraints of the chassis, and would not provide adequate bandwidth.

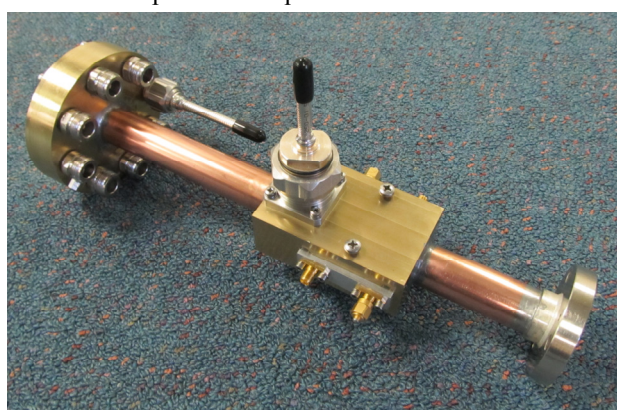

Figure 3: The 15kW 6:1 radial combiner / dual directional coupler assembly.

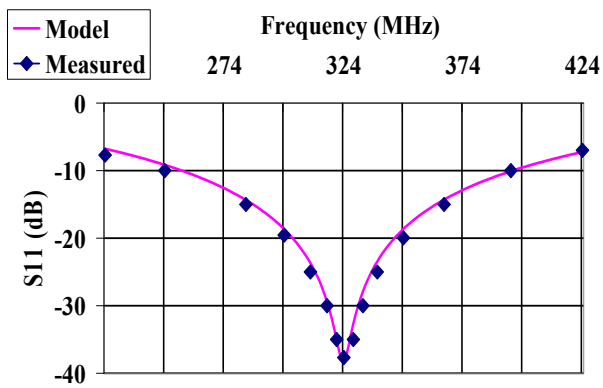

Figure 4: Modelled and measured return loss of the 6:1 combiner / dual directional coupler assembly.

The design objectives were achieved using a rigid-line transformer section only 60° long. To set the required centre frequency and bandwidth, three coaxial stubs were added, one part-way along the transformer section and two at the input end of the assembly. The dual directional coupler is located immediately after the transition to 50 ohms (see the photo in Figure 3).

ISBN 978-3-95450-115-1

The combiner behaved almost exactly as modelled. The return loss is shown in Figure 4, and shows better than 20dB over a bandwidth of 50MHz. The mid-band insertion loss was too small to measure.

PERFORMANCE

Figures 5 and 6 below show the fast rise/fall performance of the 30kW amplifier.

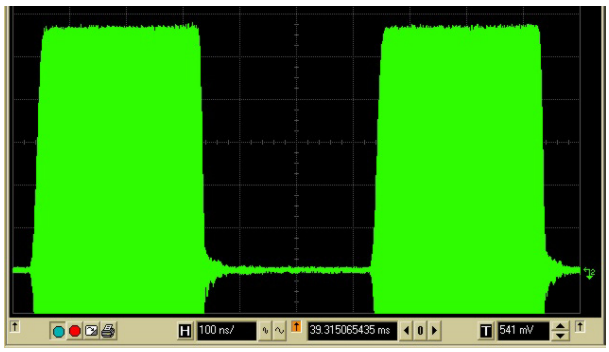

Figure 5: 30kW "micro-pulses", 100nS/div.

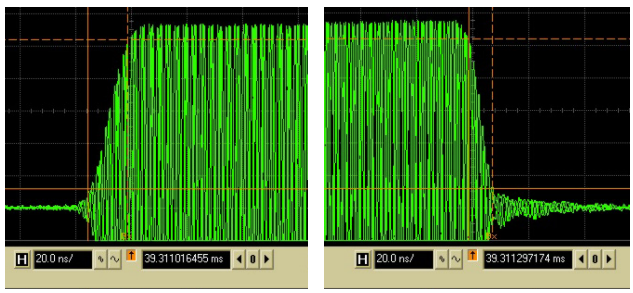

Figure 6: Detail of rising and falling edges, 20nS/div. 10-90% risetime = 14.3nS, falltime = 8.3nS.

Figures 7 and 8 below show the phase and amplitude stability of the 30kW RF output measured over a CW 600uS pulse. The waveforms were overlaid over 1000 pulses, to show the stability both within the pulse and from pulse to pulse. Most of the pulse-to-pulse variation is actually due to thermal stabilisation effects, which reduce rapidly with time.

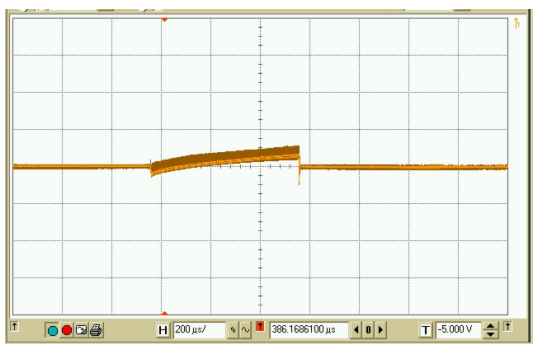

Figure 7: Phase stability. Vertical scale 1.5°/div. Phase change through pulse = 0.75°, phase spread over 1000 pulses = 0.5°p-p.

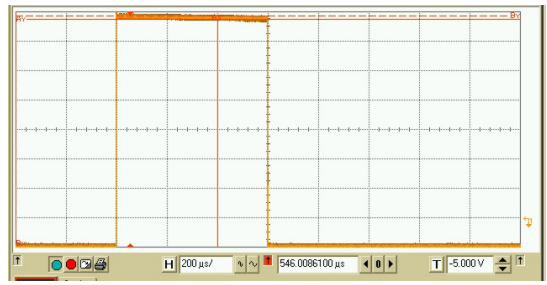

Figure 8: Amplitude stability. Amplitude droop through pulse = 1.3%. Spread over 1000 pulses = 0.85%

SUMMARY

A 30kW UHF solid-state pulsed power amplifier has been developed for use in a high-speed beam chopper, and was delivered to J-PARC in the 2011 fiscal year.

Figure 9: Front and rear views of the amplifier rack. The empty space at the bottom of the rack allows for additional amplifier units for a power upgrade.

ACKNOWLEDGMENTS

Yuichi Kanno, Yasushi Yamazaki, Masanori Nagaoka and Ryota Sato, of General Bussan Company, Tokyo, Japan.

REFERENCES

[1] F. Caspers, "Review of Fast Beam Chopping", Proceedings of LINAC 2004, Lubeck, Germany 2004.

[2] A. Aleksandrov, "Overview and Future Demands of Fast Choppers", LINAC10, Tsukuba, Japan, 2010.