DEVELOPMENT AND MANAGEMENT OF THE MODULATOR SYSTEM FOR PLS-II 3.0 GEV ELECTRON LINAC *

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Abstract

The Pohang Accelerator Laboratory (PAL) had started the upgrade project (called PLS-II) of the Pohang Light Source (PLS) from 2009 for increasing its energy from 2.5 GeV to 3 GeV and changing the operation mode from fill-up to top-up mode. Top-up mode operation requires high energy stability from the linac beam energy and machine reliability of the linac modulator systems. For providing an additional 0.5 GeV energy to the 2.5 GeV PLS linac, we added four units of the modulator system. We have two different types of the pulse modulator system in the upgrade project (PLS-II). They are thyristor control type and inverter power type. In the thyristor control type, PAL employs a de-Qing system to regulate the PFN charge voltage and controls the modulator pulse forming network (PFN) charging voltage stability. In the inverter power supply type, Capacitor Charging Power Supply (CCPS) provides highly stable charging voltage to the modulator. We will present development and management of the pulse modulator system for obtaining machine reliability and stability from 3.0 GeV linac.

INTRODUCTION

We performed the design of the additional modulator system in order to achieve the energy of 3.0 GeV for PLS-II. To achieve this energy, sixteen high power klystron and modulator units which are labelled as M01~M08 (Line Type Modulator) and M09~M16 (Inverter Type Modulator) as well as fifteen energy doubler (SLED) cavities are necessary with somewhat modest energy margin. There are two kinds of concepts in these modulator systems.

One is the existing type called a "Line Type Modulator" [1] that is a traditional resonant charging scheme, and they are installed from M01 to M08 in PAL linac. The PFN capacitors are charged to twice the DC power supply voltage due to the DC resonant charging characteristics. To achieve better regulation on PFN charging voltage, a deQing system was employed in the modulator systems. The target stability with the systems is less than 0.015% rms or 0.035% pk-pk.

The other type is an "Inverter Type Modulator" that was installed from M09~M16 in PAL linac to charge the pulse-forming network (PFN) for the pulsed power source of the RF amplifier. The energy will be charged to a load capacitor by CCPS. The voltage ramp-up on the capacitor will be linear due to the constant current output of the power supply. The target stability in the system is less than 0.1% pk-pk. The stability is exactly depending on the CCPS used as dc source power in the modulator system.

Sixteen klystron-modulator systems are finally installed in Linac Gallery to achieve the energy of 3.0 GeV for PLS-II. The peak powers of the modulator and the klystron are 200 MW and 80 MW, respectively. The klystron output frequency is 2856 MHz. Each klystron output power is compressed by a SLED. The RF output power from M02 to M16 is delivered to respective SLEDs in order to obtain the energy of 3.0 GeV. We need one module as a spare one and allow the stored beam in the SR to be stable for the period of top-up mode.

PULSE MODULATOR FOR PLS-II

Inverter Type Modulator

The PLS-II modulator is physically composed of three parts: a main cabinet, control racks, and a pulse tank. Figure 1 is the configurations for the PLS-II modulator. The main cabinet includes a pulse forming network (PFN), a thyratron switch, protection circuits, and an EM (electromagnetic) noise-filtering box. The control rack consists of an inverter power supply, an interlock & control unit, and other equipments. The klystron is mounted on the top of the pulse tank.

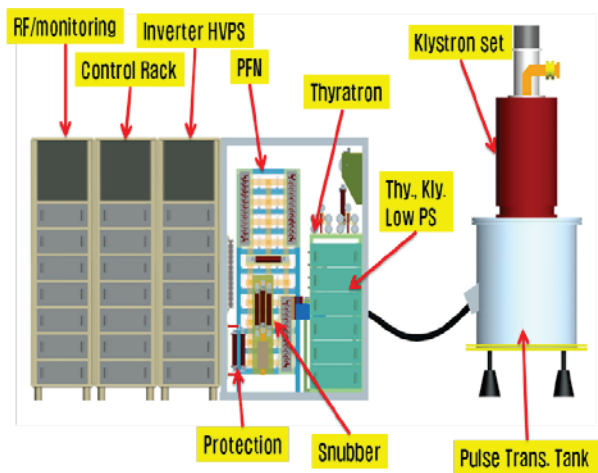

Figure 1: Configurations of the PLS-II modulator system.

Figure 2 is a simplified schematic diagram of the PLS-II modulator. The HV inverter power supply regulates the PFN voltage within 0.1% pk-pk. The inverter charging power supply acts as a constant current source. Charging voltage of the inverter power supply should be same as the PFN charging voltage. Therefore, we need twice higher voltage power supply than the resonant charging

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modulator. The charging voltage increases linearly as the PFN charges up to the desired level. Then, the charging voltage is regulated by the inverter power supply until the discharge. Therefore, this circuit does not require external voltage regulation circuit, such as de-Q'ing. After discharge, the power supply stops charging for a moment so that the thyratron can recover. This hold-time will help to reduce any possible pre-fire due to voltage appear across the thyratron during recovery.

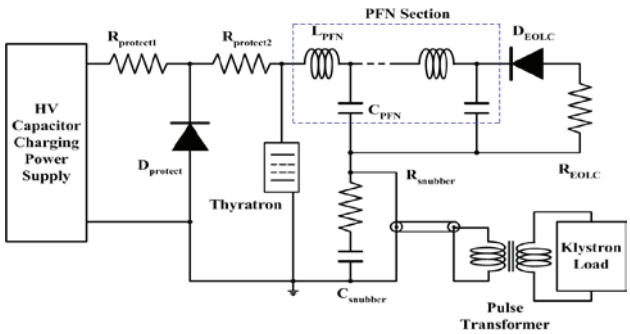

Figure 2: The schematic diagram of the PLS-II modulator.

HV Inverter Power Supply

A CCPS using high frequency inverter technology can be adopted for the PLS-II modulator system. Top-up operation is going to begin for the PLS-II. Since the operation needs to have more stable beam from the Linac and low electron beam energy fluctuation, the beam voltage regulation is required to be less than 0.1 % pk-pk. Figure 3 shows the results of the peak to peak stability that is mean:5.88mV / value:7.65V*100= 0.077% pk-pk.

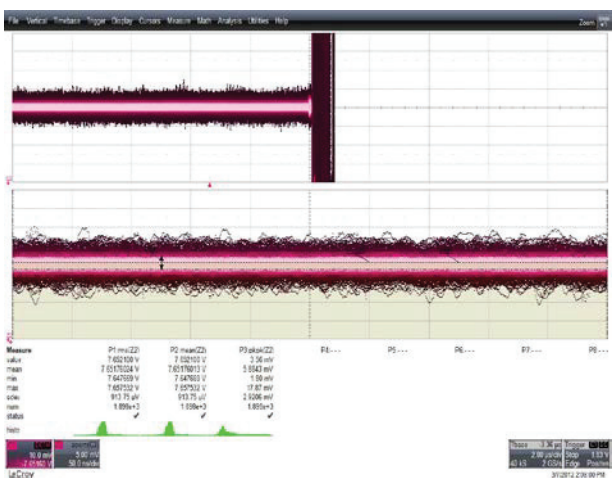

Figure 3: PFN voltage stability.

Table 1 shows specifications of the PLS-II modulator. The load capacitor of 1.4μF is normally charged to 42kV using three units of a 50kV, 10 kJ/sec rated CCPS at 10 Hz. The CCPS adopted in the modulator system are made by General Atomics.

Line Type Modulator

Figure 4 shows a simplified modulator circuit. The modulator can be divided into four major sections: a charging section, a discharging section, a pulse transformer tank, and a klystron load. Two parallel, fourteen sections, type-E Guillemin networks [2] are used for the PFN. The PFN impedance is about 2.8 Ω. Each PFN capacitor has a fixed capacitance of 50 nF, and each PFN inductor can be varied manually up to 4.5 μH. By adjusting inductance of each PFN section, we can precisely tune the flattop of the modulator output voltage pulse.

Table 1: Specifications of the PLS-II Modulator

Description	Unit	Value
Peak Power	MW max	200
Inverter CC HVPS Average Power	kW	20
Repetition Rate	Hz normal	10
Pulse Peak Output Voltage	kV	400
Pulse Peak Output Current	A	500
ESW	μs	7.5
PFN Impedance	Ω	2.7
PFN Section		
Total Capacitance	μF	1.4
Each Capacitance	nF	50
Total Inductance	uH	10.5
Each Inductance	uH	1.5
PFN Stage		14 Parallel
Pulse Transformer Turn Ratio		17
Thyratron		Litton L4888
Flat-top Width	μs	4.4
Charging Time	ms	80

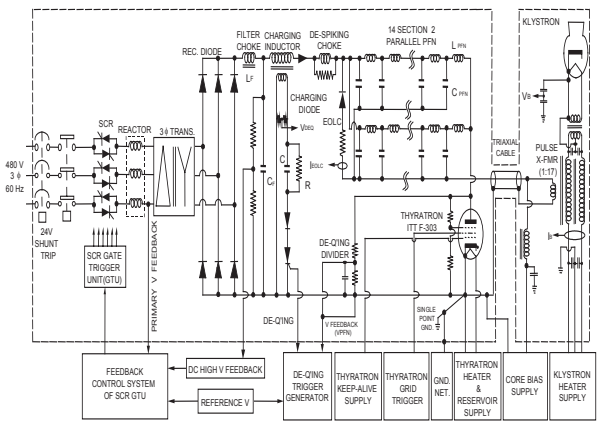

Figure 4: Schematic circuit diagram of the modulator.

The line type modulator uses a traditional resonant charging scheme. The dc power supply of the modulator is a conventional, three-phase full-wave bridge dc supply with choke input filter. Instead of using an induction voltage regulator (IVR), a phase-control system with six SCRs is used because the phase controller is more effective than IVR in terms of cost, space, and controllability. A SCR AC-AC voltage regulator controls primary 3-phase 480V AC power. The voltage regulator

receives feedback signals from the primary AC voltage and the high voltage DC (HVDC) detector. The closed loop control of the AC-AC voltage regulator ensures stable HVDC output. Therefore, the phase control charging scheme has been used for control of full three phase primary power. The charging voltage regulation of the linac modulator is done by a deQing circuit.

DeQing System

As shown in Figure 5, the circuit function of differentiating PFN charging voltage is that it detects PFN charging voltage electrically from a difference buffer in the deQing controller. The sample and hold circuit picks up the peak value of the slope voltage coming from the differentiated charging waveform. The voltage selected from the sample and hold circuit and a dc reference voltage are compared with a difference amplifier. The difference amplifier outputs an error signal voltage compared with the reference which is coming from the deQing reference voltage calculated from the deQing controller. The role of the voltage control delay is that the error signal level obtained from the comparator is adjusted by the following amplifier and converted into a digital signal used for a deQing trigger delay. Its value makes the adjustment of the timing of a deQing trigger by the digital-delay circuit. The role of CPU is that it displays a reference voltage and current high voltage, and condition of deQing on or off.

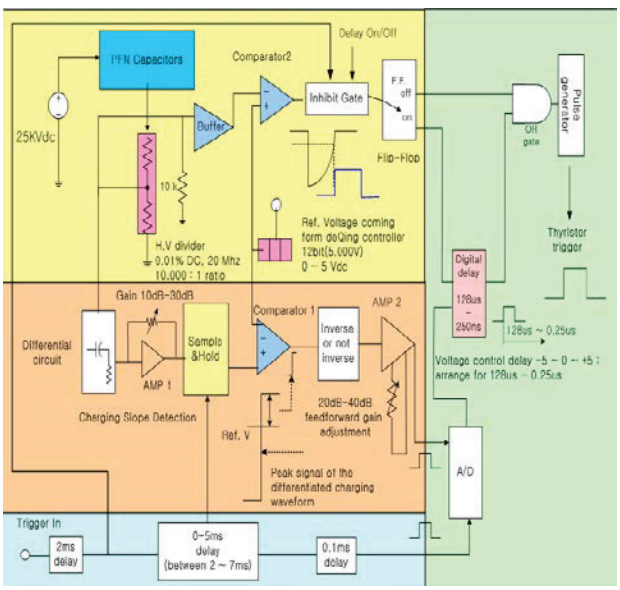

Figure 5: De-Qing block diagram.

The de-Qing circuit is normally adjusted to dissipate a few percent of the charge in each cycle. At the measurement of a grade of deQing by using the deQing controller, the grade of 4.3% deQing is the best working. At the test of the grade below 3% deQing and over 4.5%, the stability of PFN charging voltage is more deteriorating. Thus, the best deQing grade is about 4.3% at the full PFN charging voltage.

PFN voltage waveforms measured by a 5,000:1 divider (or 10,000:1 ratio) are shown in Figure 6. LeCroy HRO 64Zi Scope with 12-bit ADC function was adopted to measure the modulator stability precisely. The result of the peak to peak stability for 10 minutes is 0.03% pk-pk. Value of charging voltage in Figure 6 is 8.23(V) and the mean value is 2.6(mV).

Figure 6: Waveforms of a PFN charging voltage.

SUMMARY

With the aid of deQing, the variation, as shown in Figure 6, measured from PFN position is 0.03% pk-pk (value of mean: 8.23(V) and value of mean value: 2.6(mV)) which is a reduction of more than 2 times below that of the stability by CCPS type. However, both of the modulator types satisfy our requirement, which is less than 0.1% pk-pk. Reliability in the linac modulator systems is also very important on top-up mode operation and therefore, we are going to make daily and monthly procedures to check out their condition.

REFERENCES

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[2] G. N. Glasoe and J. V. Lebacqz, "Pulse Generators," McGraw-Hill, Chapter 6 (1948).

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