DIGITAL LOW LEVEL RF DEVELOPMENT AT DARESBURY LABORATORY

P. Corlett, L. Ma, A. Moss, STFC Daresbury Laboratory, UK.

Abstract

Digital LLRF development using Field Programmable Gate Arrays (FPGAs) is a new activity at Daresbury Laboratory. Using the LLRF4 development board, designed by Larry Doolittle of Lawrence Berkeley National Laboratory, a full featured control system incorporating fast feedback loops and a feed forward system has been developed for use on the ALICE (Accelerators and Lasers in Combined Experiments) energy recovery linac. Technical details of the system are presented, along with experimental measurements.

INTRODUCTION

The ALICE ERL accelerator uses an analogue LLRF control system to stabilise the RF fields within its superconducting cavities.

This system has performed well, giving very low RMS noise in phase and amplitude, however since ALICE was constructed, advances in digital technology have made using a digital system much more attractive.

Digital systems offer immense flexibility to the operator, in terms of being able to remotely modify control loop parameters, in addition to providing much complex integrated diagnostics.

One of the most attractive features offered by modern digital systems is adaptive feed-forward control to overcome beam loading. This has the potential to allow ALICE to operate at much higher beam current, which is presently limited by the analogue LLRF system.

Engineers at Daresbury Laboratory have been developing a digital LLRF system to replace the existing analogue system on the ALICE accelerator.

SYSTEM DESCRIPTION

Hardware

The system is based around the LLRF4 development board, designed by Larry Doolittle at LBNL [1]. This board has many of the features necessary to perform fundamental LLRF control tasks. These features include:

- 4 x 14 Bit ADCs running at up to 125MHz
- 2 x 14 Bit DACs running at up to 250MHz
- Xilinx Spartan 3 FPGA
- Programmable clocking resources

In order to allow the LLRF4 board to be used on the ALICE machine, a number of hardware additions / modifications have been made which include the addition of a Lantronix Xport RS232 to Ethernet converter which has been integrated into the system via a daughter card connected directly to the LLRF4 board. This modification allows communication between the FPGA and a host computer.

Figure 1: The LLRF4 Development Board

The RF frequency of the ALICE machine is 1300MHz. This is too high to be directly sampled at 125MHz, therefore the input signal is down-converted to a more manageable frequency prior to sampling. 50 MHz was chosen as an appropriate IF frequency. The down-conversion to 50MHz is performed externally to the LLRF4 board in a separate enclosure. This enclosure is temperature stabilised to +/- 0.1 degree C, reducing long term phase drifts to less than 0.1 degree.

Control Algorithms

The complete digital signal processing flow is shown in Figure 2. An adaptive Kalman filter [2] is placed after the Non-IQ demodulator [3] to suppress noise of the cavity probe signal. Digital Down Conversion (DDC) is used for reference signal (from master oscillator) processing. The FPGA clock is synchronized with the master oscillator signal through a phase locked loop [4].

In order to overcome beam loading effects, a simple adaptive feed forward scheme has been designed and implemented on the FPGA. Two memory blocks within the FPGA are used: - one for recording the control error signals for each RF pulse, the second for recording the error integration over the RF pulse. This integrated error signal is summed with the controller output during each beam pulse. Figure 3 shows the Feed forward processing scheme utilised.

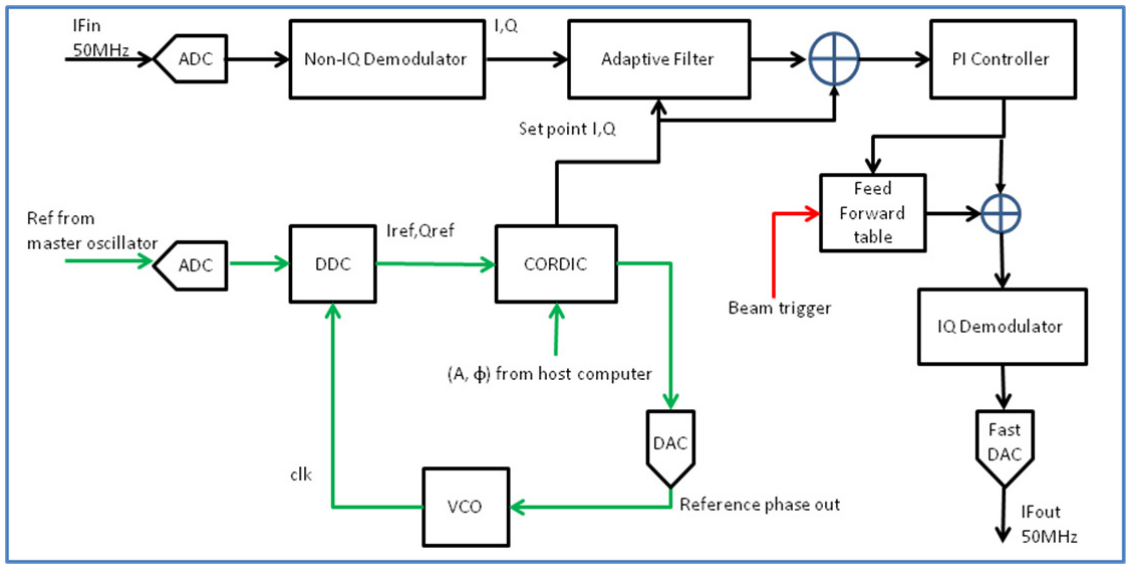

Figure 2: LLRF 4 DSP Flow

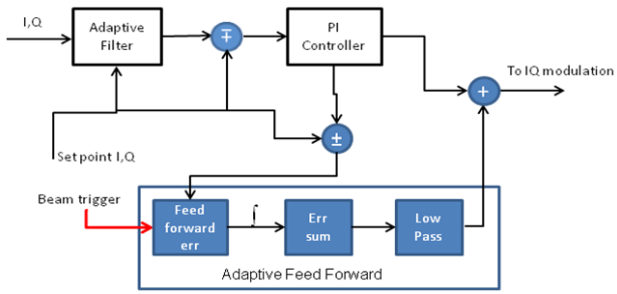

Figure 3: Adaptive Feed Forward Scheme

High Level Controls Interfacing

An intermediate layer of interfacing is implemented in Labview. This layer is the "expert" user panel, and allows members of the RF team to modify control loop parameters.

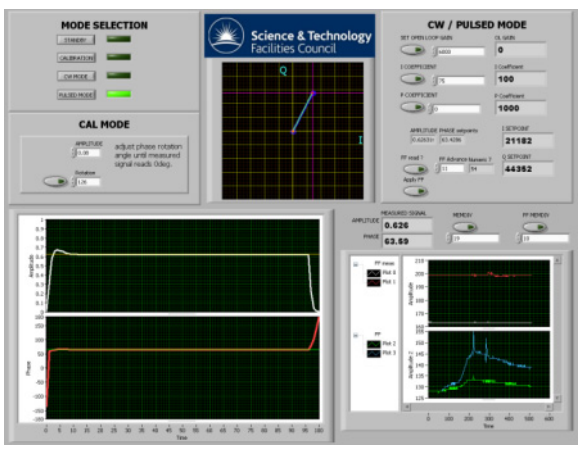

Figure 4: Labview "expert" panel

This layer communicates via the X-port device, receiving diagnostics data from the FPGA, and sending setpoints / loop parameters to the FPGA.

The ALICE machine uses EPICS for its highest level controls interface. Therefore in order to completely integrate the DLLRF system into ALICE, an EPICS control panel was necessary. The Daresbury controls group has produced a simple "operator" panel. This lacks all but the most essential control parameters such as Amplitude, Phase, and a control to activate Feed-forward.

TEST RESULTS

Bench Test / Buncher Cavity

The Digital LLRF control system was first tested on ALICE buncher cavity (a normal conducting cavity with Q ~ 20,000). A Hittite digital phase frequency detector, which is capable of measuring RMS phase noise as low as 0.008˚ was used to compare the cavity probe phase to the Master Oscillator phase.

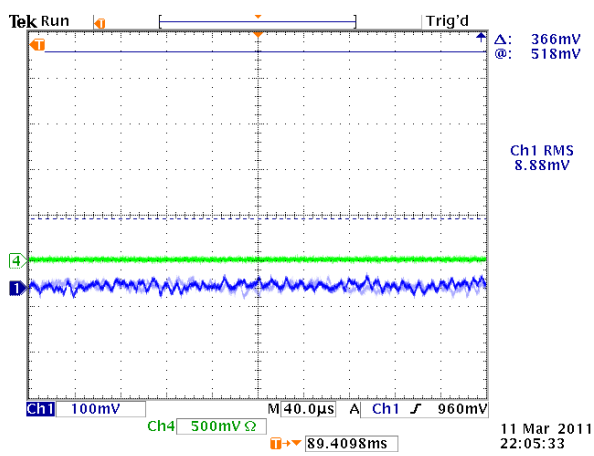

Figure 5: Phase rms error measurement of the DLLRF system applied to the buncher cavity (1°= 380mV)

The rms voltage error seen by the Hittite detector during the cavity flat–top was measured to be 8.88mV (shown in blue on Figure 5), which corresponds to rms phase error of 0.024˚.

This is consistent with the expected phase noise from the LLRF4 board.

Superconducting Cavity Tests

The digital LLRF system was recently tested on an ALICE super-conducting Linac cavity. The amplitude and phase errors were measured at a cavity gradient of 12MV/m.

A Boonton pulse power meter was used for amplitude error measurement, and a Hittite digital phase frequency detector was used to measure phase error.

Without beam, the measured amplitude error over the cavity flat-top was 0.6%. The Hittite phase detector measured the phase error to be 0.1˚.

A 100us beam pulse was steered through the cavity, and measurements of amplitude and phase were taken with high beam loading. Phase error (pk-pk) was 1 degree, and amplitude error 1.8%. Figures 6 and 7 show these measurements. Beam loading can be observed during the final ¼ of the RF pulse.

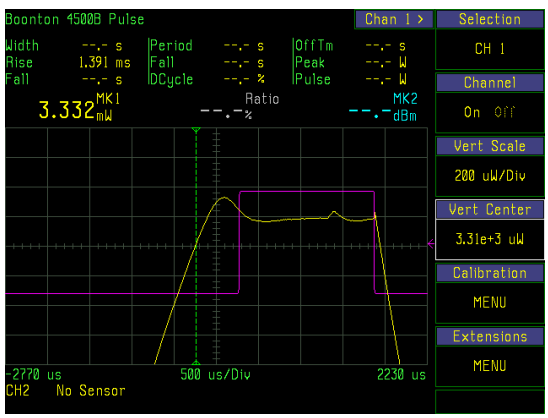

Figure 6: Amplitude error on ALICE superconducting Linac Caviy (yellow trace shows measured cavity probe power 1 division = 200uW (cables not calibrated))

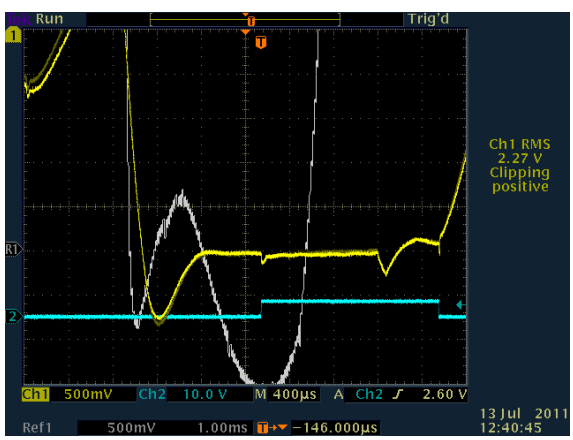

Figure 7: Phase Error during the RF pulse (Yellow trace shows phase, 1 division = 1.35 degrees)

The machine was then set up for energy recovery. In this mode, very little beam loading is observed. Therefore the feedback system can be qualified without the need to use feed-forward. The machine operators observed no additional beam jitter (as compared with operations using the standard ALICE analogue system).

For this test, only feedback control was used. A feedback plus feed forward control will be tested later this year.

The errors observed during the flat top were significantly higher than for the normal conducting tests. This is due to the higher microphonic noise level, which is about 5 times larger than for the normal conducting cavity, and the Lorentz force detuning inherent in the superconducting RF cavity. The Linac cavity presently does not have any Piezo electric tuners. Potential reasons for the much higher noise level for the superconducting test are to be investigated further.

FUTURE PLANS

Installation on ALICE

The next stage for the Daresbury Digital LLRF project is a long term test of the system using the Buncher cavity. This will demonstrate the operational reliability of the system over several weeks. In the mean time, 5 additional systems will be built up for installation on the superconducting RF ALICE cavities (plus 1 spare)

Improved SCRF Cryomodule

A major upgrade programme to install a newly designed Superconducting module in place of the ALICE LINAC cavity is due to take place in November 2011 [5]. This module has integrated Piezoelectric tuners. It is planned to use digital LLRF methods to overcome the Lorenz force detuning effect which seriously limits the operational performance of ALICE.

REFERENCES

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