A NEW REAL-TIME PROCESSING PLATFORM FOR ELETTRA 2.0 STORAGE RING

TUMBCMO24

Elettra Sincrotrone Trieste

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Processing synchronous data is essential to implement efficient control schemes. A new framework based on Linux and **DPDK** will be used to acquire and process sensors and control actuators at very high repetition rate for **Elettra 2.0**. As part of the ongoing project, the actual fast orbit feedback subsystem is going to be re-implemented with this new technology. Moreover the communication performance with the new power converters for the new storage ring is presented.

DPDK DATA PLANE DEVELOPMENT KIT

Gold Members: arm, AT&T, Ericsson, F5, Intel, Marvell, Mellanox, NXP, Red Hat, ZTE

1 - DPDK

DPDK, initially developed by **Intel** in 2010, supported directly by the Linux Foundation and sponsored by market leaders as **ARM**, **Red Hat**, **AT&T, NVIDIA (Mellanox)** and **Ericsson.**

•**DPDK is more then a Linux network stack bypass technique**. In junction with Linux kernel advanced features (cpu isolation, SMP affinity, NUMA support…) it is possible to **reach microsecond jitter performance** in normal user space program.

•**User code spins (PMD) on a dedicated core waiting for incoming packets.** Once the packets are available, data processing and retransmission can be managed by the same core or executed on other reserved cores.

2 - Elettra 2.0

•The Elettra 2.0 project, the upgrade of the old Elettra storage ring, was approved by the Italian Government in 2017 and definitely confirmed in 2019. According to the current schedule the new machine will start serving the users in **January of 2027**.

•The total number of magnets is 552 with 192 corrector coils and 171 BPMs. For the fast correction (fast orbit feedback) 72 additional coils (6 per achromat) will be used. **The total number of power converters will be 1344**.

• **Three types of correctors**: correctors embedded in sextupoles, "pure" correctors at the entrance/exit of straight sections, air core coils before each bending magnet

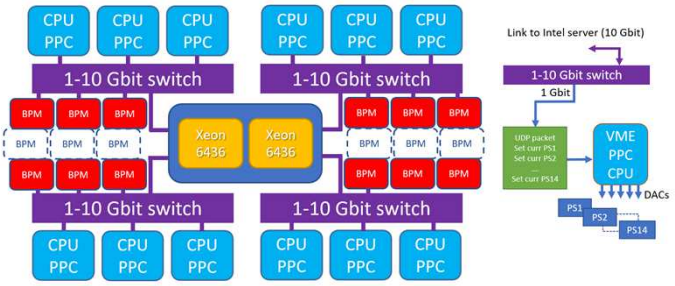
•All power supplies will be connected to a centralized server by means of dedicated fiber links **exchanging data at the fast orbit feedback rate**.

•All the beam position monitors will be acquired at least at the **fast orbit feedback rate**. Four to six beam position monitors will be acquired at turn by turn data rate. (1.15MHz)

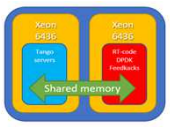
Elettra 2.0 Fast Orbit Feedback rate 40-100 kHz

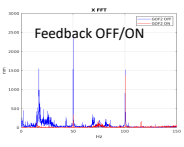
3 - Fast Orbit Feedback upgrade

Starting from the beginning of the upcoming year, **the fast orbit feedback upgrade (running in the old Elettra storage ring), will become fully operational, facilitating the assessment of components for Elettra 2.0**.
Currently, the Elettra storage ring hosts 96 BPM detectors (Libera-Electron) that transmit data via Ethernet at **10 kHz** to twelve **Motorola MVME6100 CPUs**, with each receiving data from eight BPMs by means of four 48-port Extreme X440-G2 switches. Each CPU, equipped with digital to analog cards (DAC), can superimpose a maximum current equal to one-fortieth of the total strength onto the corresponding seven horizontal/vertical correctors.



A dual-socket DELL PowerEdge R750 rack-mounted server equipped with Xeon 6436 Gold processors, 384 GB of memory and eight 10Gbit ports (two Intel X710-DA4 cards) is connected to the same switches. **These switches can be reconfigured to redirect BPM traffic from the MVME6100 boards to the first four network ports of the DELL server.**
Furthermore, the legacy fast orbit feedback running on the VME PPC CPU boards can be programmed to halt feedback calculation and process only a UDP packet, containing the DAC settings, that is transmitted by the DELL server at the **feedback repetition frequency (20 kHz)**.
The fast orbit feedback application will **run on top of DPDK Hardware Abstraction Layer** (HAL). **Eight CPU cores** are dedicated to exchange data with BPMs and power converters, **one CPU core** is dedicated to feedback calculations. A shared memory across the two sockets implements communication between Tango servers running on socket 1 and feedback code running on socket 2.

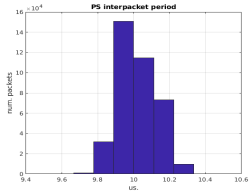




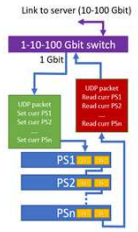
4 - Elettra 2.0 Power Converters

In-house, we have developed two prototypes of power converters, capable of handling currents of 20 A and 100 A, respectively. These converters will be employed to regulate the current for multipole magnets and the three types of correctors. The models come equipped with a controller **developed by CaenELS**, offering interfaces such as an Ethernet port connected to the ARM microprocessor and a dual gigabit SFP port directly connected to the FPGA for fast feedback point to point or daisy chained setting.

100 kHz setting rate



Elettra 2.0 power converter fast connection



To evaluate the maximum set/read speed of future power converters for Elettra 2.0, a DELL PowerEdge 750R server configured in a manner similar to the one used for the fast orbit feedback upgrade **transmits a UDP packet containing the current setpoint at a rate of 100 kHz** to the power supply's SFP interface. This frequency aligns with the speed of the internal regulation loop within the FPGA. A network analyzer, the Anritsu MT1000 in a pass-through configuration, analyzes the return packet from the power supply to the server, containing the current readout.
Based on the data recorded by the analyzer, **the time between the passage of one packet and the next amounts to 10 μs, with an rms well below the micro-second**, confirming the system's jitter very good performance in terms of packet processing.

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19th Biennial International Conference on Accelerator and Large Experimental Physics Control Systems
Cape Town, 9-13 October 2023

ICALEPCS CAPE TOWN SOUTH AFRICA 2023