CONSOLIDATION OF THE POWER TRIGGER CONTROLLERS OF THE LHC BEAM DUMPING SYSTEM

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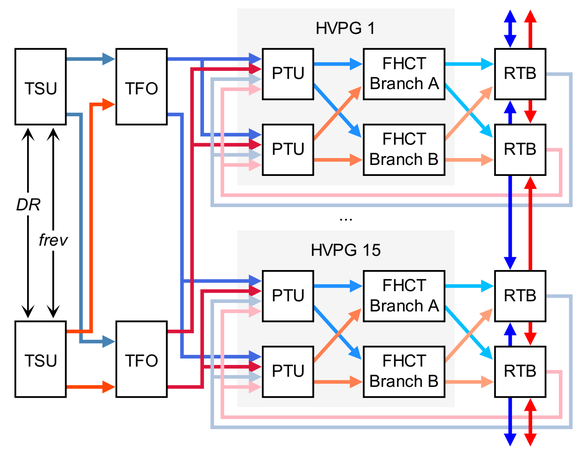
Abstract

The Power Trigger Controller (PTC) of the LHC Beam Dumping System (LBDS) is in charge of the control and supervision of the Power Trigger Units (PTU), which are used to trigger the conduction of the 50 High-Voltage Pulsed Generators (HVPG) of the LBDS kicker magnets. This card is integrated in an Industrial Control System (ICS) and has the double role of controlling the PTU operating mode and monitoring its status, and of supervising the LBDS triggering and re-triggering systems.
As part of the LBDS consolidation during the LHC Long Shutdown 2 (LS2), a new PTC card was designed, based on a System-on-Chip (SoC) implemented in an FPGA. The FPGA contains an ARM Cortex-M3 softcore processor and all the required peripherals to communicate with onboard ADCs and DACs (3rd-party IPs or custom-made ones) as well as with an interchangeable fieldbus communication module, allowing the board to be integrated in various types of industrial control networks in view of future evolution.

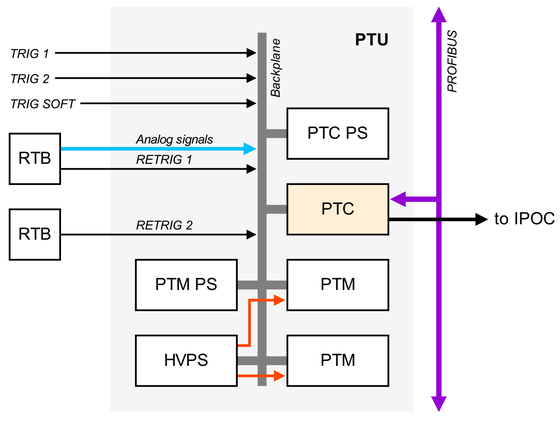
LHC Beam Dumping System (LBDS)

Two Trigger Synchronization Units (TSU) synchronize the Dump Requests (DR) with a particle-free beam abort gap, then two Trigger Fan-Out units (TFO) distribute the triggers to redundant PTUs, which start the conduction of two switches composed of Fast High Current Thyristors (FHCT) that discharge capacitors into the magnet. In addition, a redundant fault-tolerant Re-Triggering System (RTS) allows the asynchronous fast retrigger of all HVPGs if one HVPG self-triggers. Each HVPG is equipped with two Re-Trigger Boxes (RTB), that couple internal pickup signals to the redundant Re-Trigger Lines (RTL) to generate a pulse when the HVPG is triggered, and also capture the pulses on the RTLs and send them to their PTUs.



Power Trigger Units (PTU)

A PTU is composed of several internal low and high-voltage power supplies, two PTMs operated in parallel, and one PTC. Each PTU has 5 trigger inputs: two for synchronous triggers from two redundant TFOs, two for asynchronous triggers coming from the RTLs through redundant RTBs, and one software trigger input, used for test purposes, e.g. to trigger a single HVPG individually. For added redundancy, each PTM is connected to a different FHCT, in parallel with a second PTM from the other PTU (branches A and B).

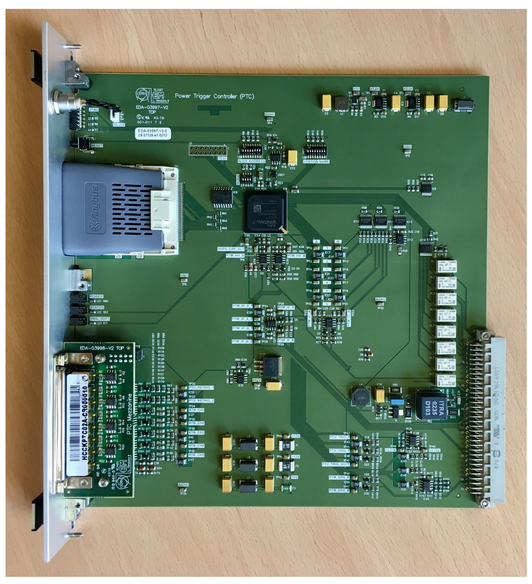


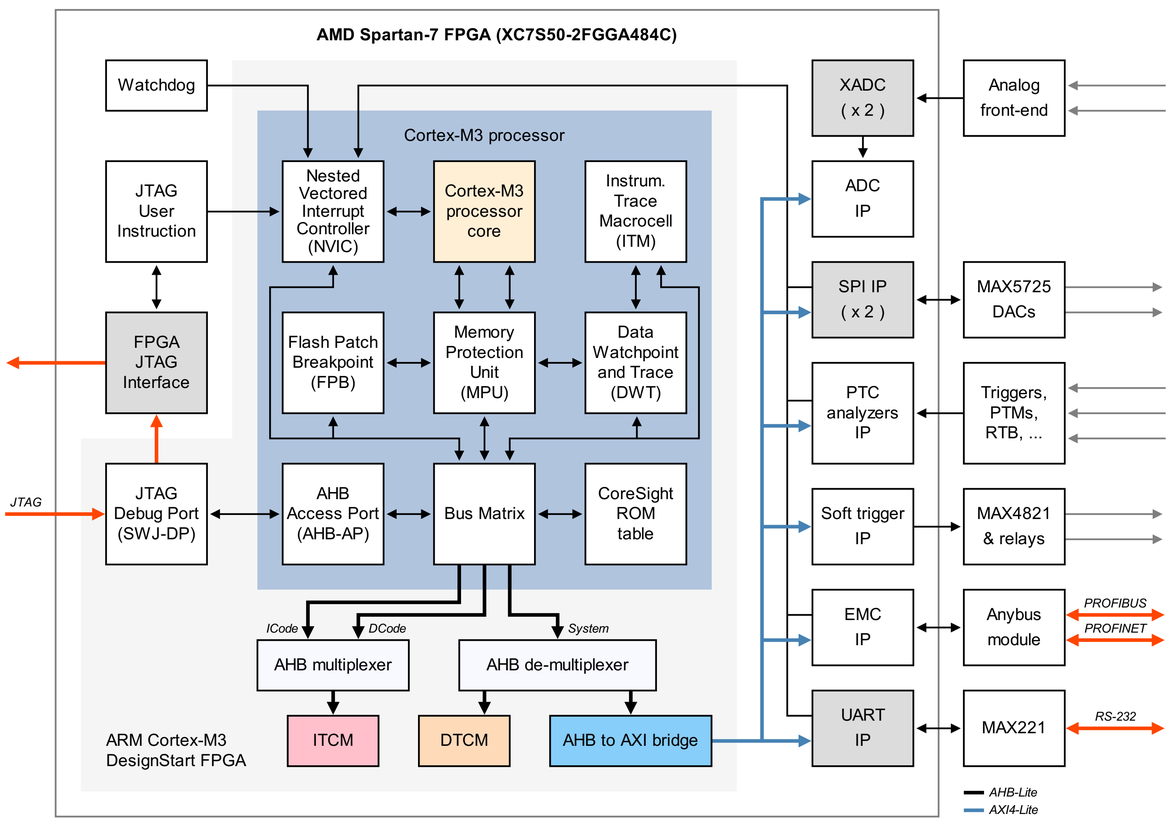
Power Trigger Controller (PTC)

The PTC controls the high-voltage power supply of the PTMs and monitors it continuously. It also supervises the rest of the PTMs power supplies with window comparators. When the PTC detects one of the 5 triggers on the backplane, it perform a post-mortem analysis of the PTU and the RTB. It checks that the two synchronous triggers were received first and, as a consequence of the HVPG pulsing, that the two asynchronous triggers were received afterwards, within a given time window. It then checks that the PTMs principal and compensation currents were nominal, and that the PTMs gate driver circuits stayed active for the expected duration. Finally, it makes sure that the 5 pickup signals at the input of the RTB were received. The results of the analyses are sent to the industrial control system of the LBDS, namely the State Control and Surveillance System (SCSS), through a fieldbus. A faulty status either makes the SCSS issue a dump request to the TSUs or prevents rearming the LBDS.

New PTC design

The new PTC has been designed as a System-on-Chip (SoC). This consists in a softcore processor, integrated with all the required peripherals, and implemented in an AMD Spartan-7 FPGA.
The ARM Cortex-M3 32-bit processor, targeted at highly deterministic control applications, was selected for its very short interrupt latency and exceptional code density. It is packaged with an Instruction Tightly Coupled Memory (ITCM), containing the embedded software developed in C, and a Data Tightly Coupled Memory (DTCM), used as RAM. The software is executed directly from the ITCM, as this is much faster than executing from the flash memory, and is thus available right after the FPGA configuration, without requiring any bootloader. A combined bitstream, including both the gateware and the software parts, is stored in the PTC flash memory.
The processor and its internal components are shown in the central blue box; their integration in the FPGA environment is comprised in the light gray box.
Connected to the AXI bus are several peripherals, either hard IPs (available in the FPGA) or provided by AMD (gray boxes), or custom-made ones written in VHDL (white boxes).





Fieldbus module

The Anybus CompactCom M40 fieldbus module from HMS Networks was selected for its extensive flexibility. These modules are fitted from the front panel of the cards via a CompactFlash type connector, and can easily be replaced to convert the board to a different fieldbus, saving the costs of a new hardware design.
The PTC is currently integrated in the LBDS SCSS using a PROFIBUS fieldbus, however an upgrade to a PROFINET network is foreseen in the near future. Both networks are already included in the embedded software and were tested in the lab.