FRIB BEAM RAMP PROCESS CHECKER AT CHOPPER MONITOR

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ICALEPCS 2023 THMBCMO26

Introduction

Chopper in the low energy beam line is a key element to control beam power in FRIB. As appropriate functioning of chopper is critical for machine protection for FRIB, an FPGA-based chopper monitoring system was developed to monitor the beam gated pulse at logic level, deflection high voltage level, and induced charge/discharge current levels, and shut off beam promptly at detection of a deviation outside tolerance. Once FRIB beam power reaches a certain level, a cold start beam ramp mode in which the pulse repetition frequency and pulse width are linearly ramped up becomes required to mitigate heat shock to the target at beam restart. Chopper also needs to generate a notch in every machine cycle of 10 ms that is used for beam diagnotics. To overcome the challenges of monitoring such a ramping process and meeting the response time requirement of shutting off beam, two types of process checkers, namely, monitoring at the pulse level and monitoring at the machine cycle level, have been implemented. A pulse look ahead algorithm to calculate the expected range of frequency dips and rises was developed, and a simplified mathematical model suitable for multiple ramp stages was built to calculate expected time parameters of accumulated pulse on time within a given machine cycle.

Design

Displayed in Fig. 1, the beam ramp process checker consists of pulse counter, micro checker, macro checker, control, Double Data Rate memory (DDR3), microBlaze and physical interface of User Datagram Protocol (UDP) and universal asynchronous receiver / transmitter (UART). The pulse counter block takes inputs from GTS event receiver, HV switch and chopper plate and counts the pulse width (PW), cycle time and total beam on time of machine cycle (MC) using an 80.5 MHz clock and generates the count done signals of each. These counts and done signals are distributed to the micro and macro checkers, where they calculate the range of expected values ahead of time and check if the presented counts fall out of range. Thereafter Fault signals can be triggered. The control block has a timer to assert valid signals of ramp steps which enable the micro and macro checker to move to the corresponding ramp stage of initialization and calculation. It packs the data of calculated range, counts and checking results of PW, cycle and beam on time of MC and loads to two DDR3 where each has 256MB memory. It also communicates with the microBlaze for user configuration and display purpose. The microBlaze system handles the UDP and UART communication protocol. The UDP provides the channel of EPICS communication. UART is to readout the DDR3 content for debug purposes

Micro Checker

Micro checker consists of a micro Digital Signal Processing (DSP) and a look ahead logic block. The micro DSP calculates the max and min target value of next pulse cycle time and width. The calculation is completed with a pipelined structure of floating point number operators of one multiplier, one divider, one adder and one floating to fixed point number converter. The final value of tolerance is derived by adjusting the calculated value from DSP with the pulse cycle ramp step size, the expected max and min value of transition period and the full power pulse. The look ahead logic block calculate the 2nd pulse cycle and width, will decide to maintain, extend or shrink the derived 1st cycle time by comparing 2nd pulse cycle time with the time left in the MC.

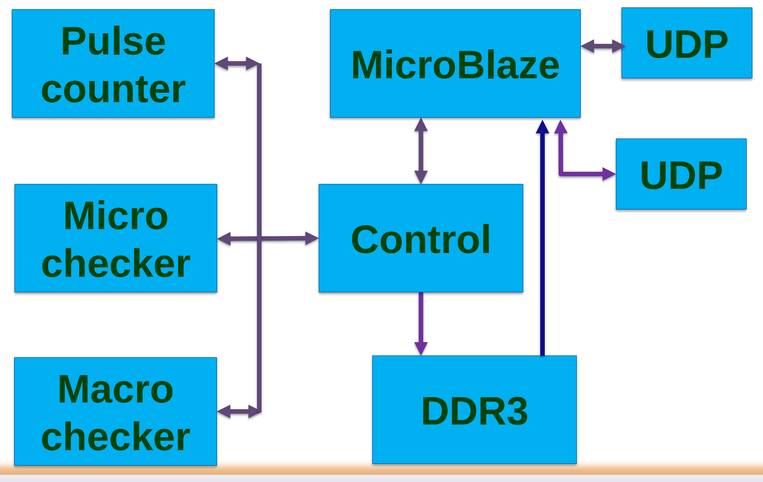

Figure 1: Figure 1: Process checker system block diagram

Macro Checker

The macro checker calculates the tolerance range for the Beam on Time (BT) of MC and checks if measured BT is within the tolerance range. The macro checker DSP is built on one of each floating point number operator of adder, subtractor, multiplier, divider and floating to fixed point number converter, and two of fixed to floating point number converters. The algorithm displayed in Figure 2 is followed to pipeline these operators and achieve the best balance of FPGA resource utilization and calculation speed. Details can be found in the paper.

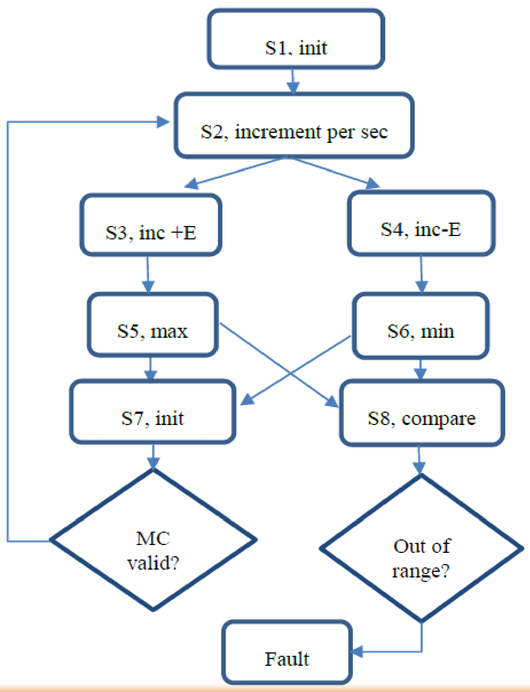

Figure 2: : macro checker DSP flow chart of data processing

Test and Results

The DSPs of micro and macro checker were tested in functional and post route simulations. The timing is checked in the post route simulation. The calculation accuracy is checked in the function simulation of the whole ramp process by comparing the calculation results of DSP with the math result from the test bench. A lab test was conducted to test the entire FPGA design. The pulse source is the GTS pulse generator. The FPGA platform is the FRIB General Purpose Digital Board. The software is the EPICS IOC and OPI of the chopper monitor. Both the micro and macro checkers are required to be configured through the EPICS before the GTS pulse starts. The results are checked with chipscope and by plotting the measured data stored in DDR3. All test results meet the design expectations.

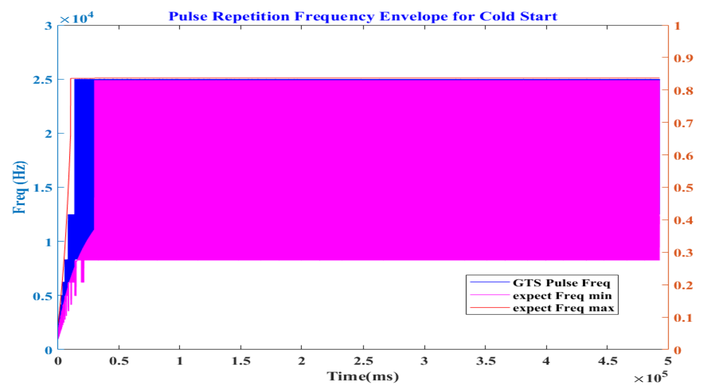

Figure 3: Micro checker calculated range and GTS PRF signal. The blue is GTS PRF, the red is the max value of PRF, the magenta is the min value of PRF.

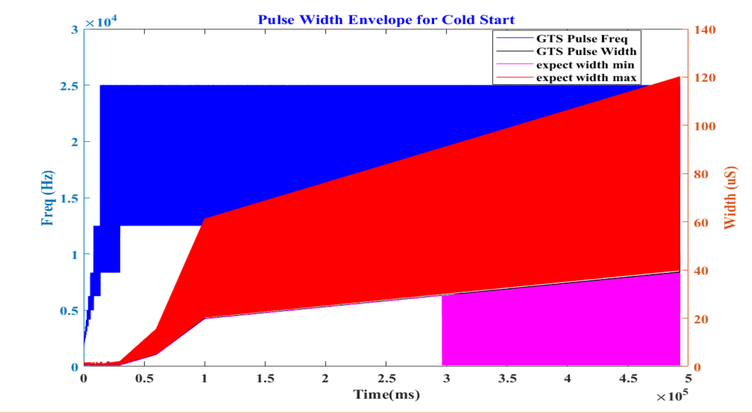

Figure 4: Micro checker calculated range and GTS PM signal. The blue is GTS PRF, black is GTS PM, red is the max value of PM, magenta is the min of PM.

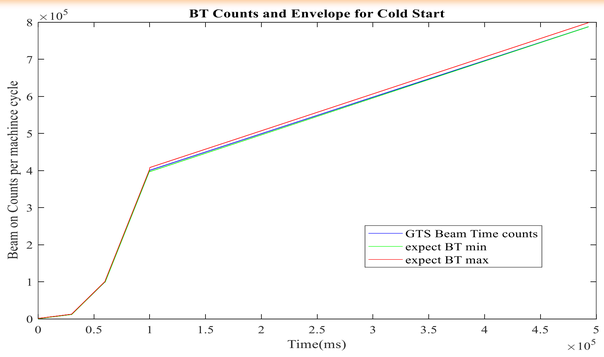

Figure 5: Macro checker calculated range and GTS beam on time counts per MC. The blue color curve is the BT time counts of MC, red color curve is the expected maxi-mum value of BT time, green color curve is the minimum value of BT timer.

Conclusion

A beam pulse ramp up process checker system was successfully developed at FRIB. The future plan is to integrate with other beam mode logics at chopper monitor and the new IOC to be able to read out the process data from DDR3 through UDP interface upon user request and display the process status and root cause data if a fault is triggered.

FRIB Facility for Rare Isotope Beams
U.S. Department of Energy Office of Science
Michigan State University

Work supported by Work supported by the U.S. Department of Energy Office of Science under Cooperative Agreement DE-SC0023633