Status of Fast Obit Feedback System of HEPS

(Cooperation work among all related systems)

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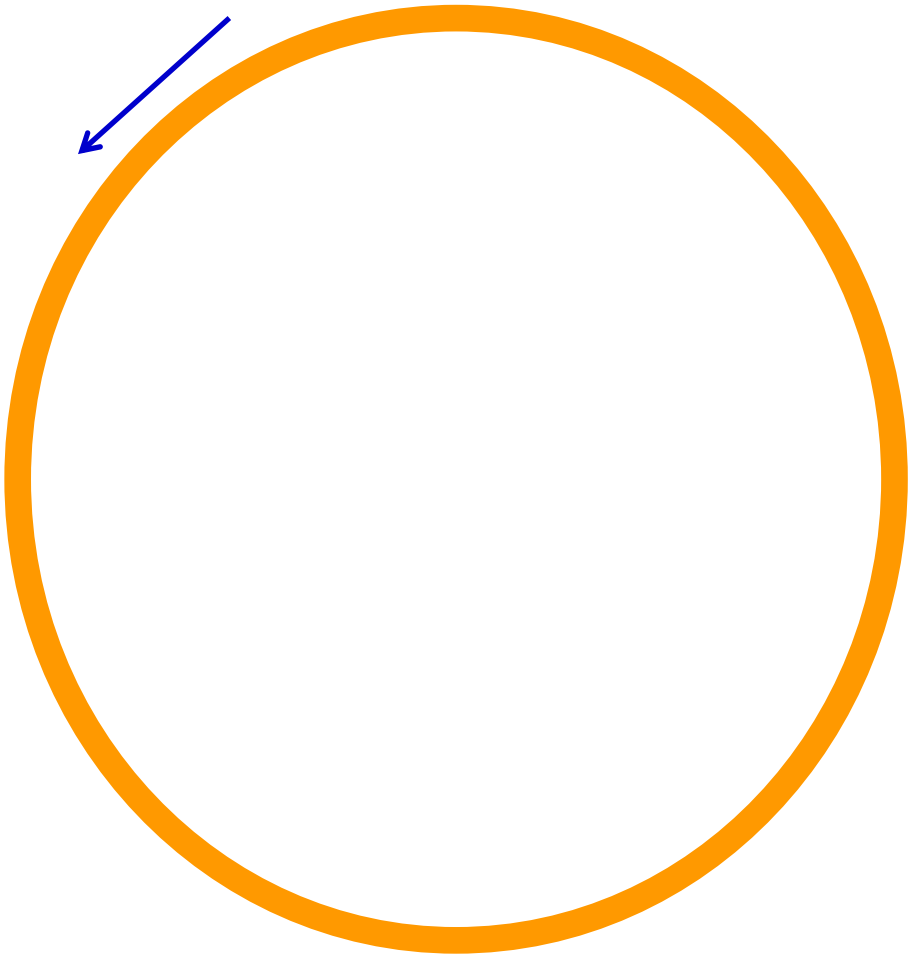
Outline

- Introduction
- Requirement
- Architecture
- Hardware and Logic Design
- Schedule
- Summary

Introduction of the FOFB



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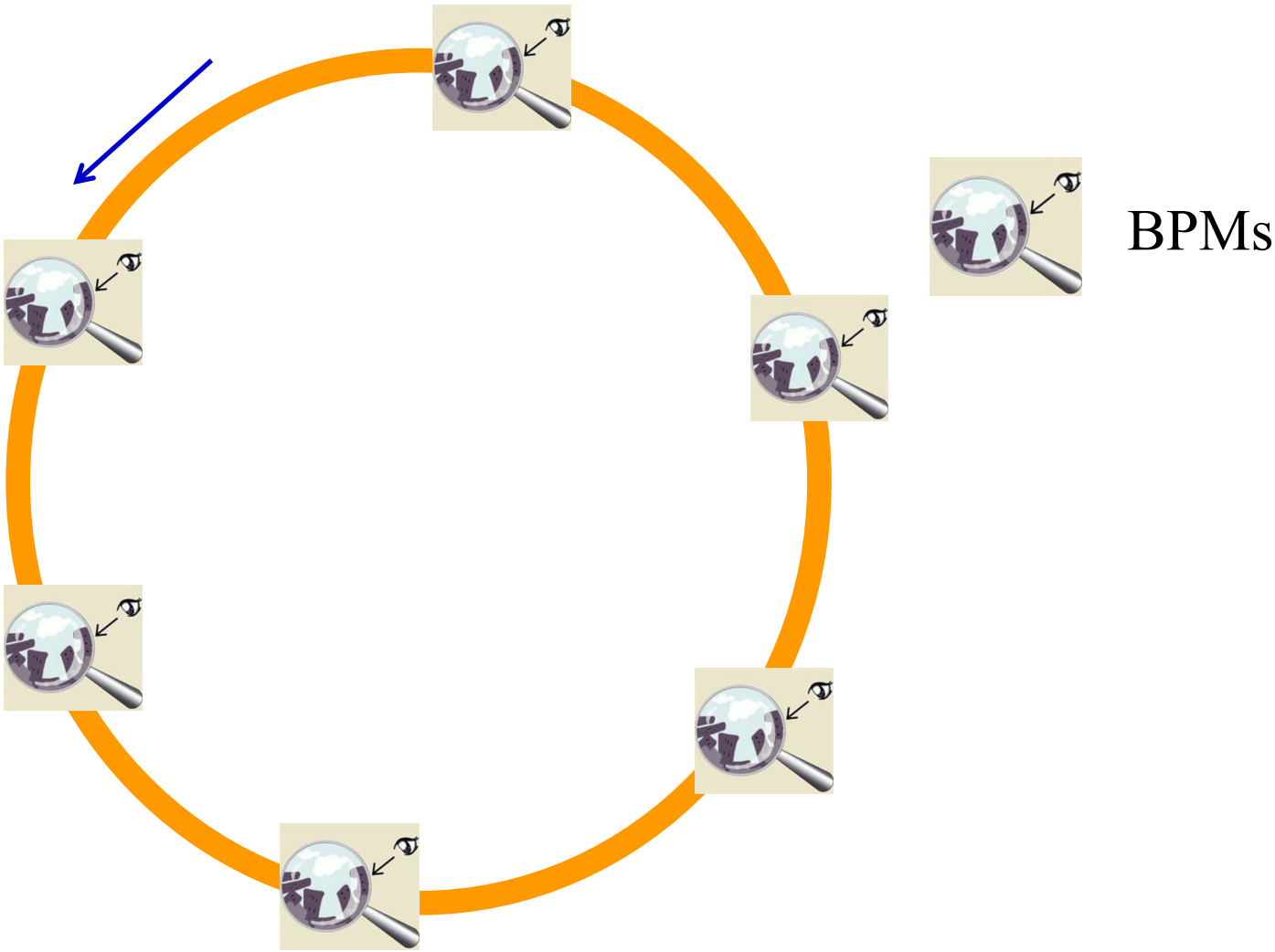

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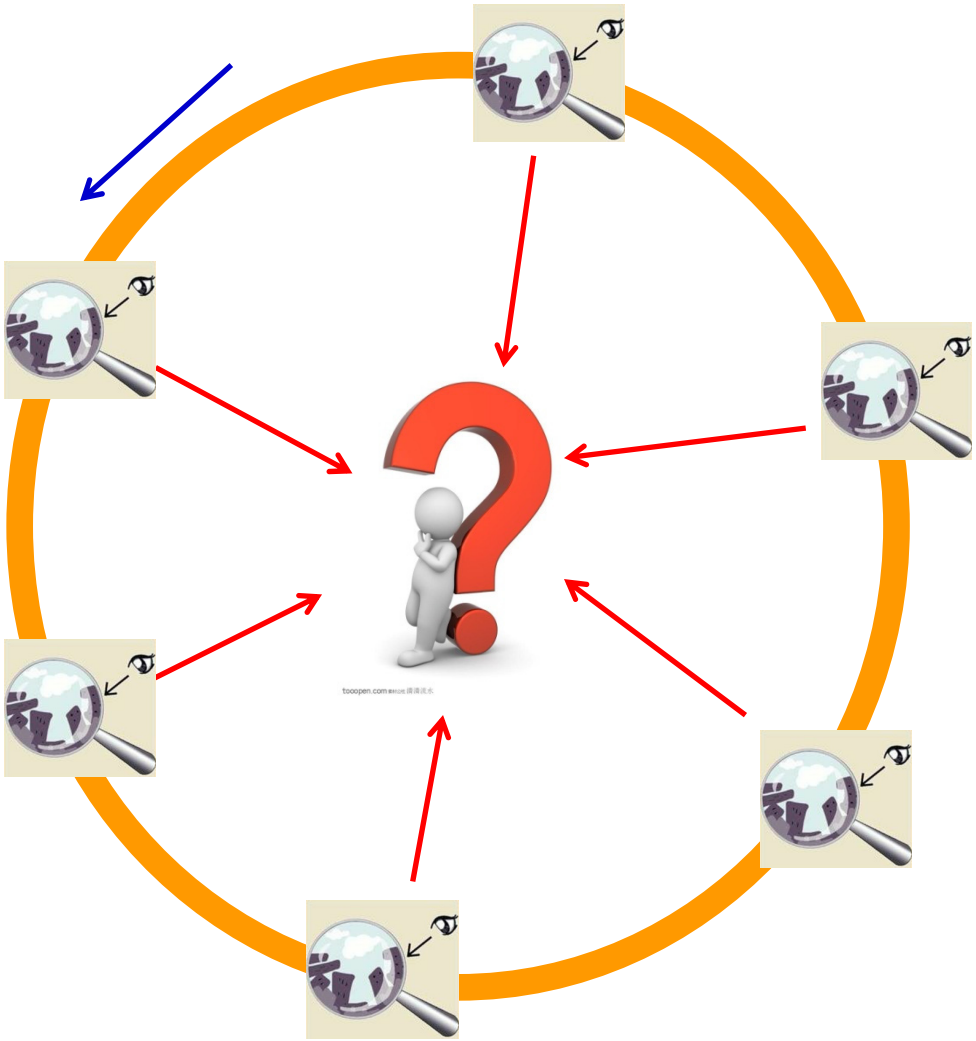

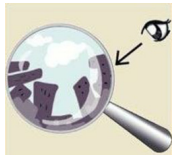

BPMs

Physics simulation, feedback logic

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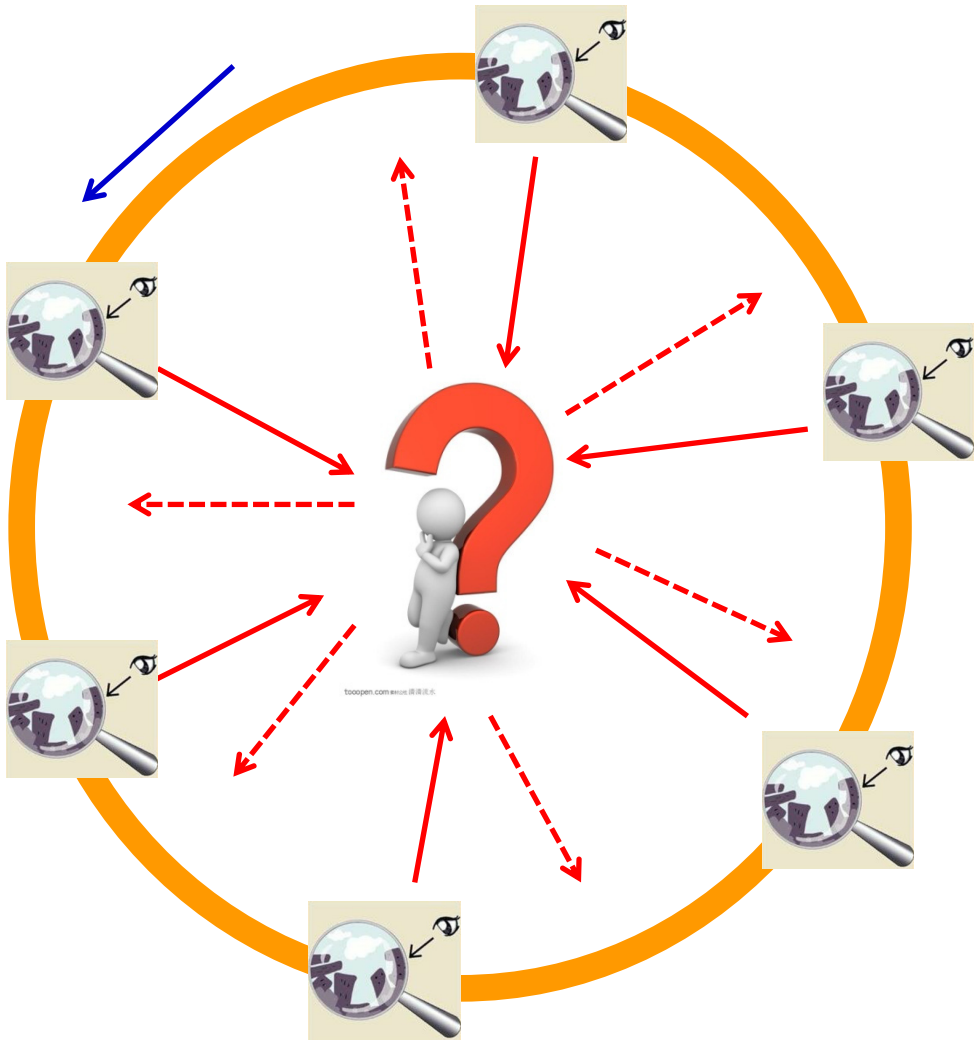

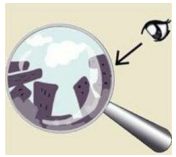

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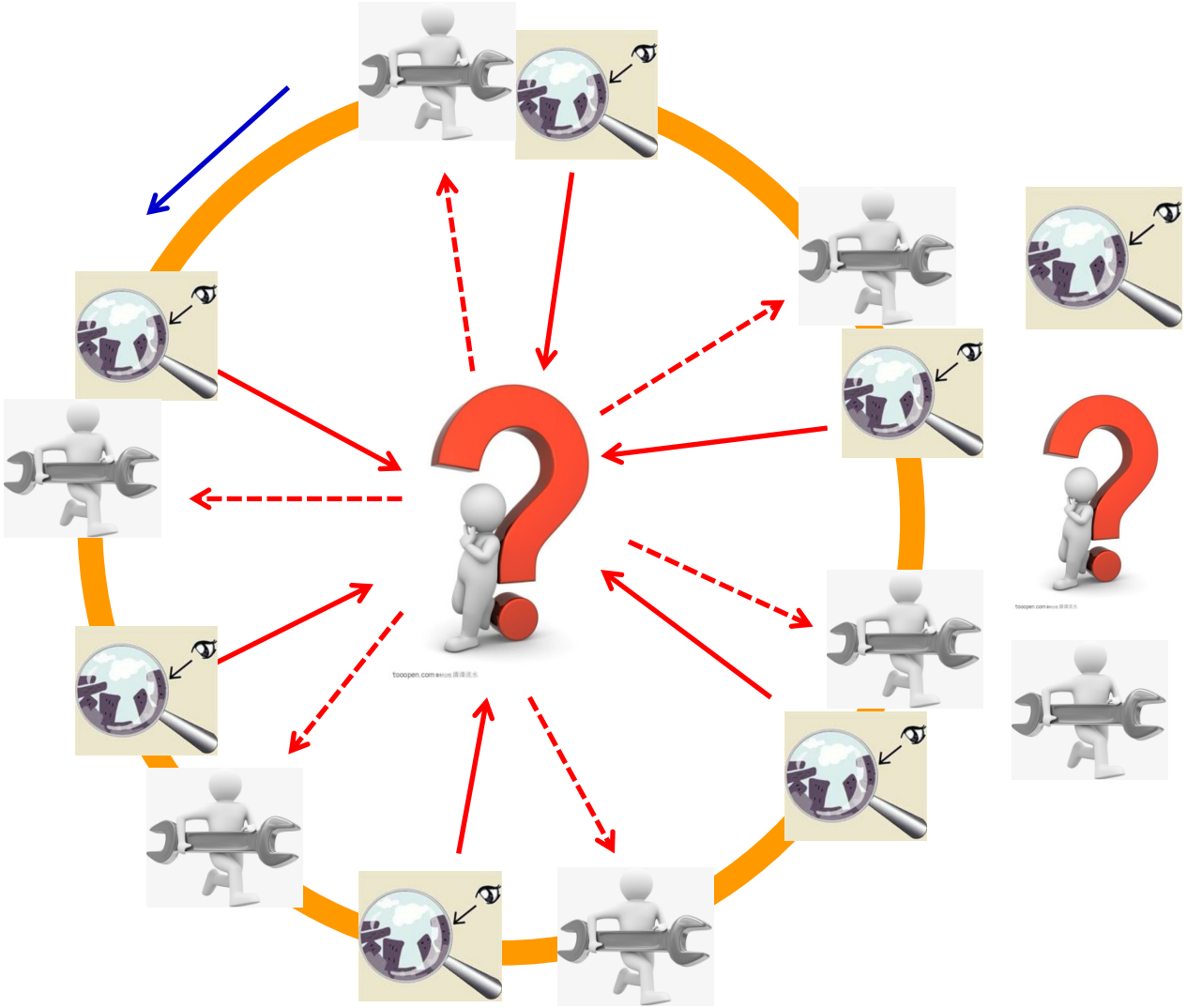

BPMs

Physics simulation, feedback logic

Power supplies, fast correctors, vacuum chambers

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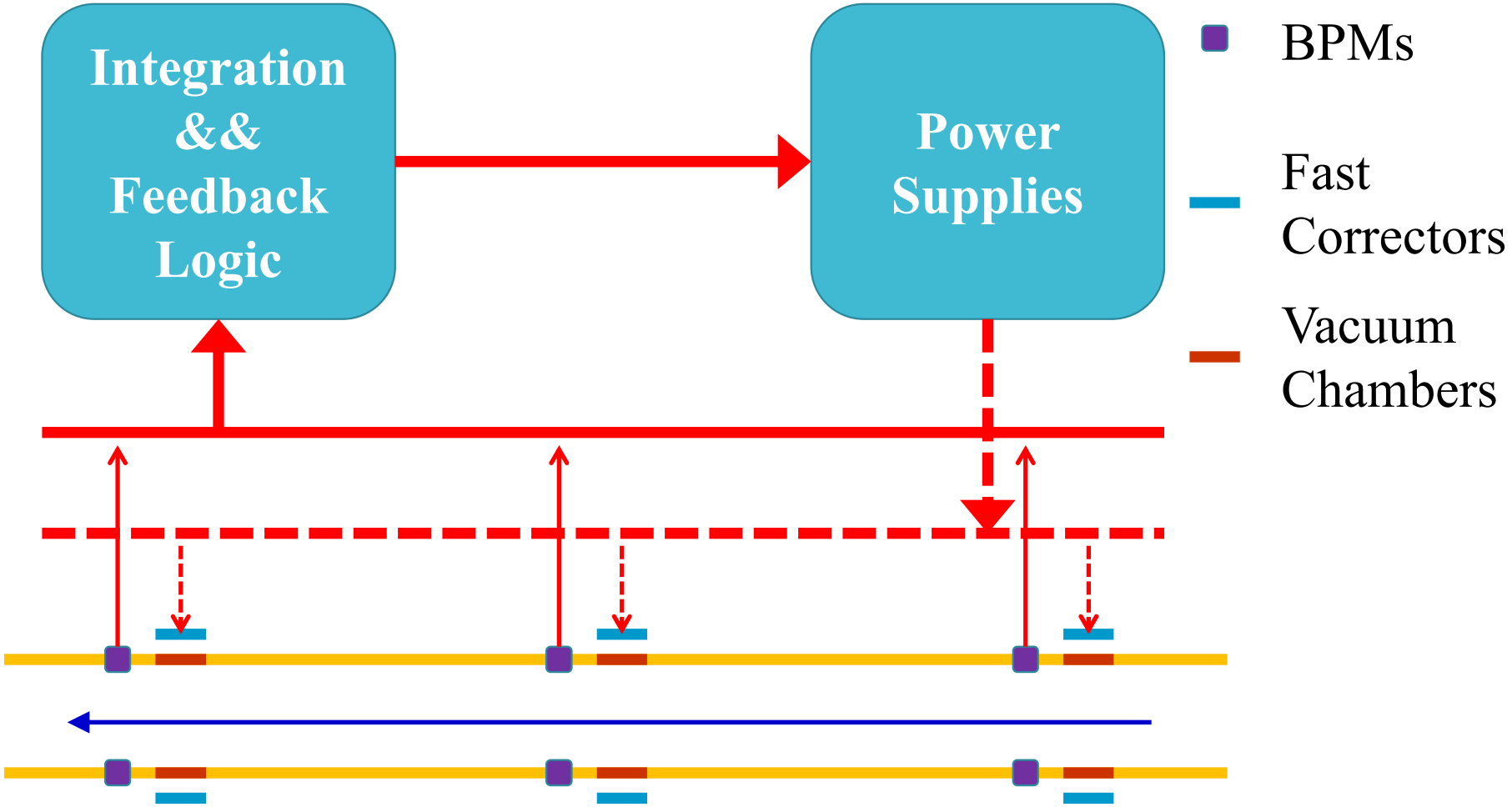
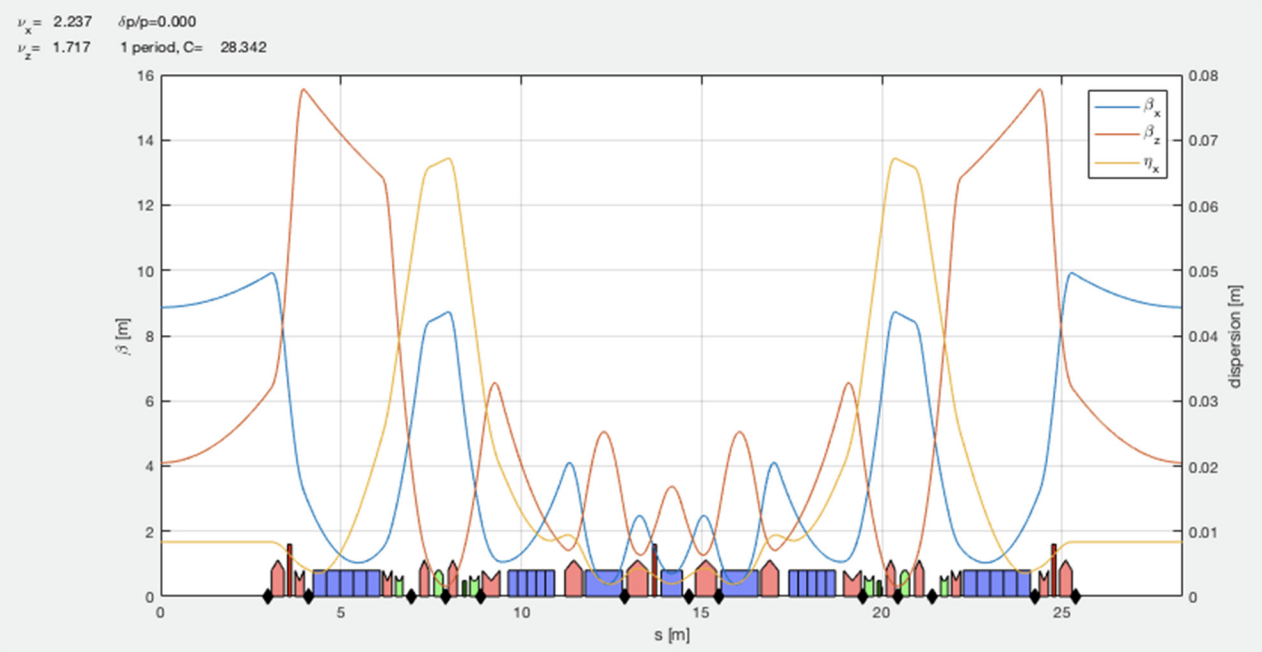


Requirement of the FOFB

- 48 identical hybrid 7BAs cell
- 12 BPMs @ 4 fast correctors per cell



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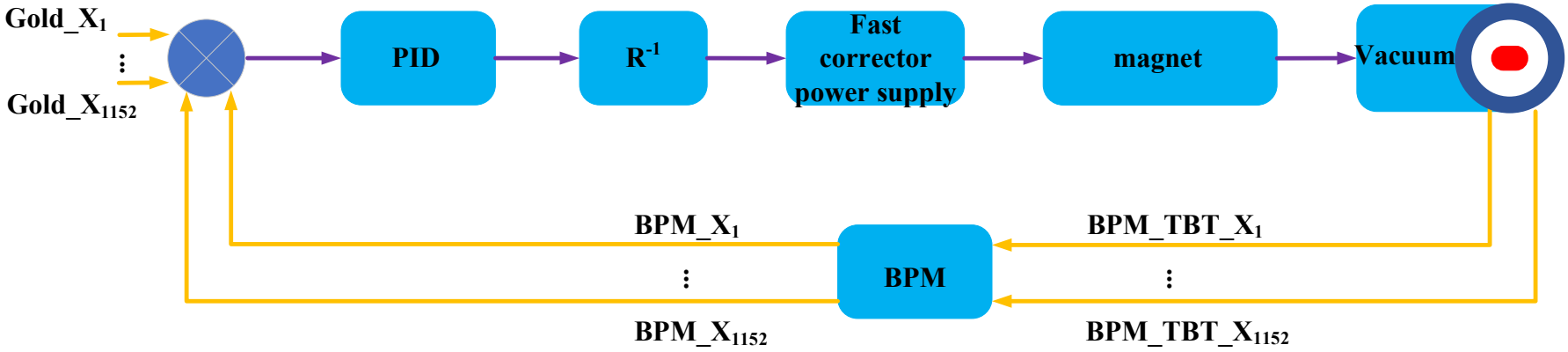
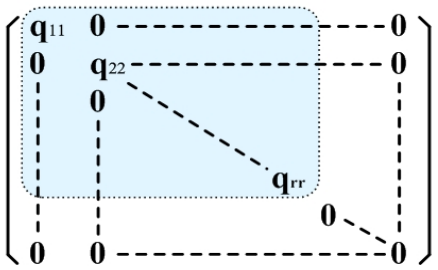


$$X_m = R * \Theta_n \xrightarrow{\text{SVD}} \Theta_n = R^{-1} X_m$$

$$R^{-1} = V\ Q \begin{bmatrix} \Sigma^{-1} & 0 \\ 0 & 0 \end{bmatrix} U^*$$



- X_m为BPM测量束流实际轨道
- R为$m \times n$响应矩阵
- Θ_n为快校正磁铁强度矢量

Requirement and Considerations

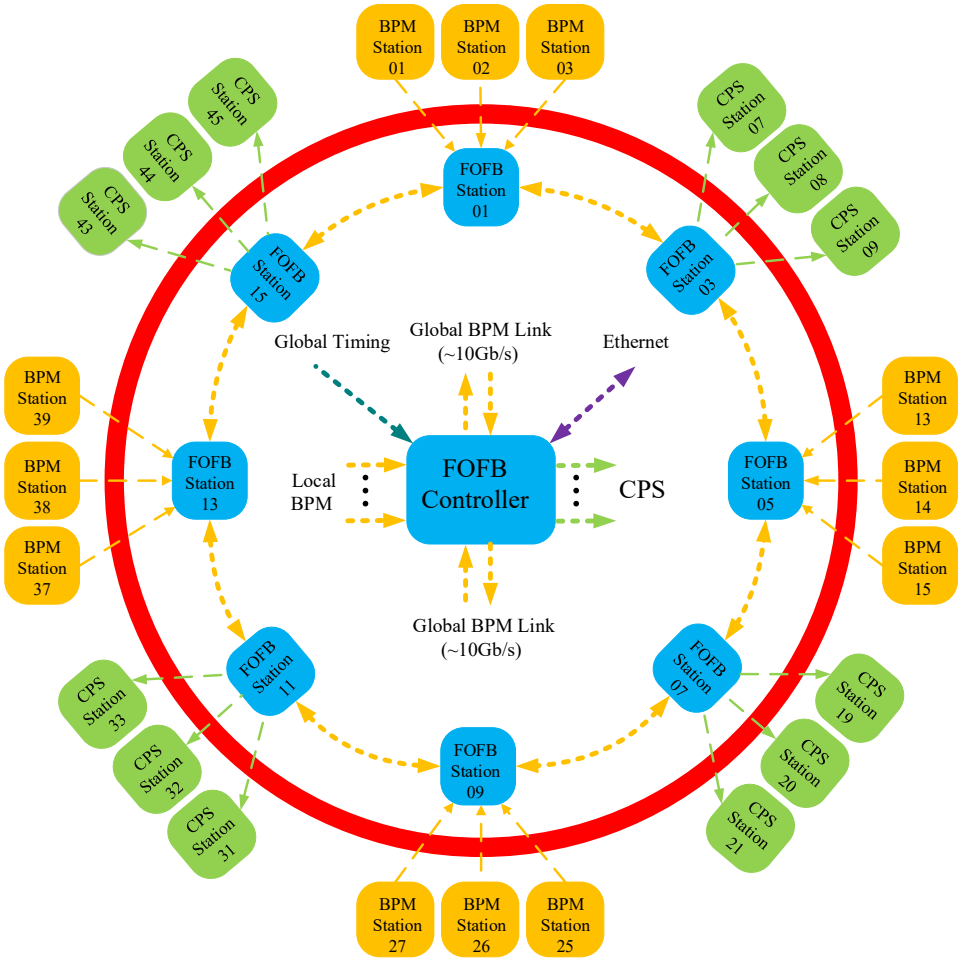
- Core chip selection : V7 from Xilinx.
- Clock frequencies of logics and DSPs, up to 1 GHz frequency is desired, at least 500 MHz.
- GTH transceivers together with optical transceivers working above 10 Gb/s for global communication, and above 5 Gb/s for BPM data collection. Multi channels will be used.

- Global timing synchronized data acquisition, transmission and logics.

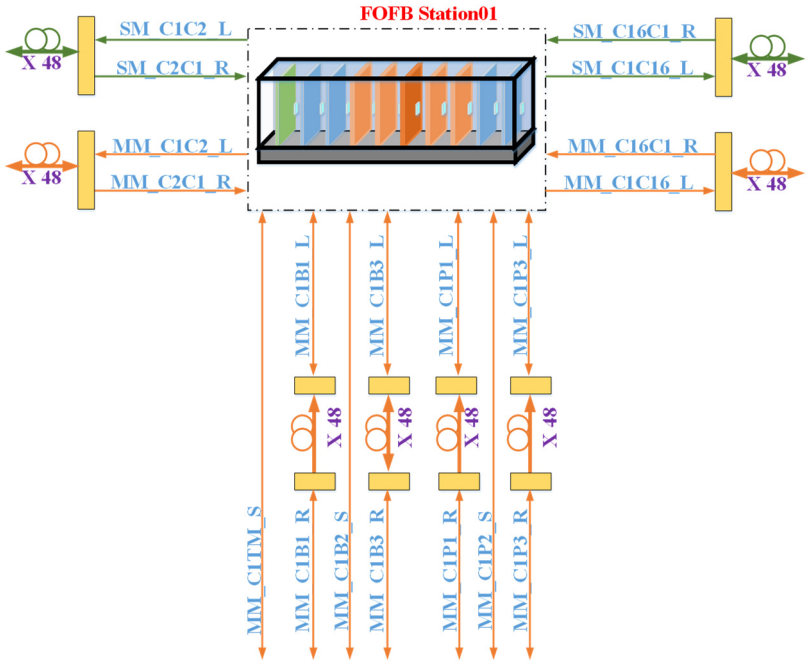
- Cable routing around the ring to minimize delay.
- Parallel data transmission to PS controllers to minimize delay.

- Ripple, effective resolution, accuracy and stability of the power supplies are very important.
- Parameters consistency for the fast correctors, power supplies and vacuum chambers are very important. The same, the best.

Architecture

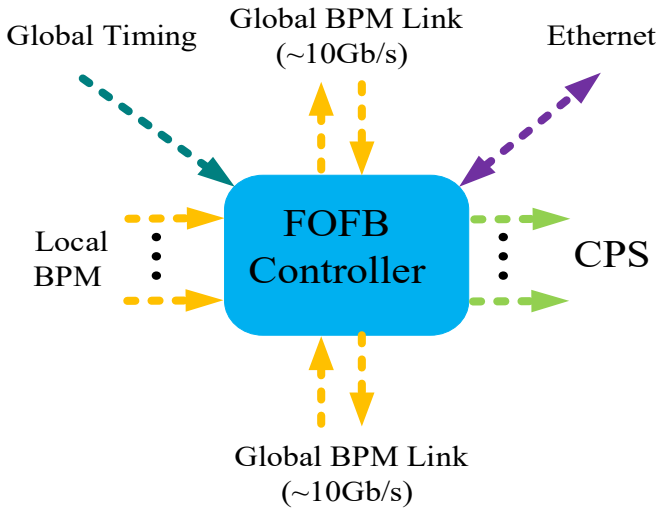


- 16 sub-stations
- 3*12 BPMs
- 3*8 fast correctors

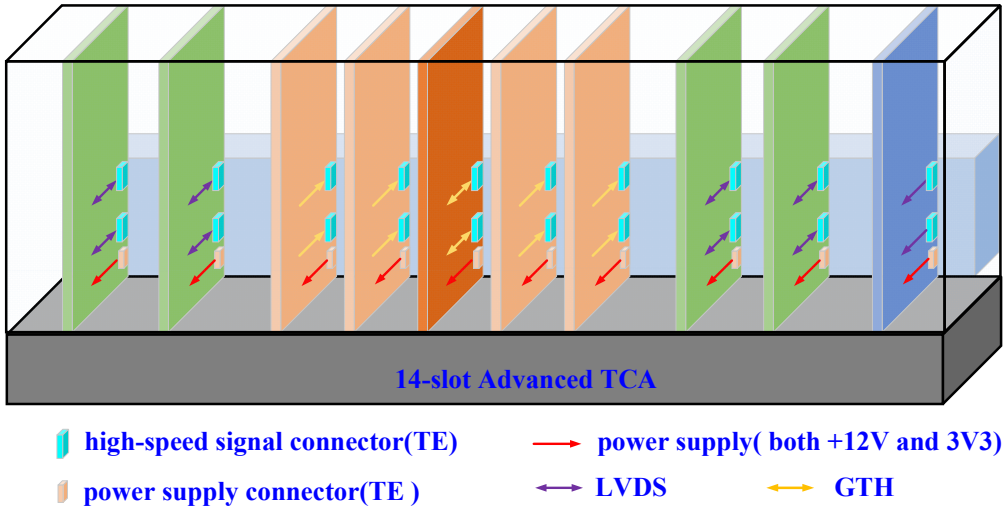


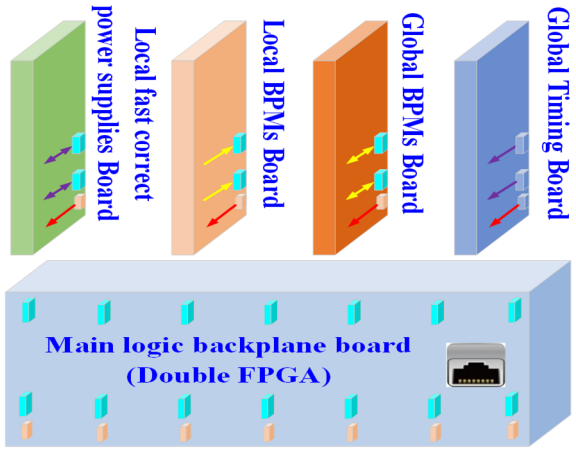
576 BPMs @192 fast corrector in both horizontal and vertical directions!

Architecture



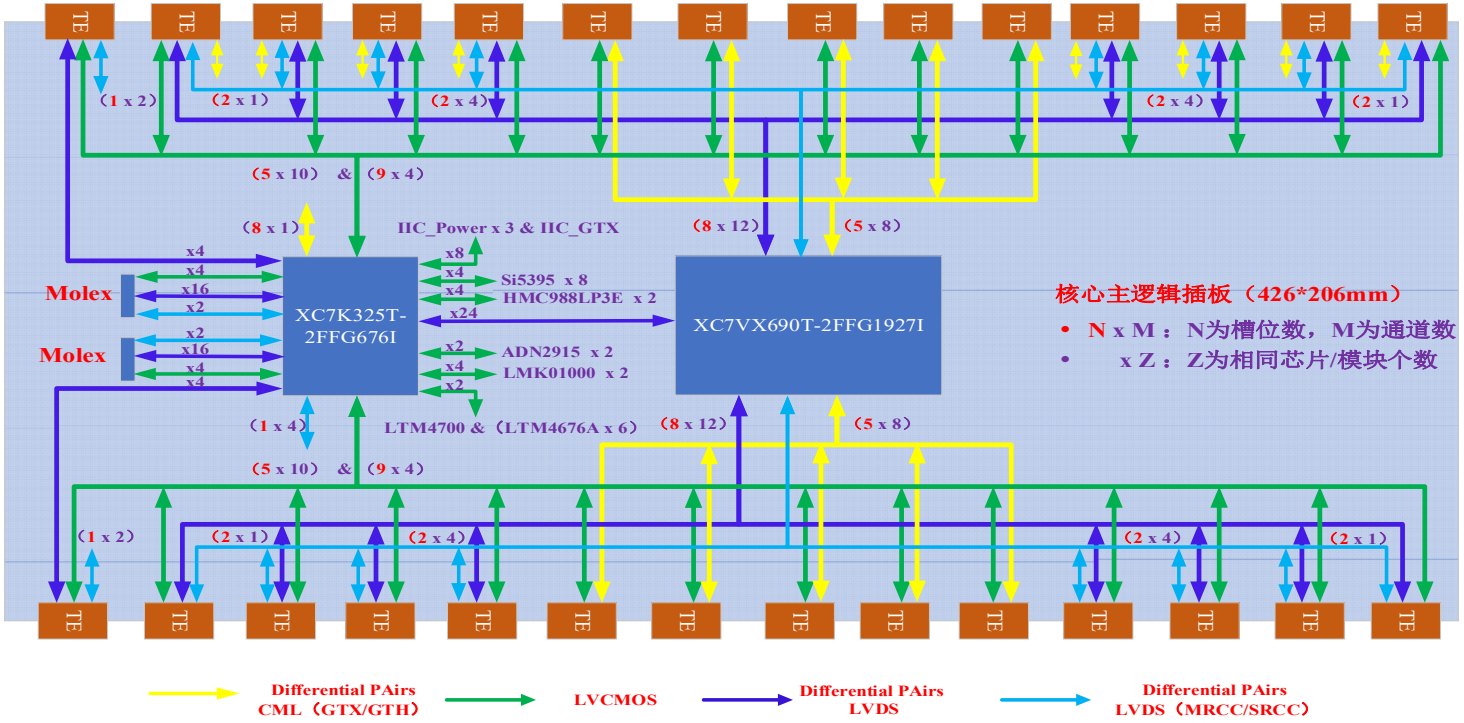
- 1 main logic backplane board
- 3 front boards for local BPMs
- 1 front boards for XBPM
- 1 front boards for global BPMs
- 4 front boards for local fast corrector power supplies
- 1 front boards for global Timing





Main Logic Backplane Board

- FPGA chip: Xilinx/XC7VX690T
- High-speed: 80 channels of GTH transceiver @10 Gb
- Clock: embedded timing / on-board 100 MHz crystal clock / LEMO clock
- LVDS: 14 slots @20 channels
- Ethernet: W5500iso



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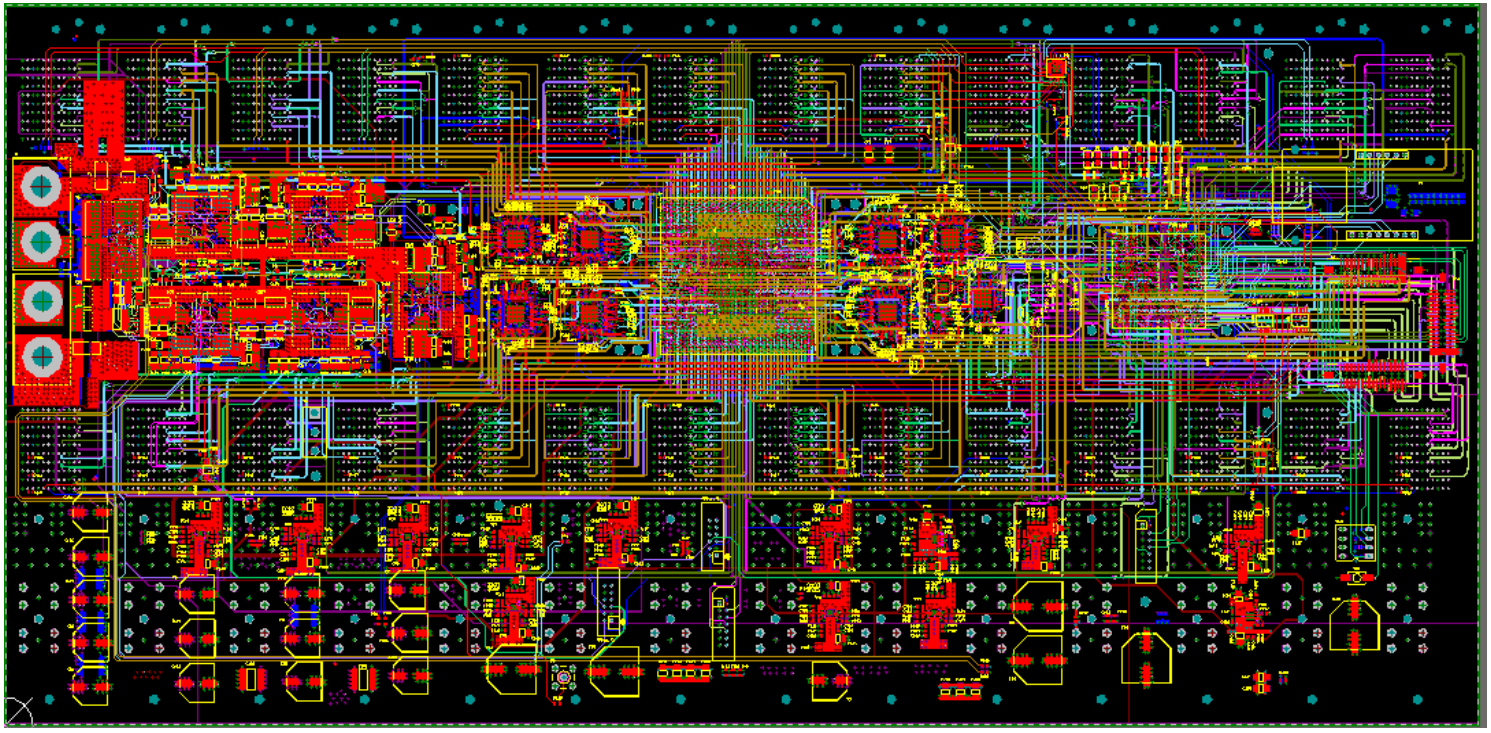
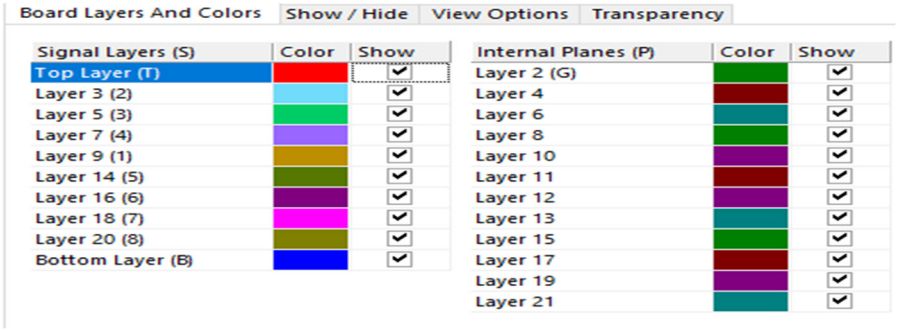
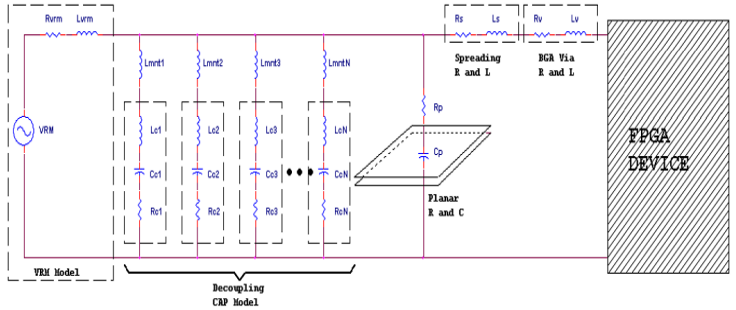


Main Logic Backplane Board

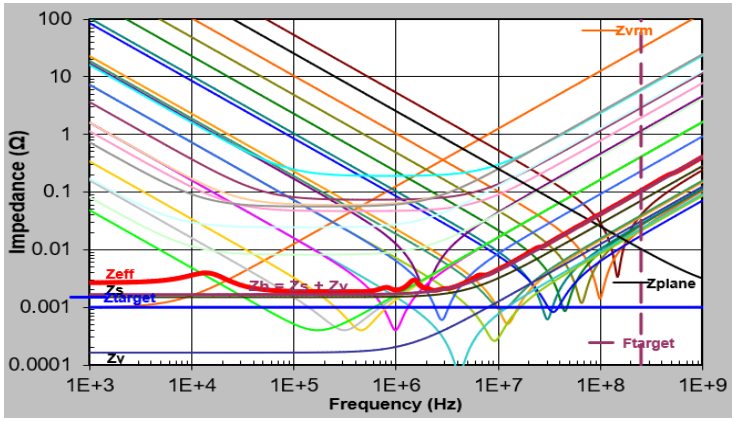
- Power Integrity:

considered such as the power stack and its division scheme, copper foil current carrying, ripple suppression and other design elements under the condition of transient current (about 100 A, 1 V@3%).





Target Impedance	Units	Value
Supply Voltage (Min)	V	1
I max	A	100
Transient Current	%	50
Vripple (+/-)	%	5
Frequency target	MHz	250
Ztarget = ΔV / ΔI	Ω	0.0010



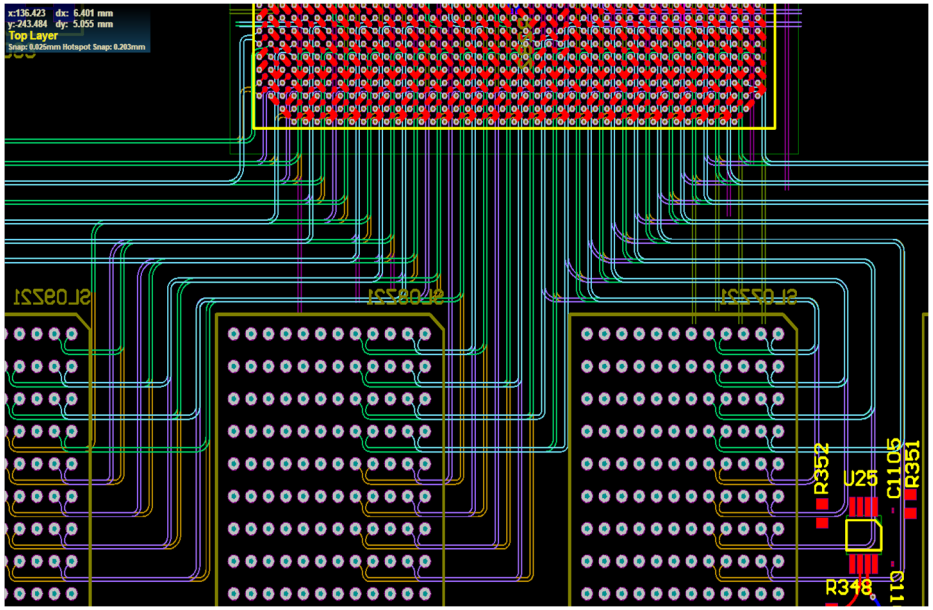
Main Logic Backplane Board

- Signal Integrity:

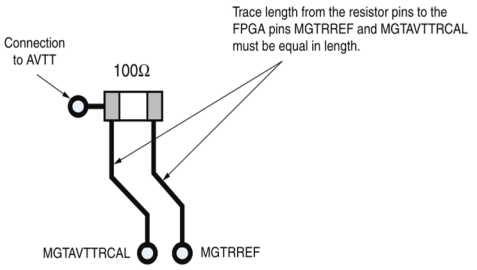
systematically studied for the characteristic impedance continuity of high-speed signals, via schemes, return path rules, nearby compensation principles, and minimizing inter-layer switching.

G-S-S-G优化模式

Signal Via + Back Drill



GTH

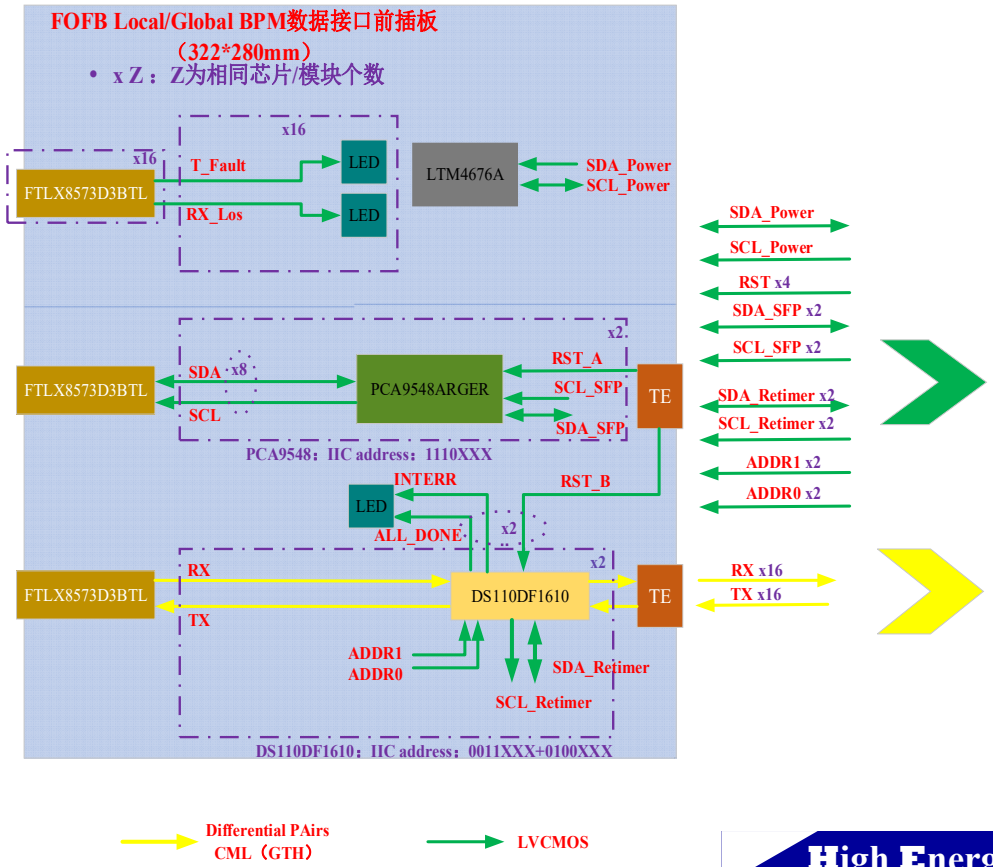


Recommend

0Ω

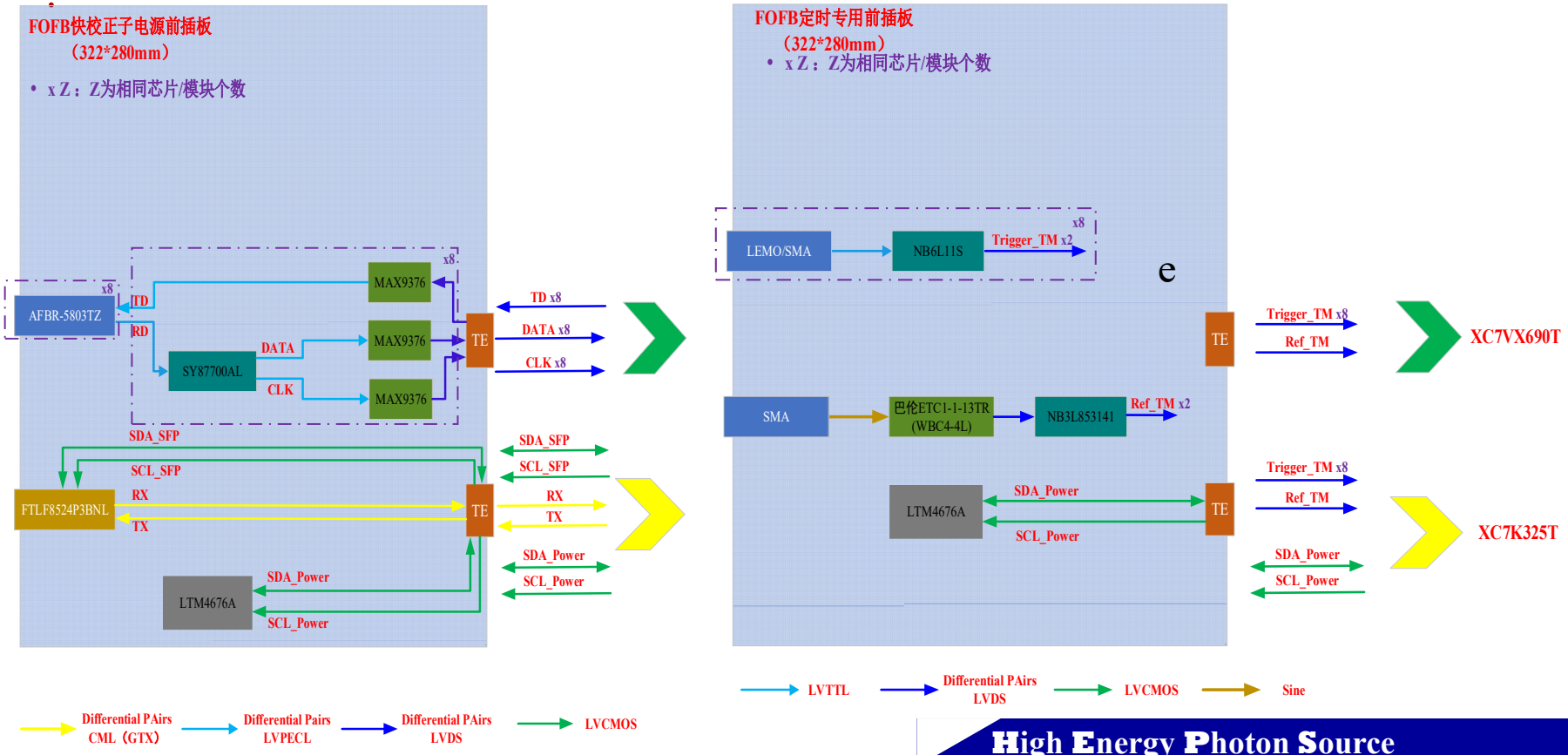
Front Board

- collect 3*12 groups of 32 bit effective data, the rate is about 2.38 Gb/s
- transmit the BPMs data, the rate is about 9.5 Gb/s



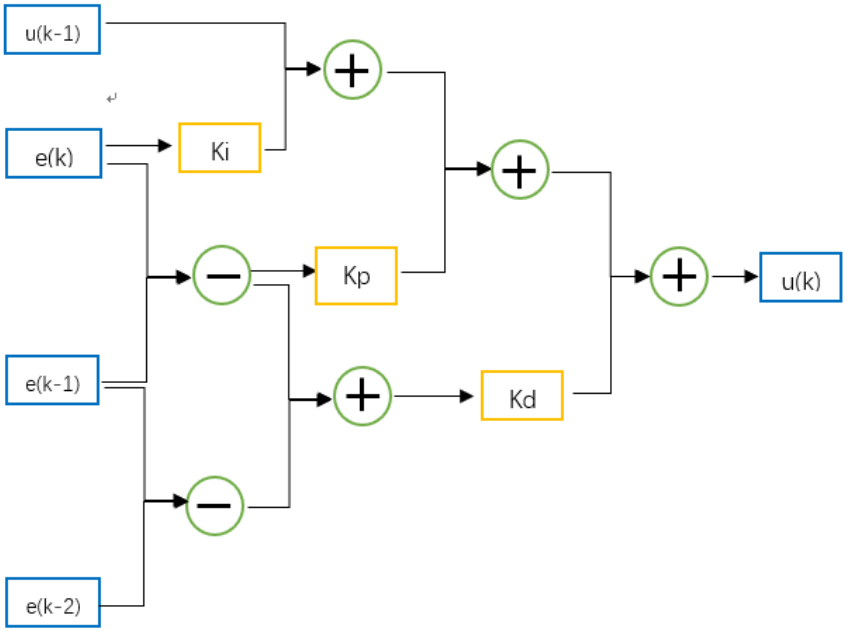
Front Board

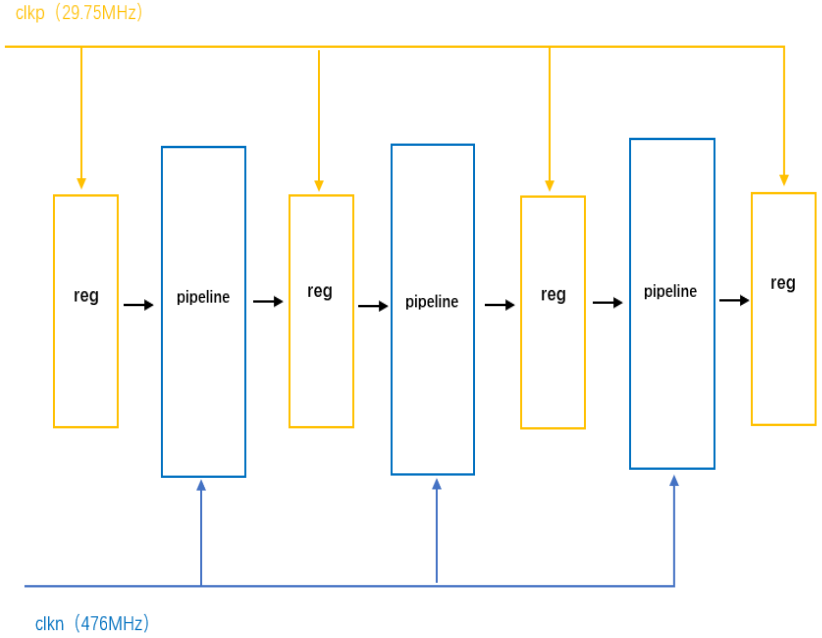
- set 3*8 groups of current for fast corrector power supply, the rate is 50 Mb/s
- receive global timing for synchronization



Logic development

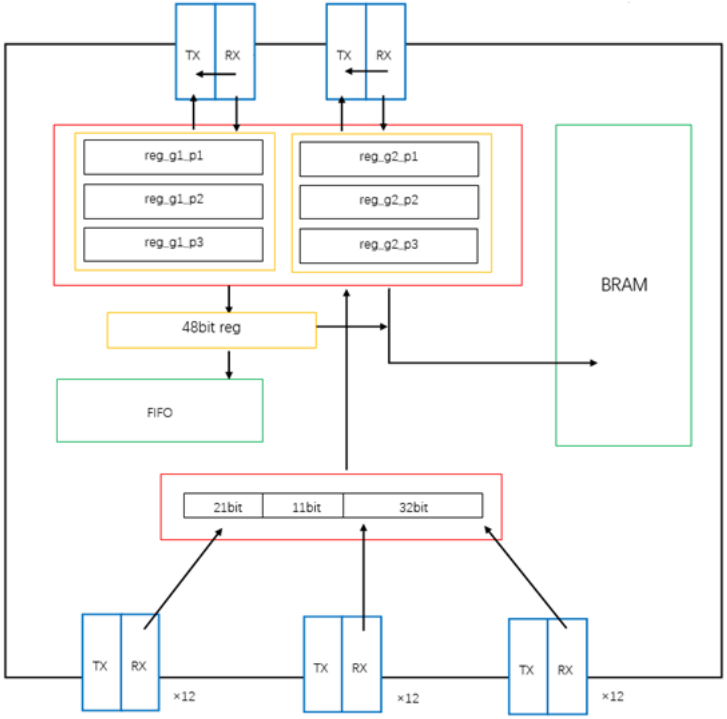
- pipeline design
- accurately control the data to reach a certain position at a certain time
- reduce latency





Logic development

- BRAM is used in the memory module design
- ensure that the data is written and read in one clock cycle
- reduce latency.



Time Consumption Estimate

- Global optical cable delay : ~5μs for ~1km cables.
- Serialization/Deserialization for half the ring : ~2μs for 16 nodes.
- Global data packets transmission : ~1μs.
- Matrix calculation : ~2μs.

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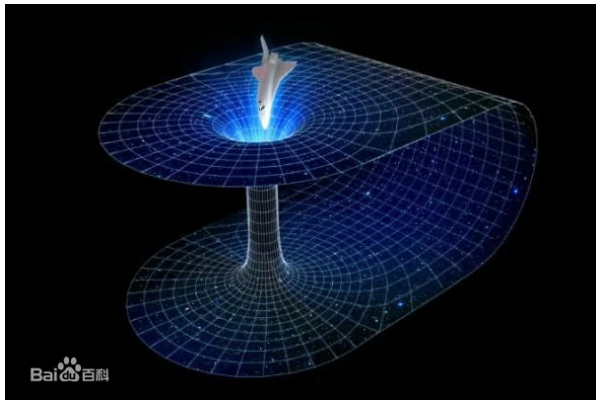

minimize latency as much as possible

Schedule

- Controllable, Orderly, and Steady!

Data	Main Mission
Apr. 1	Complete the design of all schematic
Oct. 1	Complete the design of all PCB
Dec. 1	Started joint debugging of firmware
Feb. 1	Preliminary completion of all the functional of requirements

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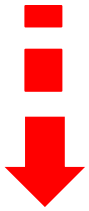

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Summary

- Preliminary design and simulation results have been carried out till now
- A bandwidth of 500 Hz can be possibly achieved, even 800 Hz
- Balance among performance, cost, difficulty, complexity, reliability, availability, scalability and maintainability.
- Tight cooperation among all related systems is the key to success

Thanks for your attention!

CSNS

HEPS