R&D Studies for the ATLAS Tile Calorimeter Daughterboard

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- I m here!!! :D

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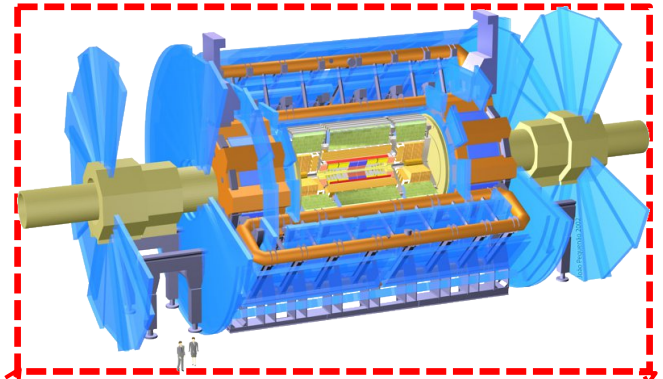
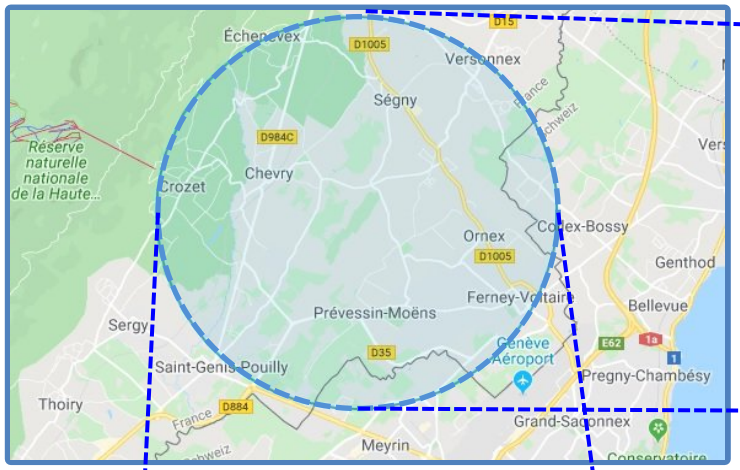
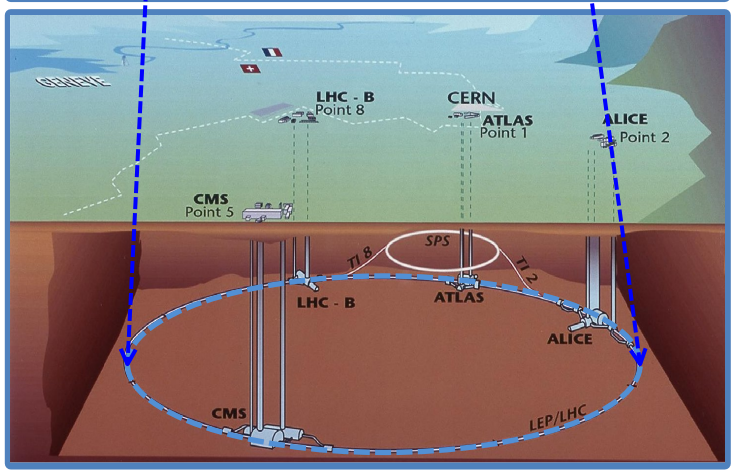
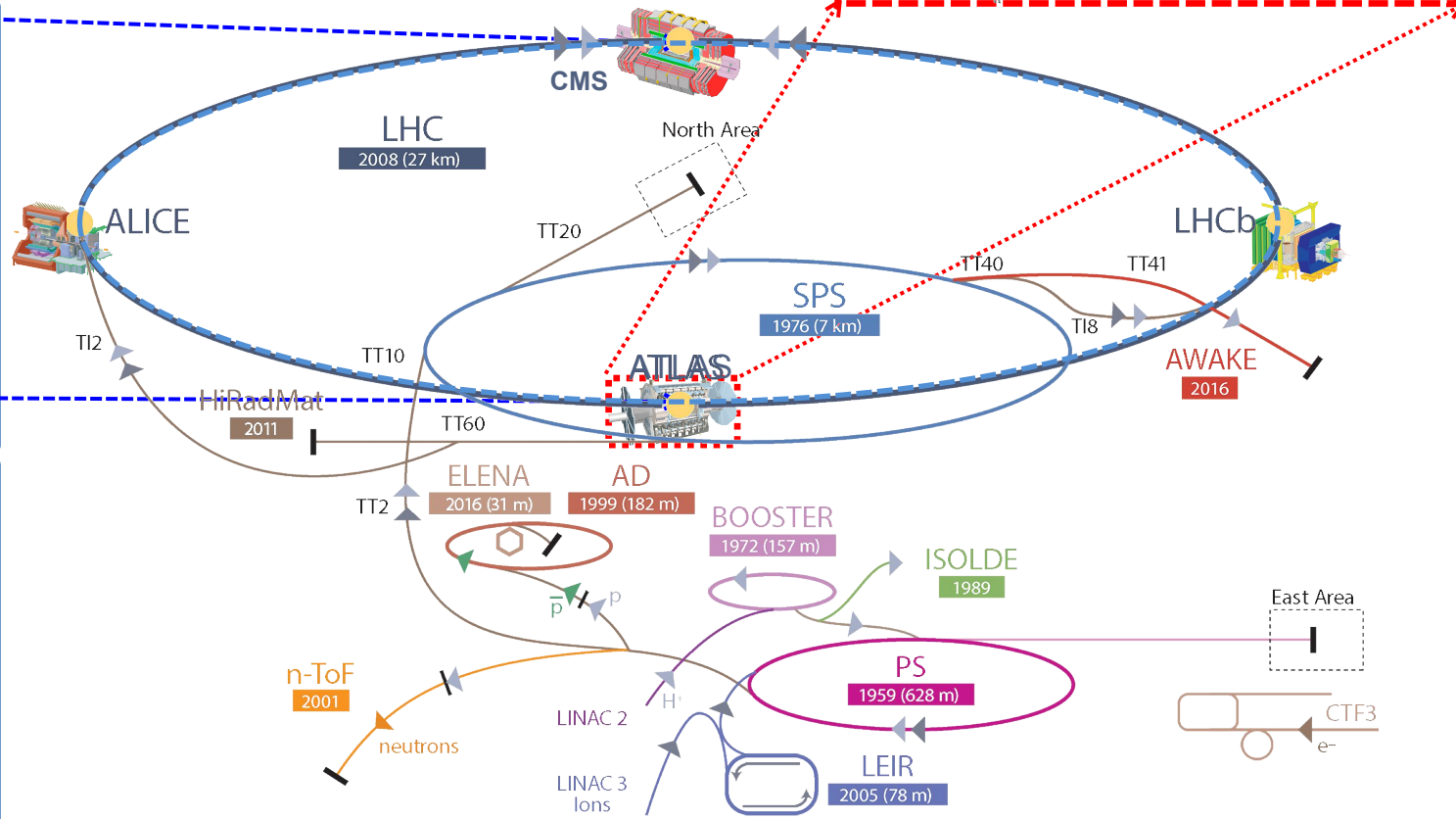
- **LHC - 27 km tunnel**, between **45 m and 170 m** beneath Swiss-French border.
- **Two parallel beam pipes** with **1232 dipoles and 392 quadrupoles**.
- **16 superconducting RF cavities** accelerate counter rotating beams up to 7 TeV.
- The beams cross in **four experimental caverns**:
  - **ATLAS** and **CMS**: General purpose to study a wide range of phenomena.
  - **ALICE**: Heavy Ion Collisions, Quark Gluon Plasma.
  - **LHCb**: Physics of b-quark interactions.









Timeline ($^{2}/_{10}$)

- Introduction
- TileCal Upgrade
- DB6 features
- DB6 concept
- ~~Timing and firmware~~
- Radiation tolerance
- Conclusions

CERN: European Organization for Nuclear Research

LHC: Large Hadron Collider
ATLAS: A ToroidaL ApparatuS

CMS: Compact Muon Solenoid
ALICE: A Large Ion Collider Experiment
LHCb: LHC beauty

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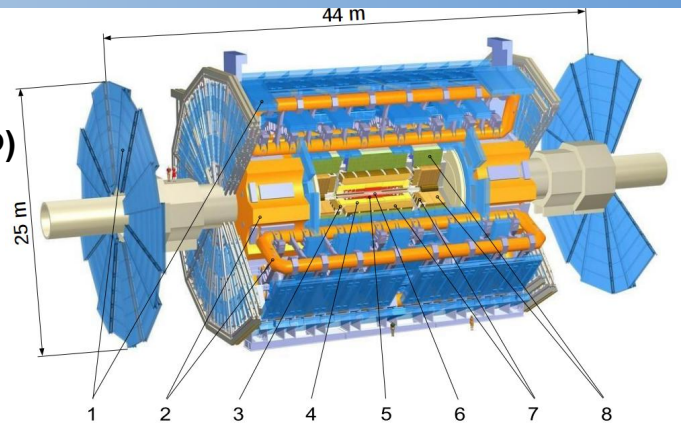
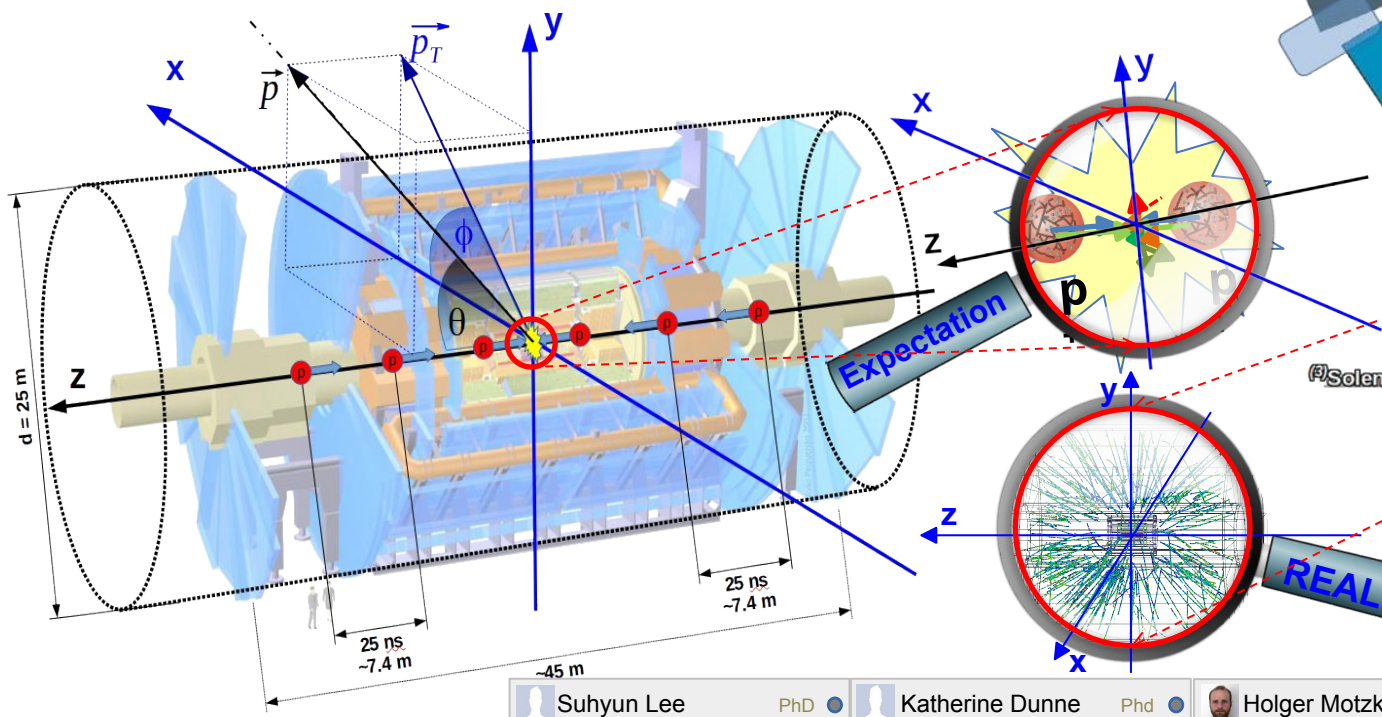
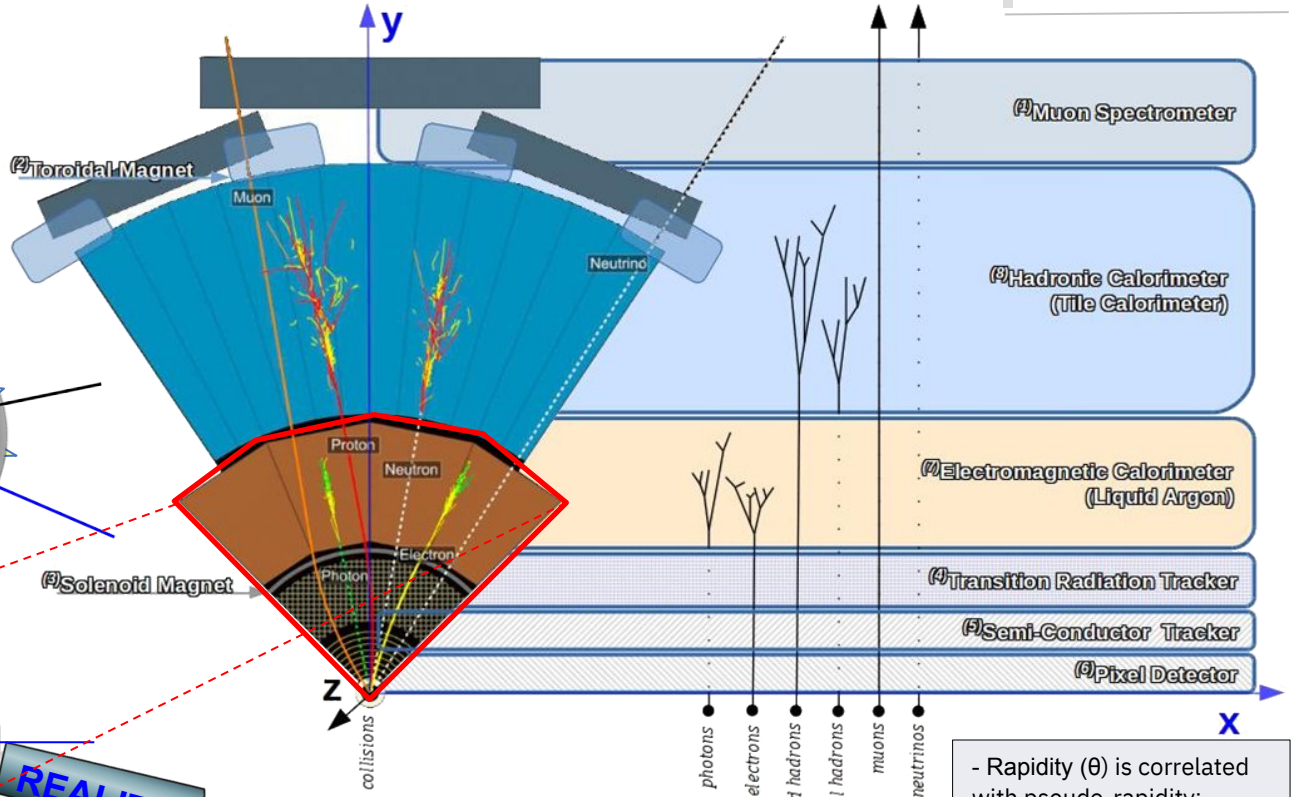
- **ATLAS Experiment** multiple detector layers from the collision center
- LHC delivers **bunches of protons** to the interaction point **every 25 ns**
- **8 detector subsystems** to cover a **large - pseudo-rapidity (η)** range and **full azimuthal angle (Φ)**
- **Inner detector: [6]Pixel detector, [5]Semi-Conductor Tracker and [4]Transition Radiation Tracker**
- **Calorimeter System: [4]Liquid Argon Calorimeter and [8]Tile Calorimeter**
- **Magnet System: [2]Solenoid magnet and [3]Toroidal magnet**
- **[1]Muon Spectrometer**

- **High Luminosity LHC (HL-LHC))** will have a **peak luminosity** of **5 x 10^{34} cm^{-2} s^{-1}** (5x LHC)
- ATLAS is undergoing upgrade R&D to:
  - **o** Cope with expected higher radiation rates
  - **o** Achieve high performance levels with acceptable trigger rates, detector occupancy, and good pile-up mitigation







- Rapidity (θ) is correlated with pseudo-rapidity:

$$\eta = \ln(\tan(\frac{\theta}{2}))$$

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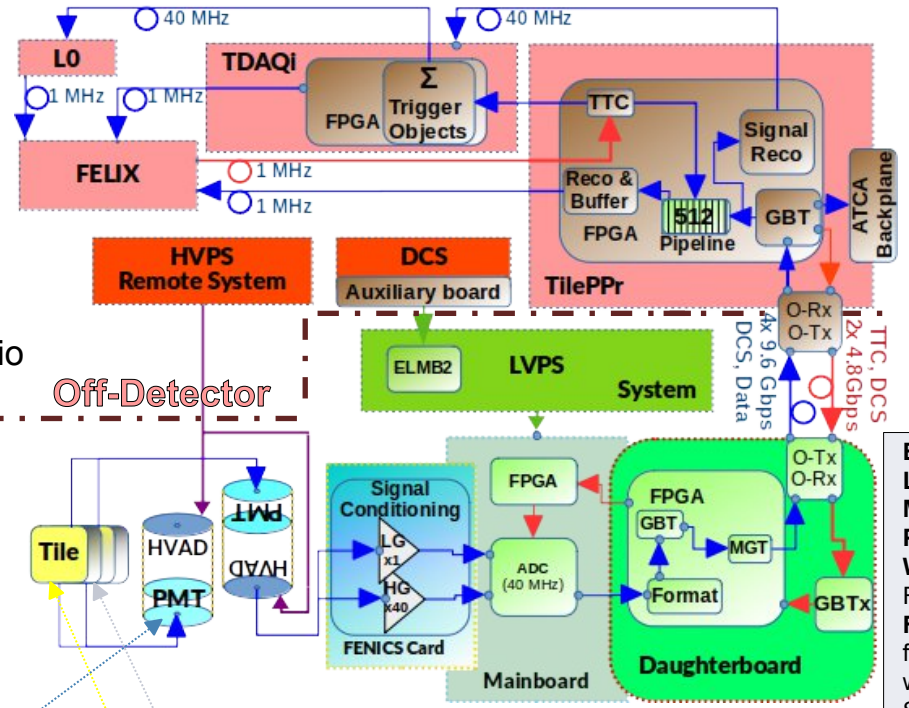
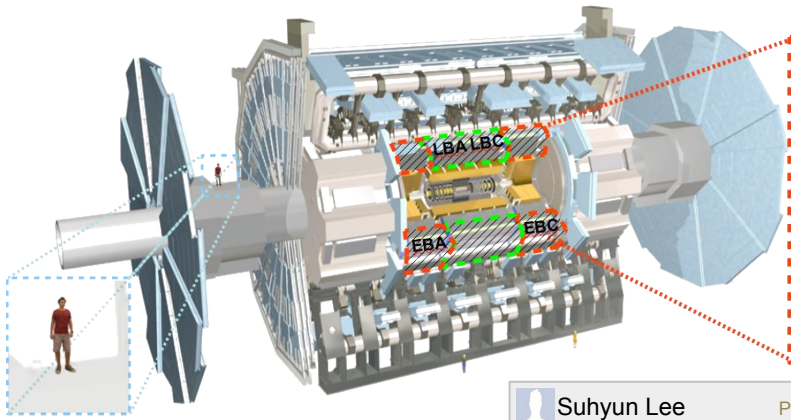
R&D studies for the ATLAS Tile Calorimeter Daughterboard.

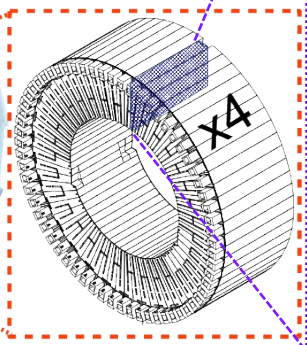
HL-LHC upgraded ATLAS Hadronic Tile Calorimeter (TileCal):
- **Sampling calorimeter** with **plastic scintillators** and **steel plates**
- Divided in **3 cylindrical barrels -> 4 partitions** (EBA, LBA, LBC,EBC)
- **Partitions sliced** in **64 wedge-shaped modules,** each housing **4 Minidrawers (MDs)** that hold the on-detector read-out electronics.

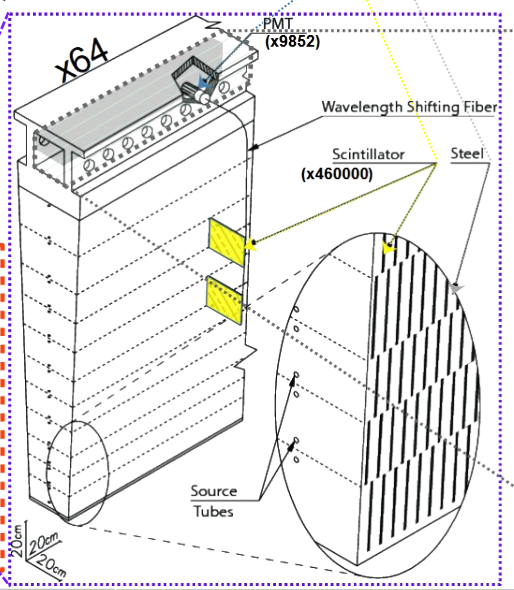
On each MD:
- up to **12 PMT blocks** convert light from the scintillators
- up to **12 FENICS** cards **condition and send two gains** of each **PMT signal** with ratio (1:40) to a **Mainboard (MB)**
- **1 MB digitizes** the FENICS cards signals **every 25 ns** and transmits them to a **Daughterboard (DB)**
- **1 DB distributes LHC synchronized timing, configuration commands and control signals** to the front-end, and **continuously transmits** the digital data from **all the MB channels** to the off-detector systems via multi-Gbps optical links

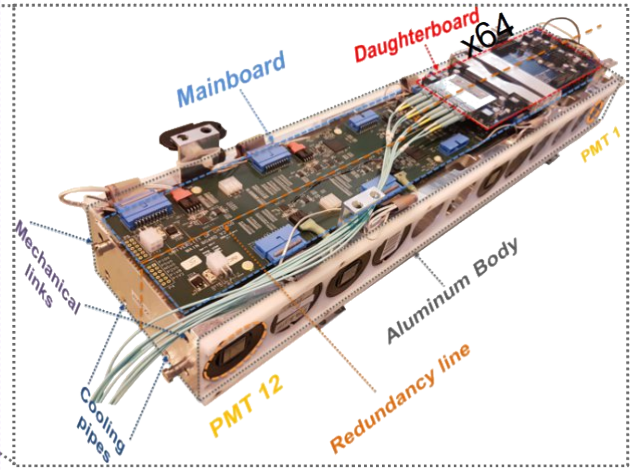
The **data received by the off-detector system** is **stored in pipelines, reconstructed and triggered-out** by:
- **Tile Preprocessors (TilePPr)**
- **Trigger and DAQ interface (TDAQi),**
- **the ATLAS Front-End Link eXchange system (FELIX)**











Timeline ($^{4}/_{10}$)

- Introduction
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- ~~Timing and firmware~~
- Radiation tolerance
- Conclusions

EBX: Extended Barrel X
LBX: Long Barrel X
MD: Minidrawer
PMT: Photomultiplier Tube
WLS: Wavelenght Shifting Fibers
FENICS: Front End board for the New Infrastructure with Calibration and signal Shaping
MB: Mainboard
DB: Daughterboard
FPGA: Field Programmable Array
GBTx: CERN Radiation toletant MBps transceiver ASIC for HEP experiments
GBT: Gigabit Transceiver protocol for HEP experiments
TilePPr: Tile PreProcessor
ATCA: Advanced Telecommunications Computing Architecture
TDAQi: Trigger and Data Aqcuitition interface
Felix: Fromt-End Link eXchange
TTC: Timing, Trigger and Control signals

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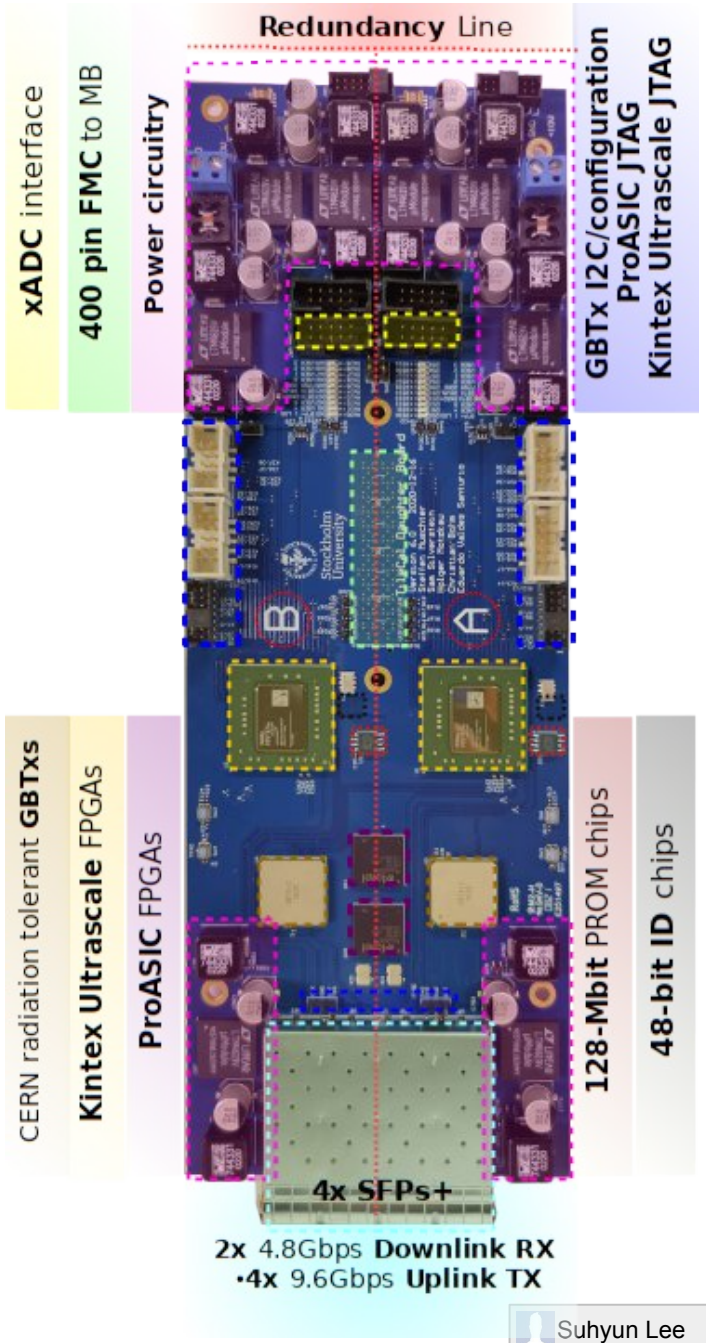

The Daughterboard revision 6:

- **Redundant** design: in two functionally equal and independently powered halves (namely half A and half B)
- **Power Circuitry:**
  - o Chained power-up sequence that delivers stable power to the different components in the order recommended by the manufacturers
  - o Fast power-cycle sequence triggered by an over-current on any of the dedicated voltages of each DC-DC converters
  - o Current monitoring interfaced to the xADCs of the KU FPGAs

- **Microsemi ProASIC FPGAs:** Translates voltages, buffers, and fans out status and remote reconfiguration signals between the GBTx ASICs and the KU FPGAs
- **Xilinx Kintex Ultrascale FPGAs:** Drives all of the DB digital logic core funtionalities
- **128-Mbit PROM chips:** Permanently stores the KU firmware
- **48-bit ID chips:** provide a unique identification number to each DB side
- **GBTx:** CERN radiation tolerant ASIC that receives configuration, commands, and high quality LHC synchronized clocks from the off-detector systems

- **GBTx I2C, ProASIC JTAG and KU JTAG interfaces:** provide in-situ configuration and monitoring interfaces for their respective ASICs
- **xADC Interfaces:** Interfaces the KU xADCs external analogue sensors for on-detector parameter monitoring (humidity, temperature, etc)
- **400 pin FMC connector:** interfaces the MB signals to the DB FPGAs
- **4x SFPs+:** interfaces the TilePPr on the off-detector systems with the DB.

Timeline ($^{5}/_{10}$)

DB: Daughterboard
MB: Mainboard
xADC: Xilinx Analogue to digital converter
FPGA: Field Programmable Array
MGT: Multi-gigabit Transceiver
ASIC: Application-specific Integrated Circuit
GBTx: CERN Radiation tolerant MGT ASIC for HEP experiments
JTAG: Joint Test Action Group
TilePPr: Tile PreProcessor
FMC: FPGA Mezzanine Card
SFP+: Small Factor Pluggable
PROM: Programmable Read-only Memory

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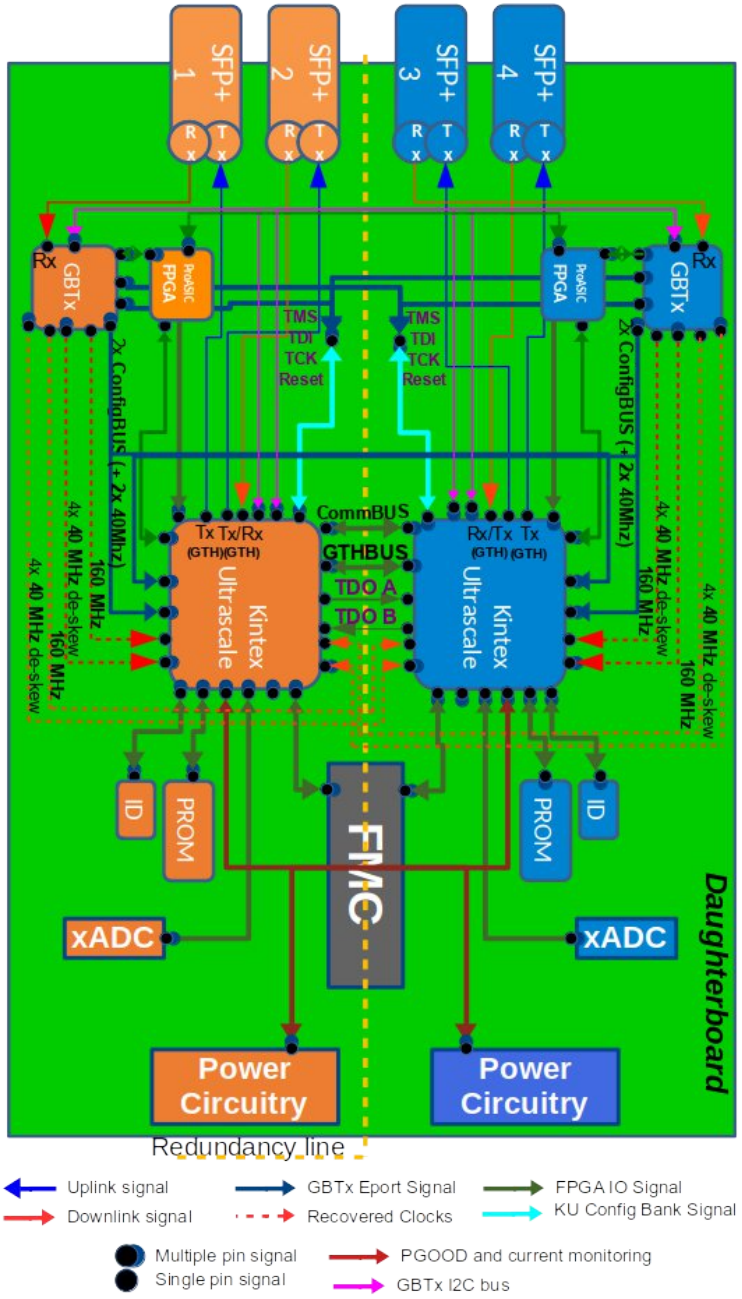

The Daughterboard revision 6:

- 2x independent redundant sides, each with:

- **o 2x SFP+s** with:
  - **> 2x Tx <= KU GTH MGTs**
  - **> 1x Rx => GBTx** (same side)
  - **> 1x Rx => KU GTH MGT** (same side)
- **o 1x GBTx** delivering**:**
  - **> Recovered clocks:**
    - **> 2x 160 MHz => KU FPGAs GTH MGTs refclks**
    - **> 8x 40 MHz de-skew** of which**:**
      - **> 4x 40 MHz Charge Injection calibration system de-skew**
      - **> 4x 40 MHz ADC-readout de-skew**
    - **> 2x 40 MHz => Configuration BUS (ConfigBUS) refclk**
    - **> 1x 40 MHz** testclock for ProASIC FPGA (same side)
  - **> 2x** (**8xConfigBUS** datapath)
  - **> Reset and JTAG signals** to KU FPGAs of both sides via the ProASIC FPGAs

- 2x KU FPGAs, each:

- **o** Interconnected with each other via:
  - **> Gigabit Transceiver BUS (GTHBUS) (MGTs)**
  - **> Communication BUS (CommBUS) (ISERDES/OSERDES)**
- **o** Interconnected with the **MB quadrants via a common FMC connector:**
  - **>** to deliver **front-end configuration** and **clocks,**
  - **>** to receive **clocks, data and monitoring signals**.
- **o** Interfaced with **Serial ID** and **configuration PROMS**
- **o** Managing **xADC** and **Cs interfaces**
- **o** Receiving opposite side **PGOOD** and **current monitoring**
- **o** Providing **independent I2C interfaces** to **both GBTxs**

- 2x Microsemi ProASIC:

- **o** to buffer **KU reset** and **JTAG signals** from both **GBTx ASICs**
- **o Voltage level translation** (SLVS->LVCMOS, LVCMOS1v8->LVCMOS1v5->LVCMOS2v5)

KU: Kintex Ultrascale
GTH: Xilinx Gigabit Transceiver H series
MGT: Multi-gigabit Transceiver
ISERDES/OSERDES: Xilinx FPGA Serializer-Deserializer technology
GBTx: CERN Radiation tolerant MGT ASIC
TMS/TCK/TDI/TDO: JTAG signals
PROM: Programmable Read-only Memory
PGOOD: Voltage stability signal provided by the DC-DC converters

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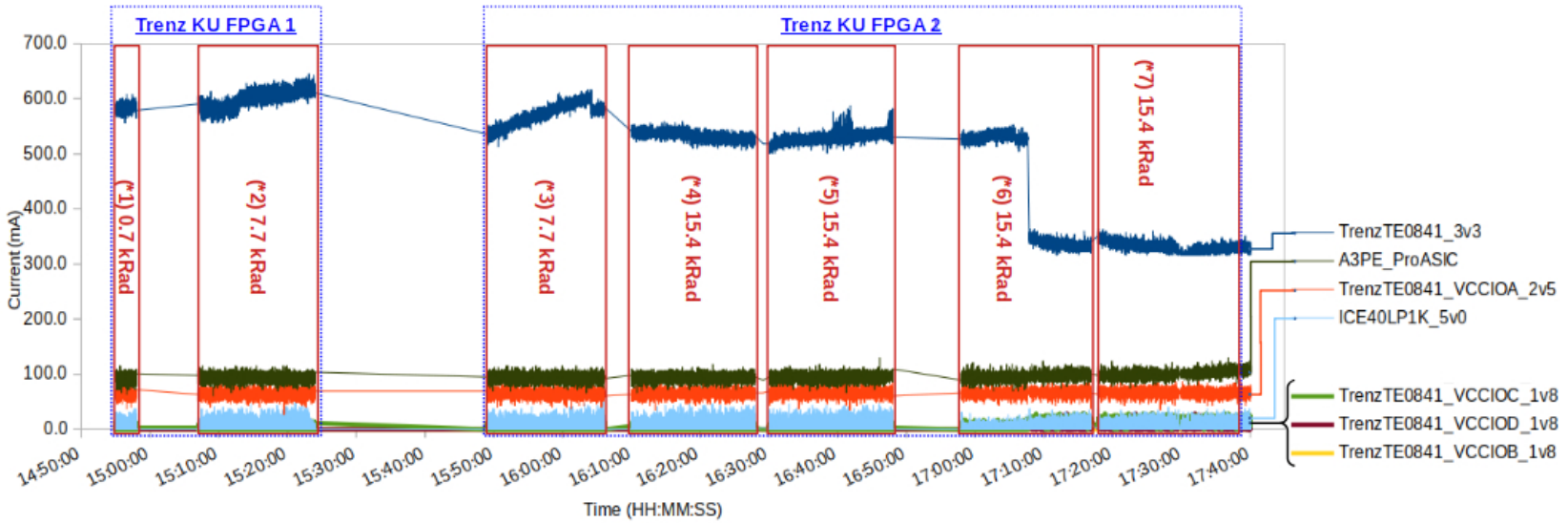
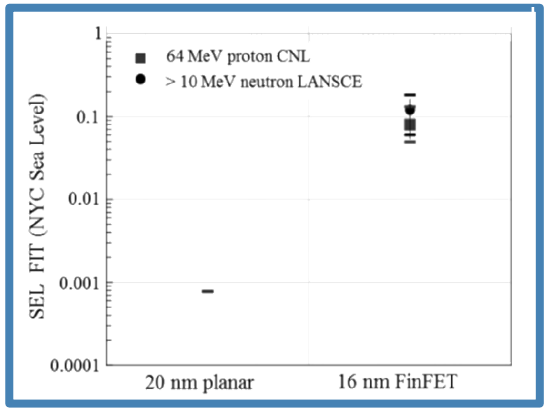
Radiation tolerance of Daughterboard Revision 6?

- **SEE -> 9x10^{12} n cm^{-2} (includes safety factors)**
  - **SEL** -> All components successfully passed the SEL test:
    - 2 Trenz TE0841 micromodules equipped with the **XKCU035 FPGA** -> Used in DB6
    - ICEBLINK LP1K evaluation board equipped with **iCE40LP1K** -> Candidate to be used in DB6
    - Microsemi A3PE starter kit equipped with **A3PE1500-PQ208** FPGA -> **A3PE250** Used in DB6
  - **SEU** -> SEU Mitigation includes:
    - Use of the **GBT protocol with Forward Error Correction (FEC) on the downlink** where up to 16 consecutive incorrectly-received bits can be corrected on every 120-bit GBT word
    - Use of redundant uplinks with **GBT protocol with (CRC)**
    - **Triple Mode Redundancy (TMR)** on the GBTx, the ProASIC firmware and the KU firmware wherever possible
    - **Xilinx Soft Error Management (SEM) IP core** on the KU FPGA preliminary tests showed 10^6 SEUs per 10^9 p cm^{-2}, ~ 7 times the SEUs seen during the KU+ tests (10^6 SEUs per 10^9 p cm^{-2}). These are acceptable rates ranging between the K7 FPGAs and the KU+ FPGAs
    - SEU tests planned for 2022 to assess KU FPGA SEU rates and un-correctable error mitigation strategies



XILINX FPGA DEVICE FAMILY FUNCTION BLOCK CROSS SECTIONS

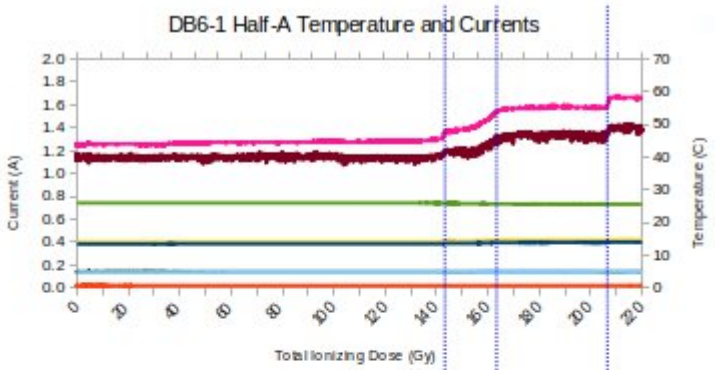
Device Family	SRAM Logic Configuration (cm^2/bit)	Flip Flop (cm^2/bit)	DSP Block (cm^2/DSP)	BRAM (cm^2/bit)
Virtex-II	33.6x10^{-15}	88.0x10^{-15}	78.0x10^{-12}	4.70x10^{-15}
Virtex-4	15.6x10^{-15}	66.0x10^{-15}	10.0x10^{-12}	4.20x10^{-15}
Virtex-5	19.5x10^{-15}	24.0x10^{-15}	10.0x10^{-12}	2.44x10^{-15}
Virtex-6	9.75x10^{-15}	7.40x10^{-15}	5.40x10^{-12}	1.74x10^{-15}
Kintex-7	5.20x10^{-15}	5.34x10^{-15}	0.98x10^{-12}	1.31x10^{-15}
UltraScale	1.89x10^{-15}	2.05x10^{-15}	0.94x10^{-12}	2.52x10^{-15}
UltraScale+	0.12x10^{-15}	0.30x10^{-15}	<0.20x10^{-12}	0.59x10^{-15}

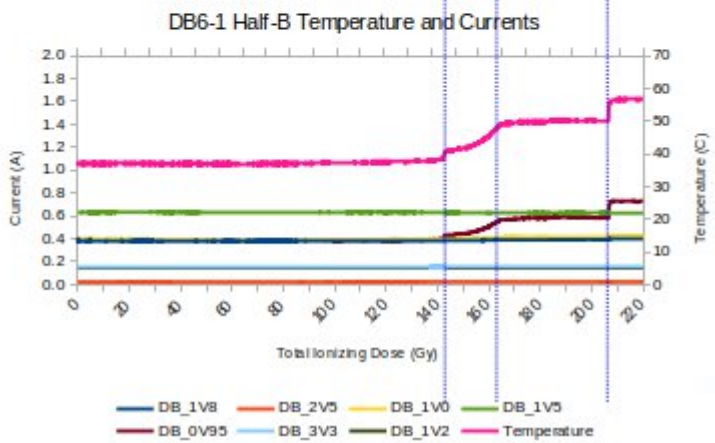


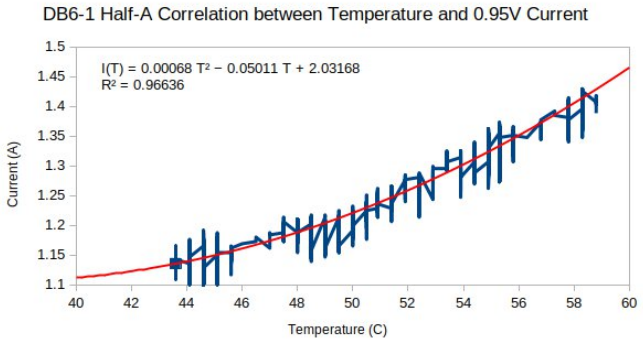
KU: Kintex Ultrascale
KU+: Kintex Ultrascale+
K7: Kintex 7
FEC: Forward Error Correction
TID: Total Ionizing Dose
SEE: Single Event Effects
SEL: Single Event Latchup
SEU: Single Event Upset
TMR: Triple Mode Redundancy
SEM: Xilinx Soft Error Management IP Core

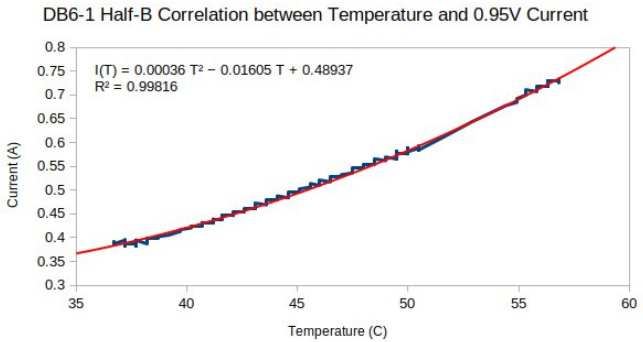
Radiation tolerance of Daughterboard Revision 6?

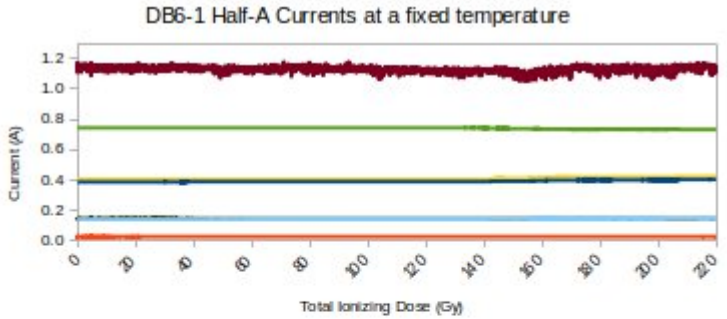
- **TID -> Highest expected: 2.16 kRad -> 2xDBs**
  - Most components tested during DB5 TID tests, tests planned for end of 2020 to cover the new components included in DB6
  - ProASIC preliminary tests during SEL tests were sucessful -> ~72 krad delivered by 266 MeV proton beam
  - Dedicated TID test at CERN CC60 facility:
    - **DB6-1 fast irradiation @3.37 Gy/h to 220 Gy → ~2.5 days**
      - None of the DB components were damaged by the deposited TID
      - VCCRAM and the VCCINT of the KU FPGA 0.95 V current increase at around 140 Gy correlated to the failure of the active components of the fan used to cool down the FPGAs
      - Correlation between the 0.95 V current and the FPGA temperature -> a second degree polynomial regression

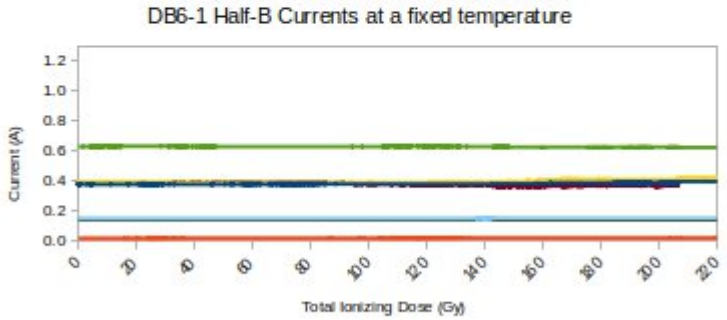












KU: Kintex Ultrascale
KU+: Kintex Ultrascale+
K7: Kintex 7
FEC: Forward Error Correction
DBX: Daughterboard revision X
TID: Total Ionizing Dose
NIEL: Non-Ionizing Energy loss
MGT: Multi-gigabit Transceiver
SEE: Single Event Effects
SEL: Single Event Latchup
SEU: Single Event Upset
TMR: Triple Mode Redundancy
SEM: Xilinx Soft Error Management IP Core

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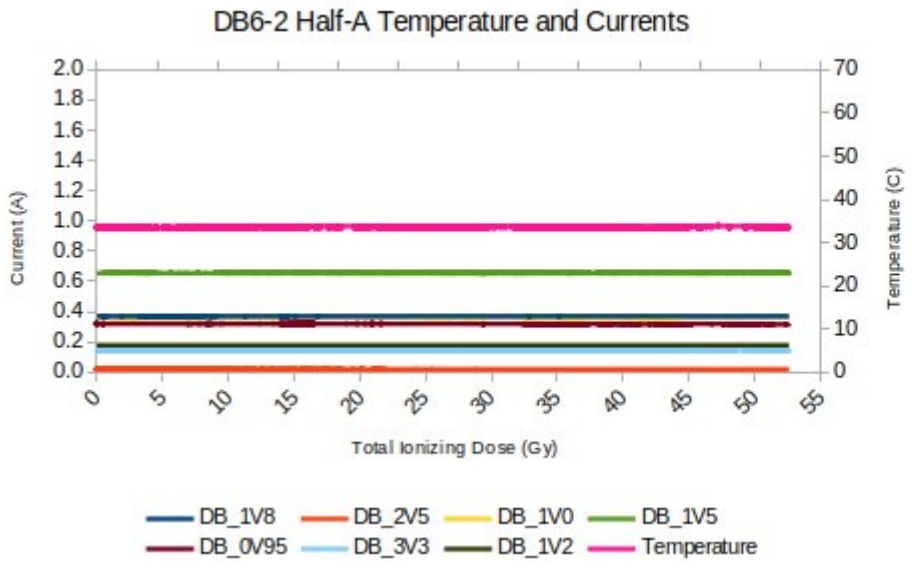
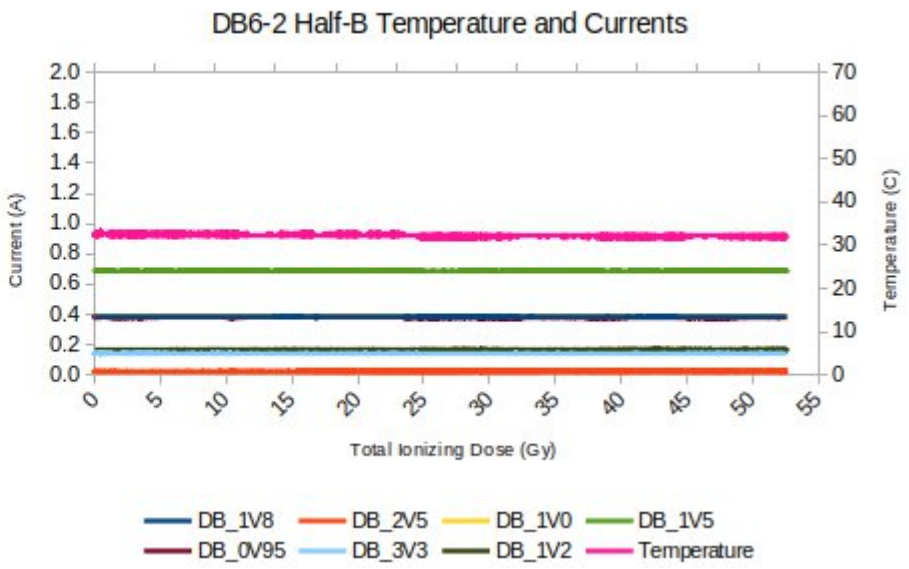
  - ProASIC preliminary tests during SEL tests were sucessful -> ~72 krad delivered by 266 MeV proton beam
  - Dedicated TID test at CERN CC60 facility:
    - **DB6-2 slow irradiation @0.03 Gy/hour to 43 Gy → ~6 days**
      - None of the DB components seem to have been damaged by the deposited TID
      - The temperature and currents were stable during the whole deposited dose (no fan failure)





- **NIEL -> 9x10^{12} n cm^{-2} (includes safety factors)**
  - Baseline Coretek SFP+ transceivers were qualified
  - Further tests planned for the end of 2021 to cover the components not qualified (ProASIC and KU FPGA)

KU: Kintex Ultrascale
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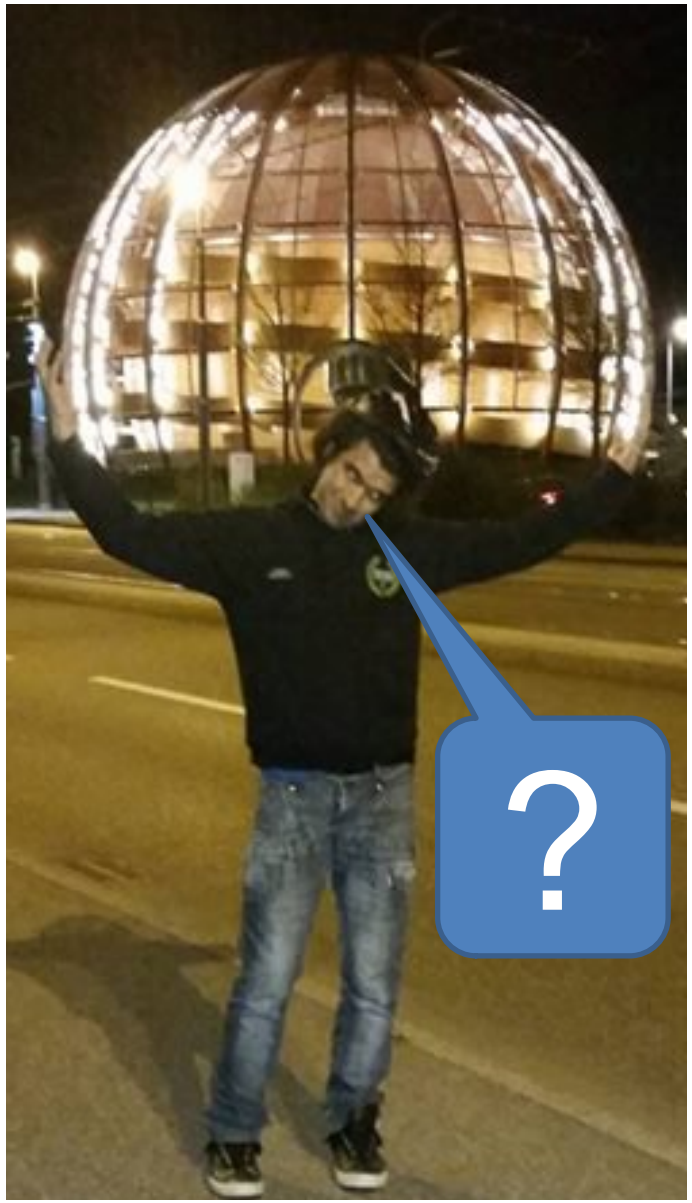
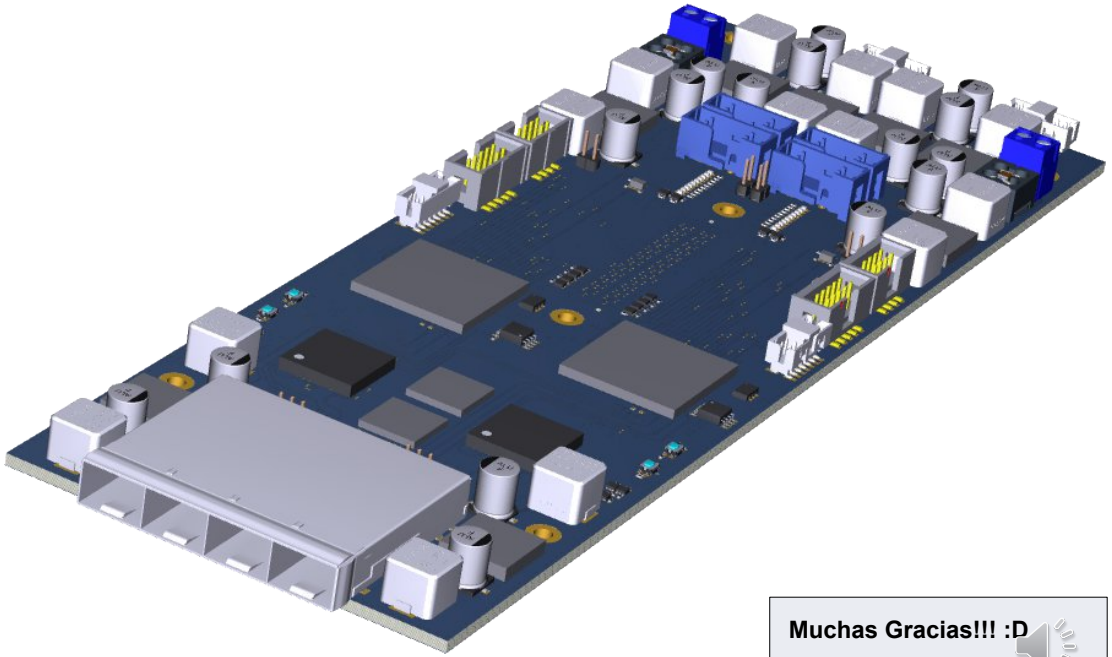


- The DB6 design is finished and has been reviewed by the TileCal Upgrade collaboration
- 10 Prototypes were produced for firmware development, TID tests and NIEL radiation tests
- DB6 fulfills the radiation requirements for TID and SEE imposed by the HL-LHC.
- The Radiation Tests Campaign is planned to continue with NIEL taking place by the end of 2021, and with the SEU tests by the of 2022
- Preliminary firmwares have been successfully implemented for both the ProASIC and the KU FPGAs and tested over a testbeam campaign at CERN SPS.
- ~930 DB6s will be produced as part of Stockholm University contribution to the upgrade of TileCal for the HL-LHC era



Muchas Gracias!!! :D

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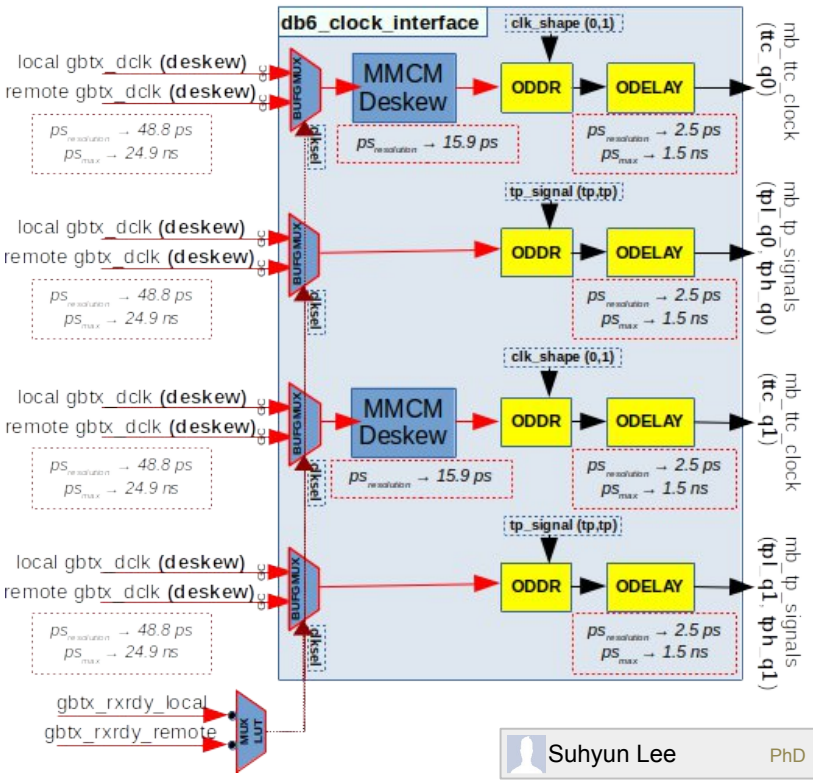
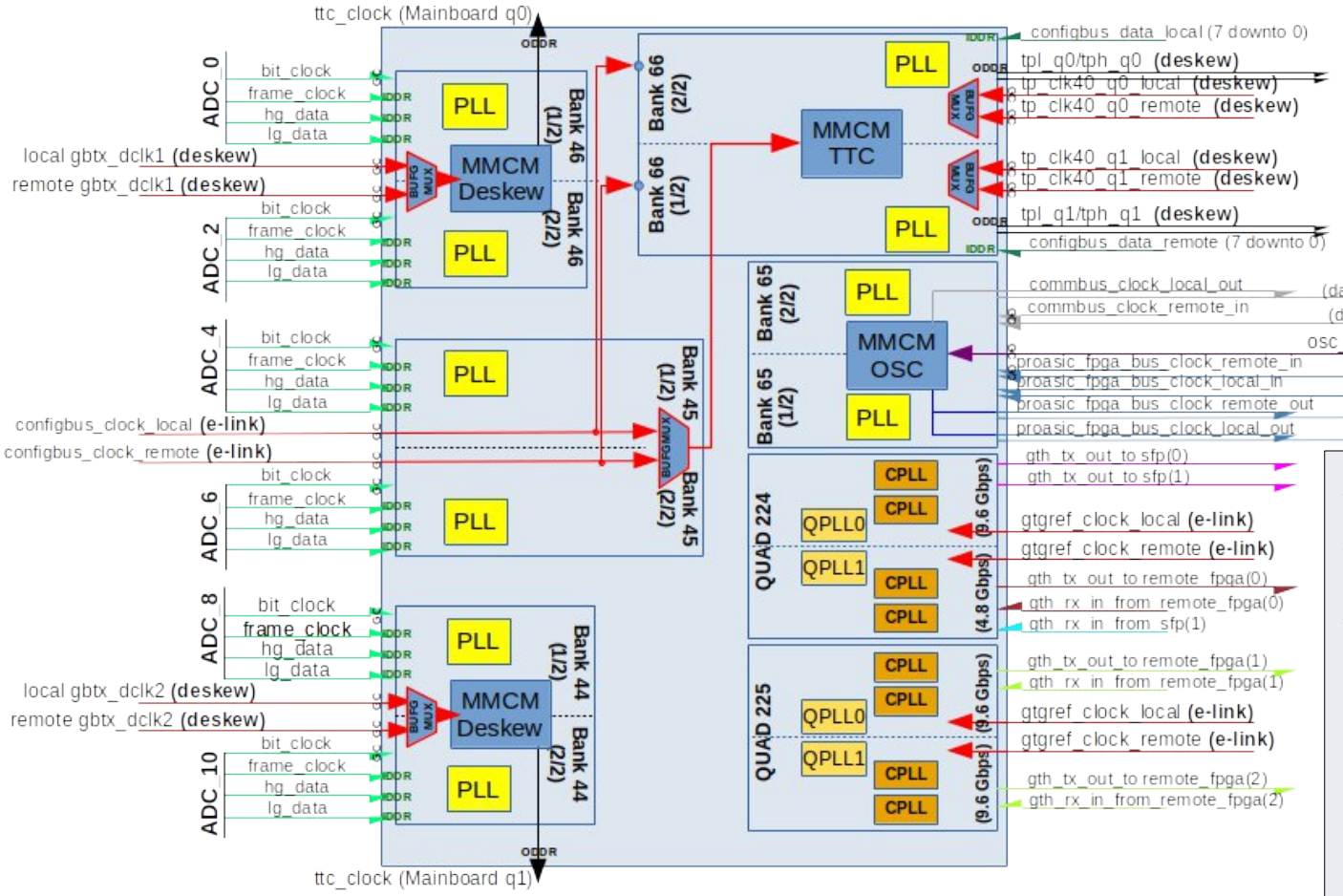
Xilinx Kintex KU035 FPGA (Up to 16 GTH MGTs, 10 CMTs, Plenty logic blocks, Plenty HR and HP IOs):
- **Banks 44, 45 and 46** -> 6x dual-gain ADC read-out 560Mbps data, 280 MHz bit_clocks, 40 MHz frame_clocks (ISERDES)
- **Bank 45** -> MUX 40 MHz ConfigBUS clocks and **Bank 66** -> receive 8x 80 Mbps configbus data (ISERDES)
- **Bank 65** -> receives 100 MHz OSC clock, and interfaces ProASIC and CommBUS, and a loopback interface for development and testing
- **QUAD 224** ->transmits data to off-detector 2x120-bit GBT words @40MHz = 9.6 Gbps, and interfaces with opposite FPGA via GTHBUS
- **QUAD 225** ->interfaces with opposite FPGA via GTHBUS, and a loopback interface for development and testing
- **Bank 44 and 46** -> receive and deliver 40 MHz de-skew clocks that drive the two groups of three ADCs sitting in each of the MB quadrants
- **Bank 66** -> receives 40 MHz de-skew clocks for the trigger pulses of Charge Injection Calibration System (CIS) in both MB quadrants

- The ADC deskew includes three possible stages: GBTx+MMCM+ODELAY
- The CIS deskew includes two possible stages: GBTx+ODELAY





CMT: Clock Management Tile
GTH: Xilinx Gigabit Transceiver H series
ISERDES/OSERDES: Xilinx FPGA Serializer-Deserializer technology
PLL: Phase locked Loop
MMCM: Mixed Mode Clock Management
CPLL - QPLL: ChannelPLL - Quad PLL
MUX: Multiplexes
IDELAY- ODELAY: Input - output TAP delay controller on the IOs of the KU

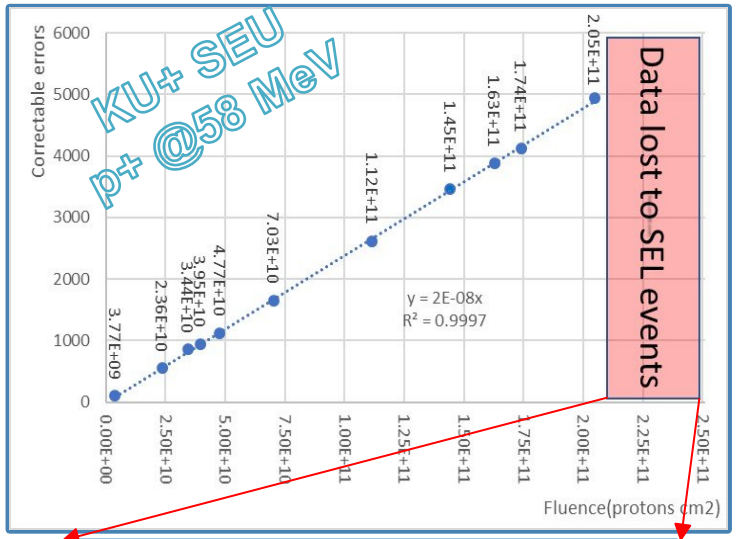
R&D studies for the ATLAS Tile Calorimeter Daughterboard.

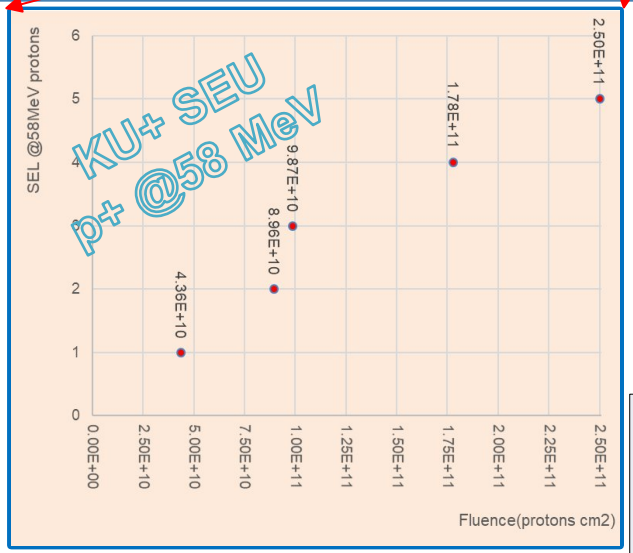
Why Xilinx Kintex Ultrascale KU035 FPGA?

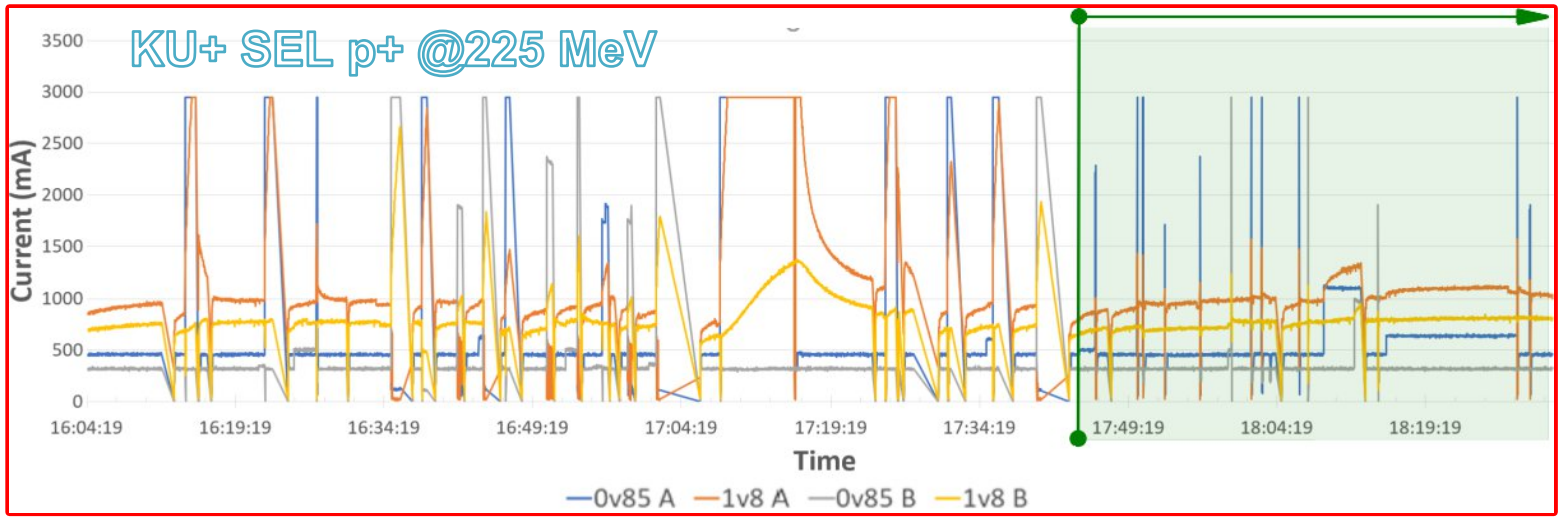
- **Daughterboard revision 4 (DB4)** uses **Kintex 7** (K7) architecture, powered by **GTX** MGTs that:
  - Have a bandwidth gap between 8.0Gbps and 9.8Gbps (DS182)
  - Cant deliver 9.6 Gbps with any of the reference clocks provided by the GBTx (40 MHz, 80 MHz, 160 MHz, 320 MHz)

- **Daughterboard revision 5 (DB5)** uses **Kintex Ultrascale+** architecture (KU+), powered by **GTY** MGTs, capable of driving 9.6Gbps with 80 MHz and 160 MHz GBTx reference clocks, but:
  - KU+ is based on the 16 nm FinFET process that showed to be suceptible to Single Event Latchups (SELs) during the Single Event Upset (SEU) tests with 58MeV protons, resulting in $2x10^{-11}$ SEL-fluence rate
  - $2.36x10^{-10}$ SEL-fluence rate was observed during KU+ 226 MeV protons SEL tests
  - SEL occurrence is unacceptable for ATLAS on-detector electronics

- **Daughterboard revision 6 (DB6)** uses **Kintex Ultrascale** architecture, powered by **GTH** MGTs, compatible with driving 9.6Gbps with 80 MHz and 160 MHz GBTx reference clocks, and based on 20nm plannar TMSC process, where no SEL were observed during 226 MeV proton SEL tests ran up to $9x10^{12}$ n cm^{-2} (includes 8x HL-LHC expected fluence accounting for safety factors)







Timeline ($^{12}/_{10}$)

- Introduction
- TileCal Upgrade
- DB6 features
- DB6 concept
- Timing and firmware
- Radiation tolerance
- Conclusions

KU: Kintex Ultrascale
KU+: Kintex Ultrascale+
K7: Kintex 7
DBX: Daughterboard revision X
GTX/GTH/GTY: Xilinx Gigabit Transceiver X/H/Y series
MGT: Multi-gigabit Transceiver
SEL: Single Event Latchup
SEU: Single Event Upset

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