PAUL SCHERRER INSTITUT

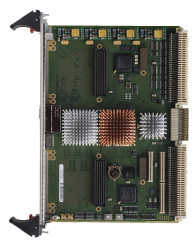
PSI

Babak Kalantari :: Electronics section :: AEK :: Paul Scherrer Institut

CompactPCI-Serial Hardware Toolbox
for SLS 2.0

Changing to a new bus-standard

- Hardware technology at PSI is heavily based on VME (SLS, SwissFEL, HIPA/Proscan)
- VME performance does not keep up with today's demand (e.g. speed, architecture)
- New projects are coming up: **SLS 2.0**
  - SLS systems were built 20 years ago
  - Many SLS hardware (VME crate, CPU's, I/O cards) already facing operatonal/availabiltiy issues
  - In 2025 that **SLS 2.0** starts, our latest processing platform will be 14 years old

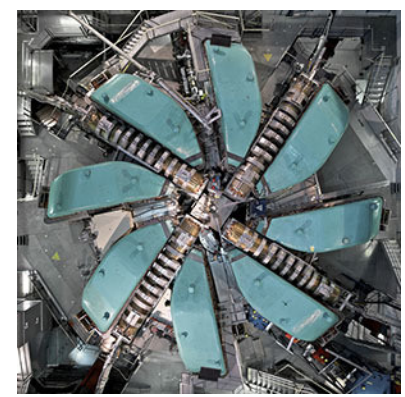


VMEbus Technology™

SwissFEL

SLS

HIPA



Changing to a new bus-standard

- Core team of embedded system experts: hardware/firmware/software deciplines
- Considered 4 bus standards: VME, uTCA, CompactPCI-Serial, VPX
- Evaluated aspects:
  - Feature & Technology
  - Usage & Status Today
  - Future Usage & Prespectives
  - Manpower Efficiency
  - Hardware Cost Efficiency

Rating: 0%=bad, 50%=not great, 100%= acceptable, 150%=good, 200%=excellent

	VME64x	uTCA.0/AMC	uTCA.4	cPCI-Serial	VPX		Weight
Features & Technology	**124%**	**93%**	**154%**	**149%**	**102%**		**4**
Crate Backplane	78%	150%	175%	156%	125%		3
Rear Transition Modules (RTMs)	88%	0%	175%	156%	0%		2
Size	173%	100%	162%	115%	135%		2
System Management & Interoperability	180%	95%	95%	165%	135%		2
Usage & Status Today	**81%**	**79%**	**64%**	**63%**	**102%**		**1**
COTS Availability Today	83%	87%	99%	51%	118%		3
Annual Sales Volume / Market Size Today	86%	100%	50%	100%	164%		2
Usage at Existing Facilities	75%	56%	38%	50%	44%		3
Future Usage & Perspectives	**10%**	**60%**	**41%**	**99%**	**119%**		**6**
COTS Availability 2035+	8%	40%	35%	113%	135%		3
Annual Sales Volume / Market Size 2035+	25%	100%	50%	100%	150%		2
Usage for New Projects 2025+	0%	50%	41%	78%	63%		2
Man Power Efficiency	**157%**	**54%**	**50%**	**107%**	**54%**		**4**
Hardware Cost Efficiency	**125%**	**75%**	**125%**	**150%**	**75%**		**3**
Overall Rating	**91%**	**70%**	**83%**	**118%**	**92%**		

Weight factor specifies importance of each aspect from the evaluator's view.

Ratings reflect personal views of the evaluation team members based on their experience and Know-how of the standards.

Decision for CompactPCI-Serial

- Technology trend: shifting from parallel bus architectures to switched serial interconnects (e.g. PCIe, Ethernet)
- VMEbus: obsolete, data transfer bottleneck, powered housing only
- uTCA risks: lack of PSI-internal Know-How, IPMI complexity, small market
- VPX: lack of know-how, expensive

- **CompactPCI-Serial**
  - \+ Promissing future perspective
  - \+ based on proven, wide-spread serial technologies (PCIe, Ethernet)
  - \+ PSI-internal Know-How available (compared to uTCA)
  - \+ high potential for synergies between PSI divisions
  - \+ Moderate availability of modern hardware with reasonable price
  - +/- Small form-factor

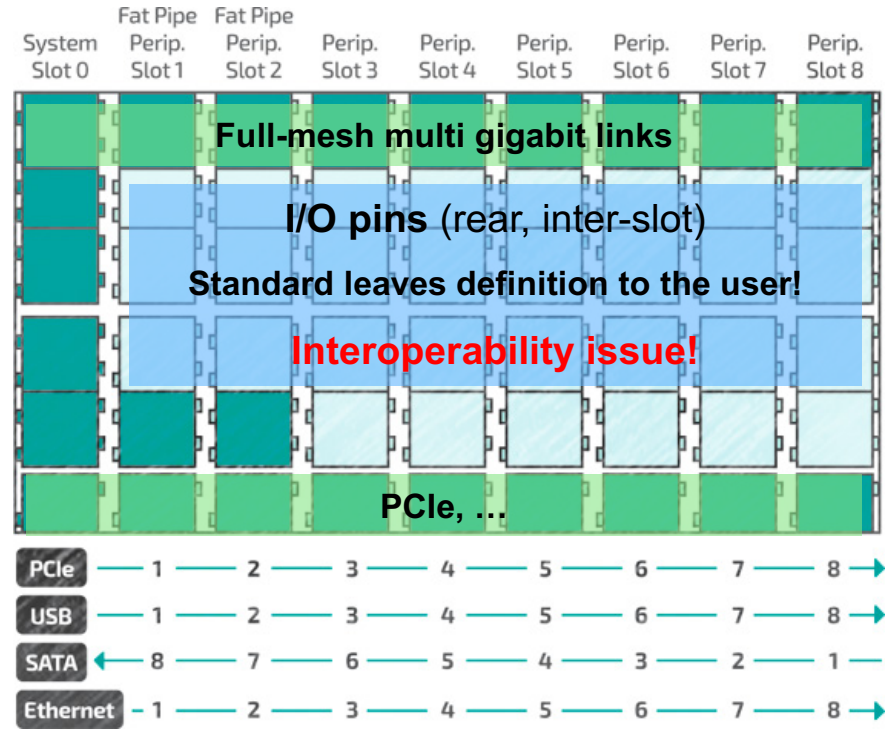
OpenCPSI-S recommendation

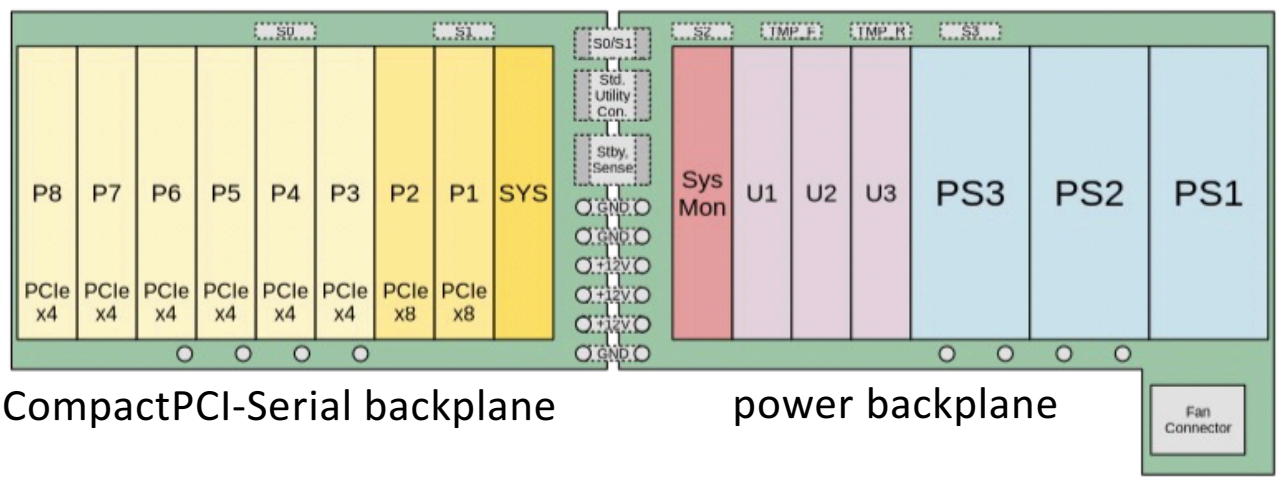
Open Common Parallel Serial Interconnect – Solution (OpenCPSI-S) is a recommendation by PSI for definition of the user I/O pins as well as a concept for power backplane.

It defines signaling and/or function of each user I/O pin to address interoperability issue. This allows PSI engineers to independently develop interoperatable boards, therefore eases collboration among PSI divisions. Currently two FPGA cards are in parallel under development in two divisions.

- Universal FPGA Board Pinout
- Minimal common pin definition for RTM‘s
- Scalable power supply (up to 3 PSU)
- Optional system monitor and utility slots

CompactPCI-Serial backplane





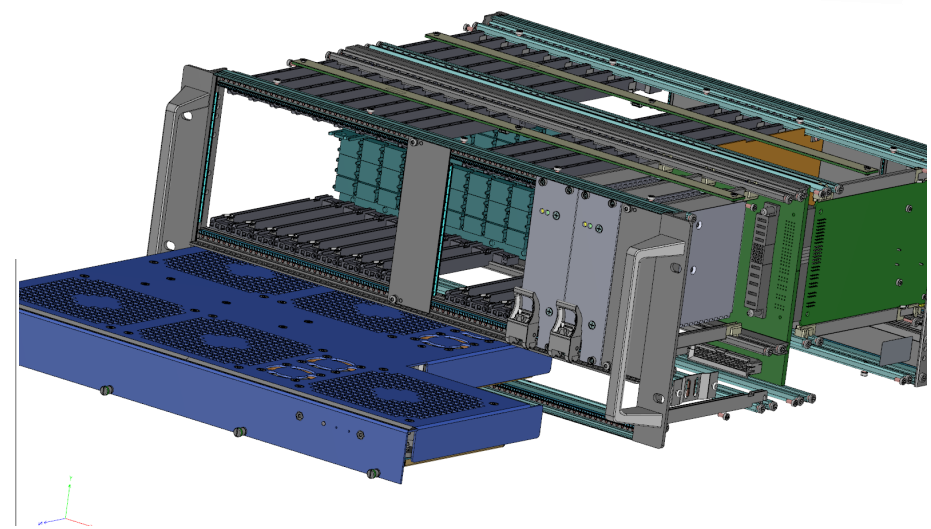
CompactPCI-Serial backplane power backplane

OpenCPSI-S Crate

- Development in collaboration with external partner
- Number of improvements are applied to COTS crates
- Status: prototypes are being tested at PSI

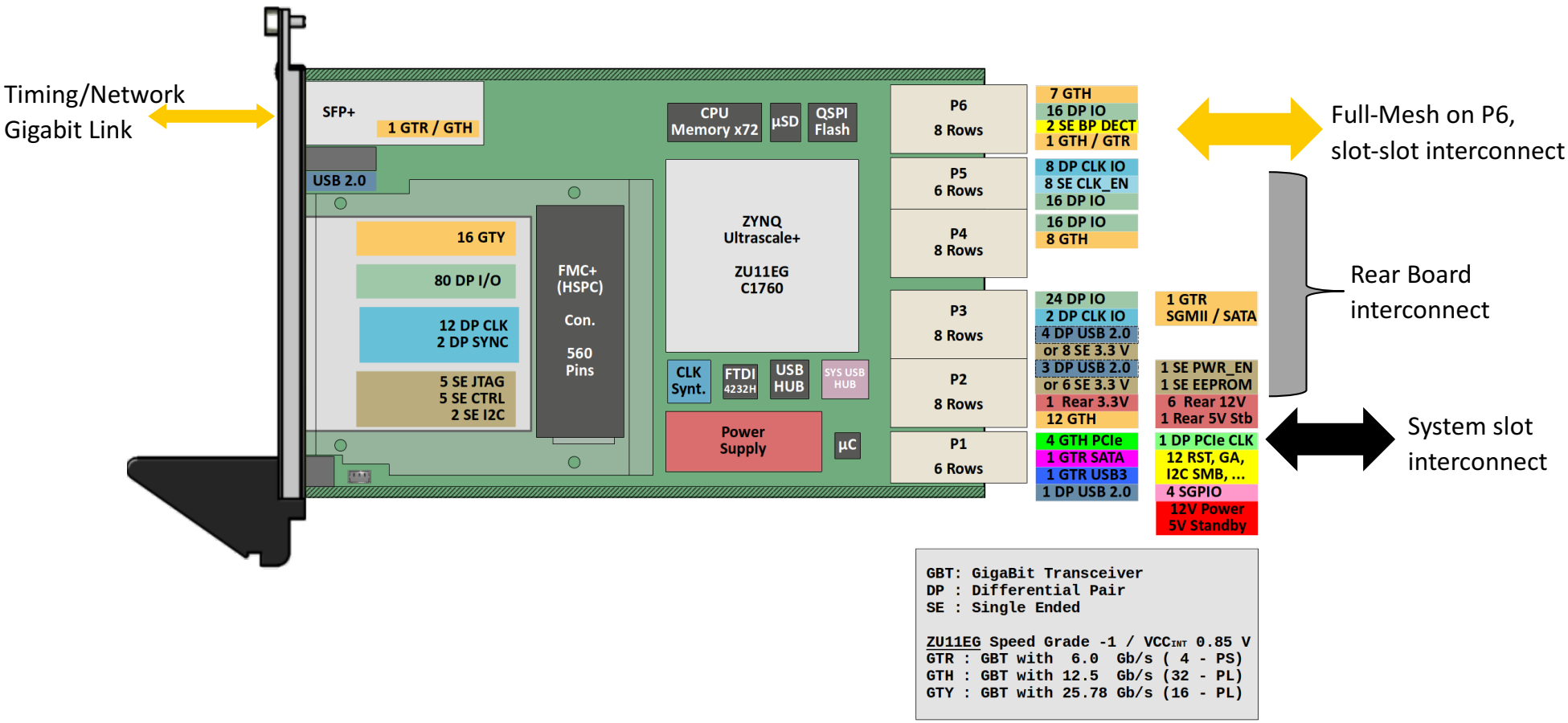
Crate prototype

- Extended rear depth to 160 mm
- Scalable power supply: up to 3x PSU (1000 W)
- Optimized cooling
- Easier maintenance
- Front + Rear temperature sensor array
- Noise reduction
- Standard CompactPCI-Serial backplane
- Separate power backplane
- System monitor & utility slots



OpenCPCI-S FMC+ Carrier (CPSI_UFC)

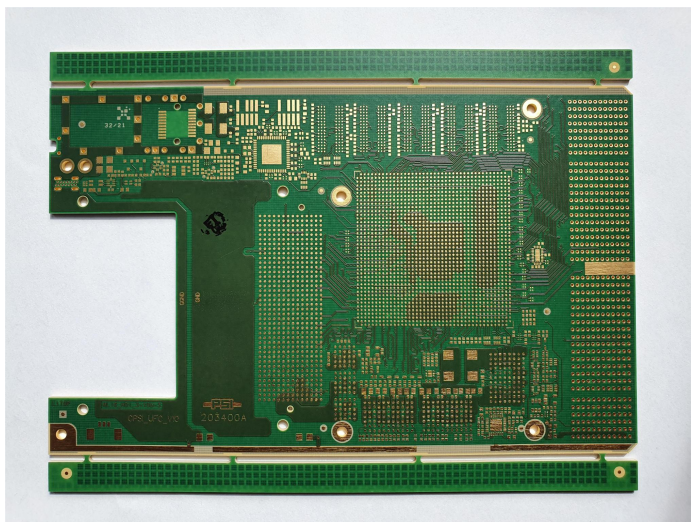
- Mixed collaboration internal-external development in GFA division
- High-end carrier with a high performance, large Zynq US+ MPSoC (ZU11EG)
- Application: LLRF, high-end DAQ & control (fill pattern feedback, scope recorder)

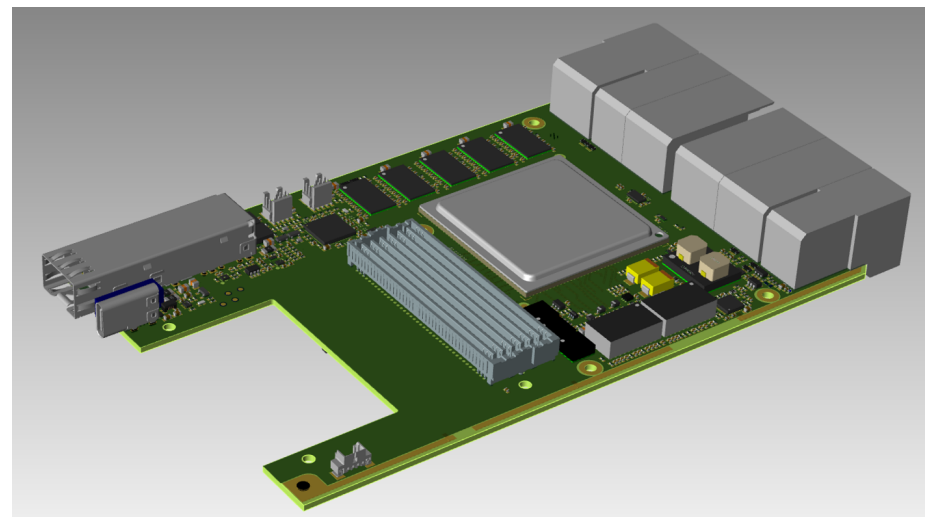


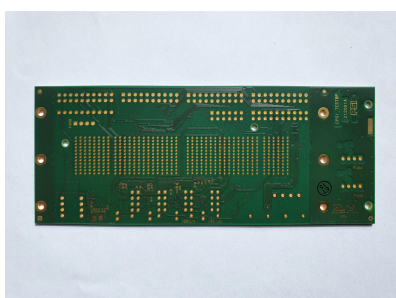
OpenCPCI-S FMC+ Carrier, Status (CPSI_UFC)

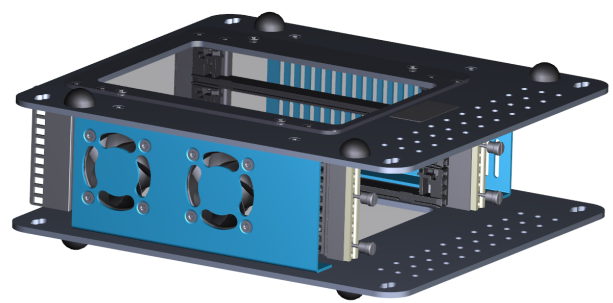
- Prototypes currently in production by external partner + board bring-up
- Hardware/Software framework for functional test is in preparation
- Functional testing planned for Nov.-Dec. 2021

Prototype PCB







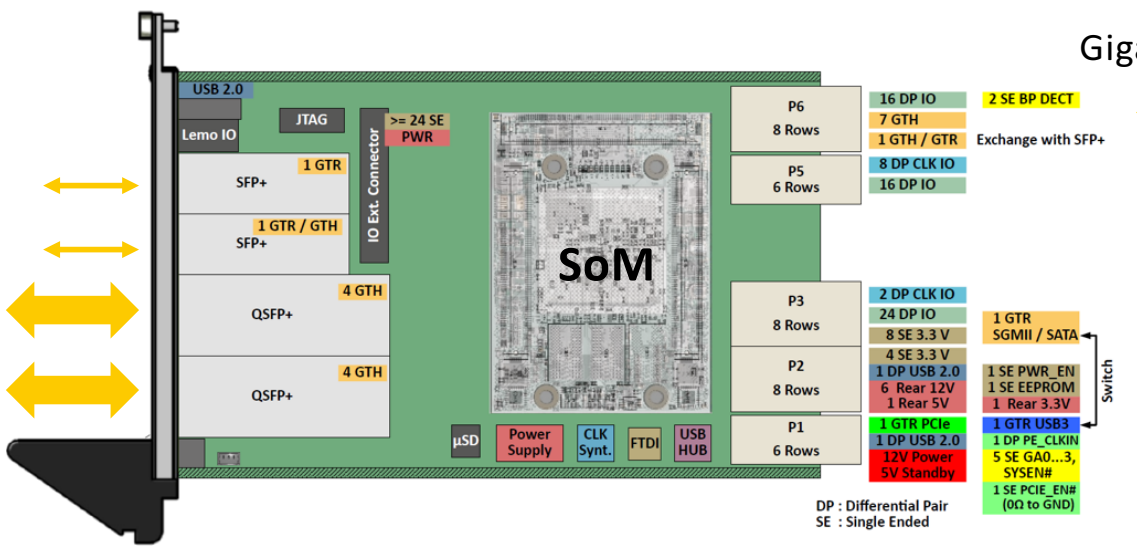


Test-Box for CPSI_UFC carrier and its backplane PCB

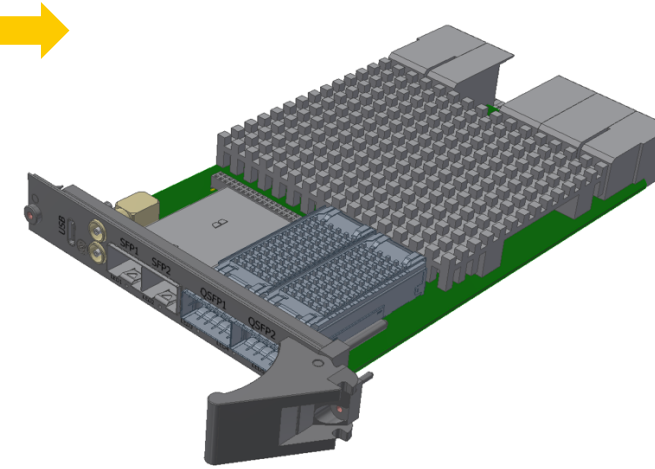
OpenCPCI-S COM-IO Board (CPSI_CIO)

- Under development at PSI in NUM division
- Uses commercial Enclustra SoM with Zynq US+ arch (XU1-6CG)
- Apps: SLS2.0 Event timing, data stream processing; DAQ for SINQ instruments
- Timing, EVR: PSI Embedded VHDL component, EVM: MRF EVM port
- Prototypes expected Q4/2021

Multi gigabit data streams

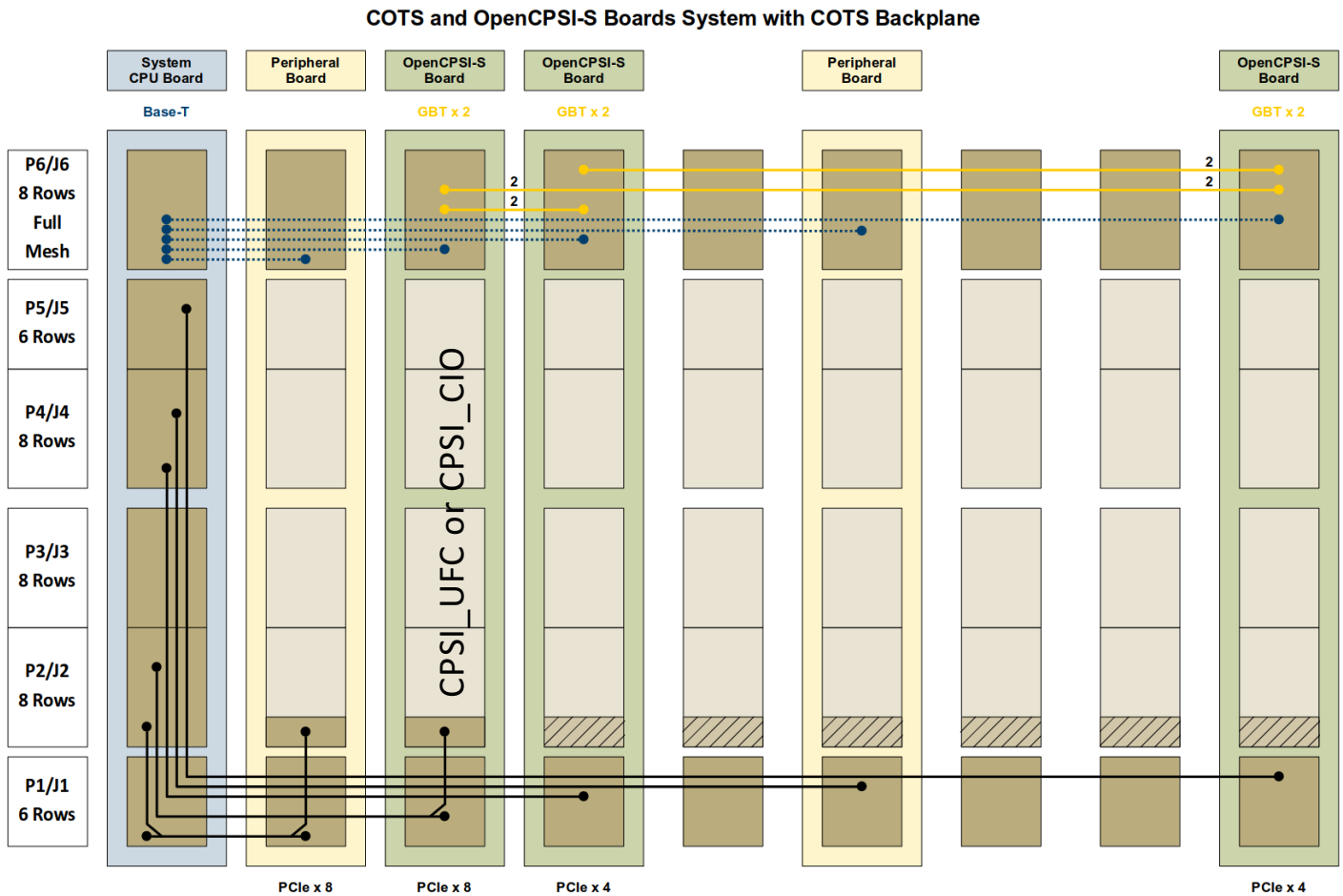


Gigabit links on backplane



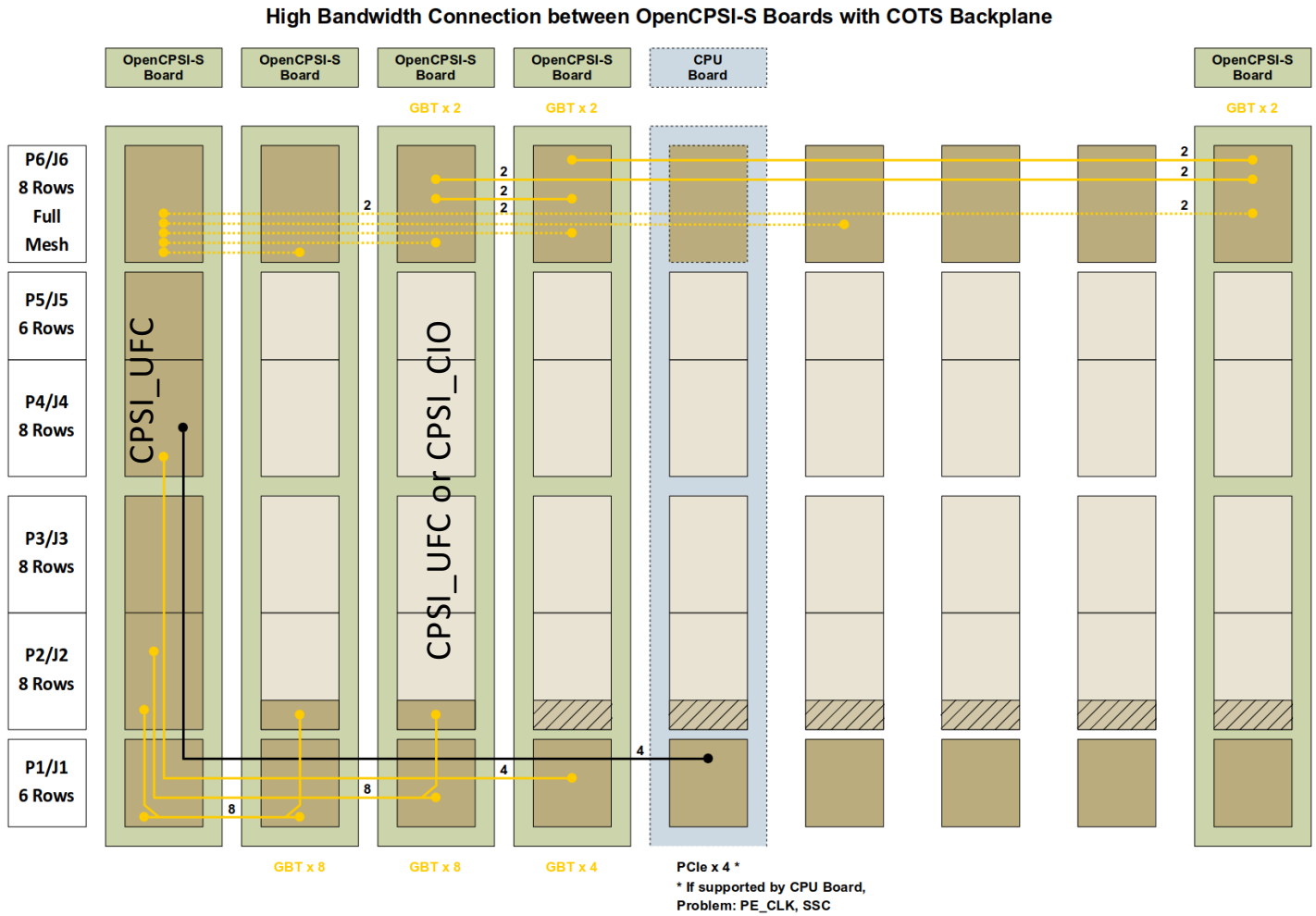
Topologies with Standard CPCI-S Backplanes

CPU-Centric System with FPGA Boards in peripheral slots



Topologies with Standard CPCI-S Backplanes

FPGA-Centric System with FPGA Board also in system slot

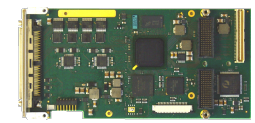


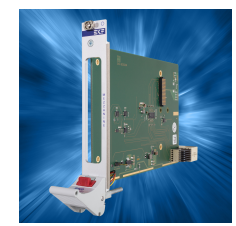
CPCI-S Toolbox Portfolio Summary

- COTS CompactPCI-Serial tools
  - System CPU: EKF SC5 FESSTIVAL, Xeon(R) 3.00GHz, Quad core, 16 GB RAM
  - XMC I/O module on XMC carriers
  - FMC/FMC+ modules (ADC, DAC, etc.)
  - COTS Crates
- OpenCPSI-S tools
  - FMC+ carrier (CPSI_UFC)
  - COM-I/O board (CPSI_CIO)
  - Various signal interfacing boards (RTM's)
  - OpenCPSI-S Crate

System CPU

XMC I/O

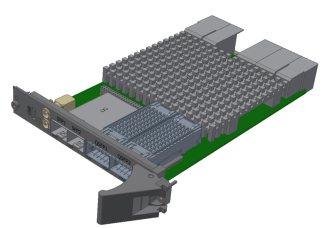




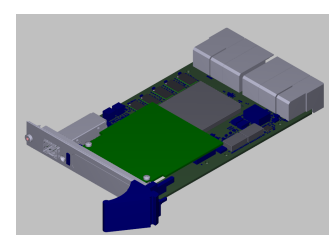
FMC+ I/O

CPSI-S crate

CPSI_CIO



CPSI_UFC



Thanks to all colleagues in GERTS standardization core team from GFA and NUM divisions as well as electronics and controls sections.