Generic data acquisition control system stack for MTCA ADC hardware

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Cosylab

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World Leader in Control Systems for Science and Proton Therapy

10 locations worldwide: USA, China, Korea, Japan, Ukraine, Slovenia, Switzerland, Sweden, France, Russia (Siberia)

200+ people
150+ highlly skilled developers and engineers
22 PhD holders from STEM fields

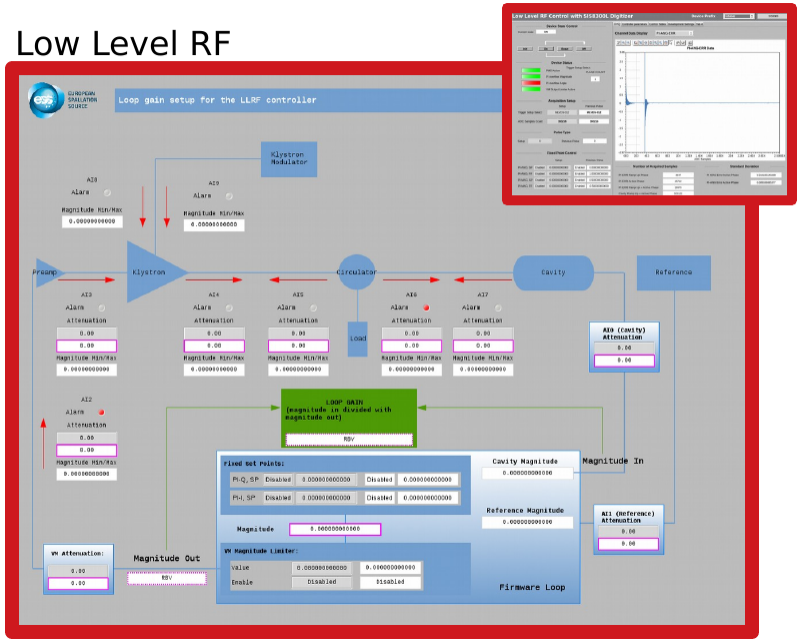
We offer **services** and **products** which require **expert knowledge**

We develop **state-of-the-art hardware** and **software**

DAQ application experience

- Different applications:
  - Beam current monitor
  - Beam loss monitor
  - Beam profile monitor
  - LLRF
- Different DAQ vendors

Low Level RF



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The question

Can we make the DAQ control system stack generic?

Goals

Improve code reusability and reduce code needed to support a new device

Allow custom implementations and extension of functionality

Cover as many control system frameworks as possible

Reduce expertise needed to support new hardware

Support different HW vendors with similar FPGA chips and I/O specs

Micro TCA

- System developed on AMC523 from Vadatech
  - Using MRT523 and MZ523B
  - 125 MSPS, 12 CH AI, 2 CH AO

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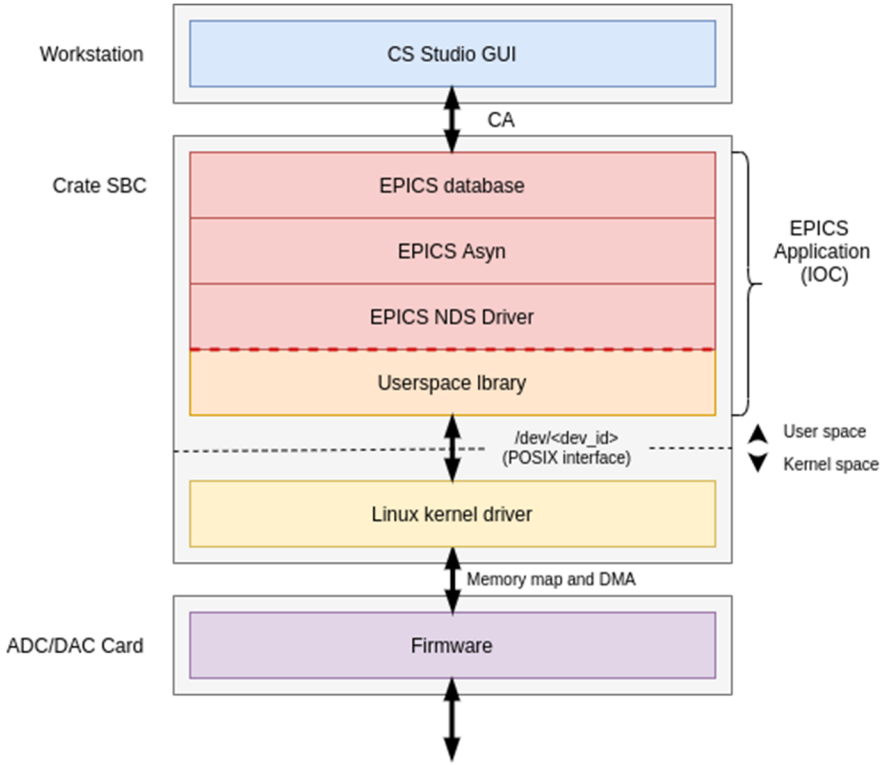
gDAQ Architecture



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Configuration

- Configured using JSON
  - Affects all components in the stack

```
{
"deviceName" : "Vadatech AMC523",
"deviceIdAddr" : "0x500",
"deviceId" : "0x5654A523",
"fwGitHashAddr" : "0x600",
"fwGitHash" : "0x831d28ef07cf3d6d136a9f14a1bf58e193c12469",

"memorySize" : "0x8000000",
"dmaAxisWidth" : 128,

"mmapSize" : "0x6101b",
"daqBase" : "0x10000",
"dgenBase" : "0x20000",
"trigBase" : "0x30000",

"clkPeriod" : 8,
"adcVoltageRef" : 2.0,

"aiChannels" : 12,
"aiSampleWidth" : 16,
"aiSampleAlign" : 8,
"aiDataRate" : 125E6,

"aoChannels" : 2,
"aoSampleWidth" : 16,
"aoSampleAlign" : 2,
"aoDataRate" : 125E6,

"nDgenStreams" : 12,
"dgenStreams" : [
"ADC_0",
"ADC_1",
"ADC_2",
```

Firmware

- Configurable data width up to 32 bit
- Configurable up to 32 data acquisition and 32 signal generation channels
- Configurable buffer allocation for each channel separately
- Enable and disable for each channel
- Multiple trigger sources including software
- Arm and automatic re-arm
- Trigger mode: Front trigger, end trigger (prebuffering)

- Multiple data generation sources: from RAM, internal data stream (NCO), digitally processed ADC data
- Data streaming options: on trigger, periodic

Kernel and user-space

- Kernel driver
  - Thin driver
  - Handles DMA and maps the FPGA register-map to user-space

- Userspace library
  - Generalized C++ API
  - Supports data input and data output use-cases
  - Allows access to device data and can be extended

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Why NDS?

- Nominal Device Support
- Supports EPICS as well as TANGO
- Databases and device servers can be programmatically instantiated and configured
  - Allows variying channel count
  - Allows variying channel size

- Code on github:
  - https://github.com/Cosylab/nds3

Generic DAQ

CHANNELS | ADDITIONAL TRIGGERS | OVERVIEW | DATA BROWSER

Channels

IN 01

Channel 01 configuration

ENABLE

ARM

TERMINATE

SOFT TRIG

Trigger mode: end trigger | end trigger

Arm mode: auto-rearm | auto-rearm

Slope: 1

Offset: 0

FPGA state: idle

Channel state: enabled

Samples per trigger: 128 | 128

Number of triggers: 1 | 1

Triggers

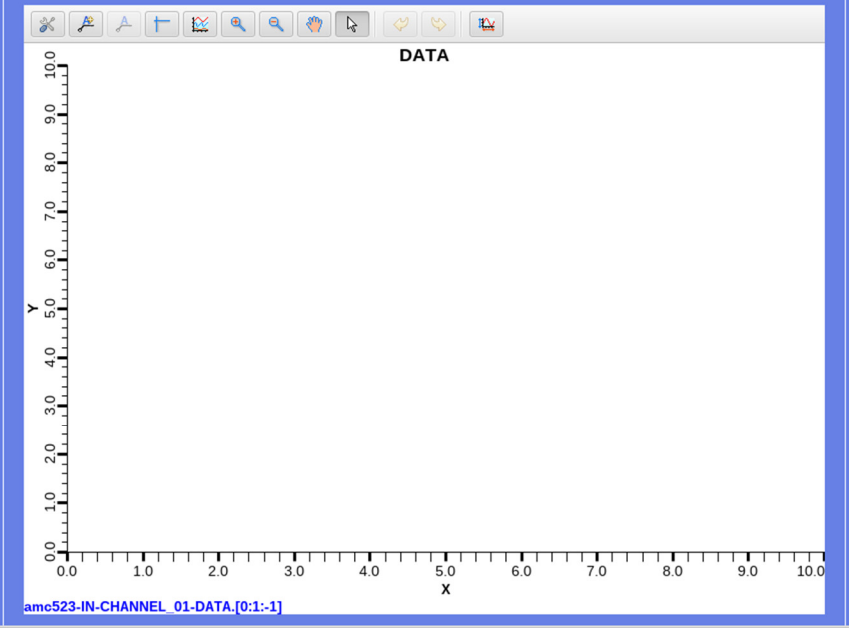
- Front panel trigger
- Back plane trigger 0
- Back plane trigger 1
- Back plane trigger 2
- RTM DensiShield 0
- RTM DensiShield 1
- RTM DensiShield 2
- RTM DensiShield 3
- Timing event 0
- Timing event 1
- FPGA counter

Global

Device state: ON — SEND OUTPUT SOFT TRIGGERS

Conversion: ON — SEND INPUT SOFT TRIGGERS

Graph



Activities org.phoebus.ui.application.PhoebusApplication nov 20 01:31

CS-Studio (Phoebus)

Display

Generic DAQ

CHANNELS | ADDITIONAL TRIGGERS | OVERVIEW | DATA BROWSER

Channels

IN 01

Channel 01 configuration

ENABLE

ARM

TERMINATE

SOFT TRIG

Trigger mode: end trigger | end trigger

Arm mode: auto-rearm | auto-rearm

Slope: 1

Offset: 0

FPGA state: running

Channel state: running

Samples per trigger: 128 | 128

Number of triggers: 1 | 1

Triggers

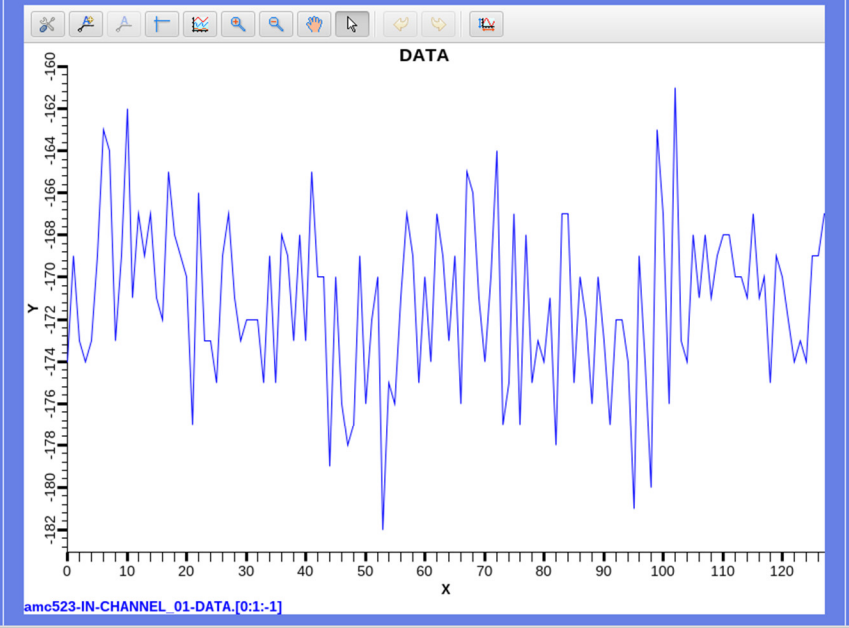
Front panel trigger	RTM DensiShield 0	Timing event 0
Back plane trigger 0	RTM DensiShield 1	Timing event 1
Back plane trigger 1	RTM DensiShield 2	FPGA counter
Back plane trigger 2	RTM DensiShield 3	

Global

Device state: ON — SEND OUTPUT SOFT TRIGGERS

Conversion: ON — SEND INPUT SOFT TRIGGERS

Graph



CS-Studio (Phoebus)

Display ×

General DAQ

CHANNELS | ADDITIONAL TRIGGERS | OVERVIEW | DATA BROWSER

Channels

OUT 00

Channel 00 configuration

ENABLE

ARM

TERMINATE

SOFT TRIG

LOAD DATA

Mode: triggered | triggered

Arm mode: auto-rearm | auto-rearm

Set source: | ADC_0

FPGA state: idle

Channel state: enabled

Idle value: 0 | 0

Buffer offset: 0 | 0

Buffer size: 128 | 128

Triggers

- Front panel trigger
- Back plane trigger 0
- Back plane trigger 1
- Back plane trigger 2
- RTM DensiShield 0
- RTM DensiShield 1
- RTM DensiShield 2
- RTM DensiShield 3
- Timing event 0
- Timing event 1
- FPGA counter

Global

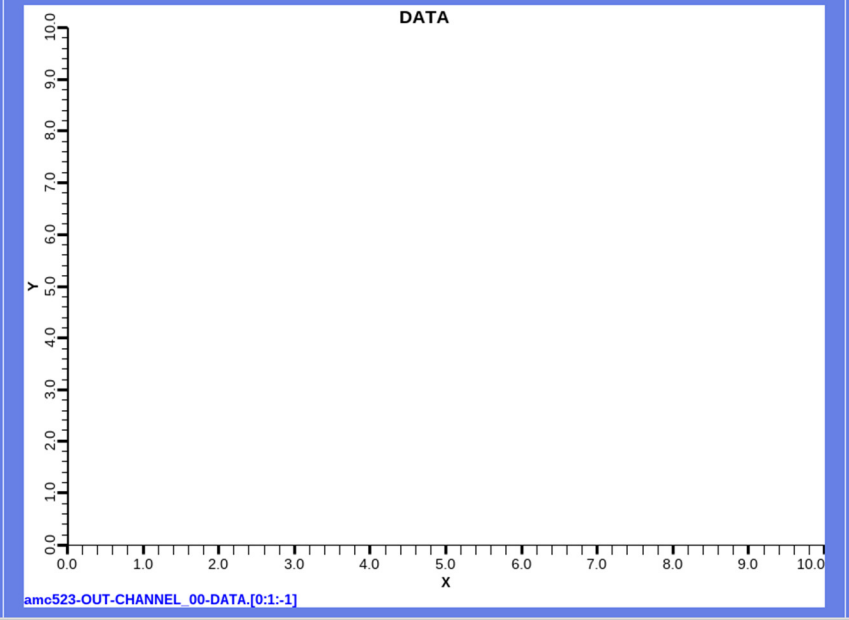
Device state: ON

Conversion: ON

SEND OUTPUT SOFT TRIGGERS

SEND INPUT SOFT TRIGGERS

Graph



Activities org.phoebus.ui.application.PhoebusApplication nov 20 01:32

CS-Studio (Phoebus)

Display ×

Generic DAQ

CHANNELS | ADDITIONAL TRIGGERS | OVERVIEW | DATA BROWSER

Channels

OUT 00

Channel 00 configuration

ENABLE

ARM

TERMINATE

SOFT TRIG

LOAD DATA

Mode: triggered | triggered

Arm mode: auto-rearm | auto-rearm

Set source: | ADC_0

FPGA state: idle

Channel state: enabled

Idle value: 0 | 0

Buffer offset: 100 | 100

Buffer size: 250 | 250

Triggers

- Front panel trigger
- Back plane trigger 0
- Back plane trigger 1
- Back plane trigger 2
- RTM DensiShield 0
- RTM DensiShield 1
- RTM DensiShield 2
- RTM DensiShield 3
- Timing event 0
- Timing event 1
- FPGA counter

Global

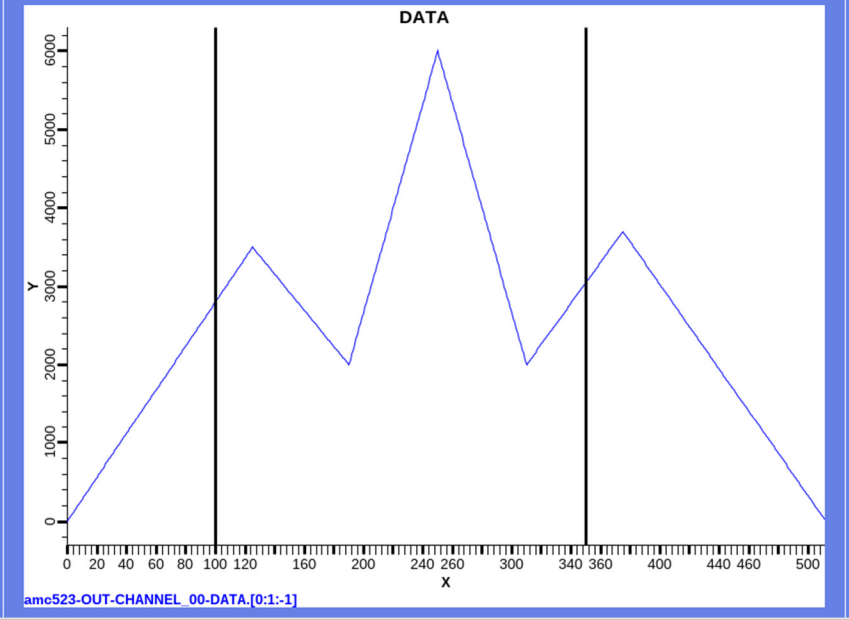
Device state: ON

Conversion: ON

SEND OUTPUT SOFT TRIGGERS

SEND INPUT SOFT TRIGGERS

Graph



Generic DAQ

CHANNELS | ADDITIONAL TRIGGERS | OVERVIEW | DATA BROWSER

Input channels

SEND INPUT SOFT TRIGGERS

Device state: ON

Ch index	Enable	Arm	Terminate	Soft trigger	Trig mode	Arm mode	Fpga state	Channel state	
00	EN	ARM	TERM	ST	front trigger	auto-rearm	idle	enabled	Configure
01	EN	ARM	TERM	ST	front trigger	single	idle	enabled	Configure
02	EN	ARM	TERM	ST	front trigger	auto-rearm	idle	enabled	Configure
03	EN	ARM	TERM	ST	end trigger	auto-rearm	idle	enabled	Configure
04	EN	ARM	TERM	ST	front trigger	single	idle	enabled	Configure
05	EN	ARM	TERM	ST	end trigger	auto-rearm	idle	enabled	Configure
06	EN	ARM	TERM	ST	front trigger	auto-rearm	idle	enabled	Configure
07	EN	ARM	TERM	ST	end trigger	auto-rearm	idle	enabled	Configure
08	EN	ARM	TERM	ST	front trigger	auto-rearm	idle	enabled	Configure
09	EN	ARM	TERM	ST	end trigger	auto-rearm	idle	enabled	Configure
10	EN	ARM	TERM	ST	front trigger	auto-rearm	idle	enabled	Configure
11	EN	ARM	TERM	ST	end trigger	auto-rearm	idle	enabled	Configure

Output channels

SEND OUTPUT SOFT TRIGGERS

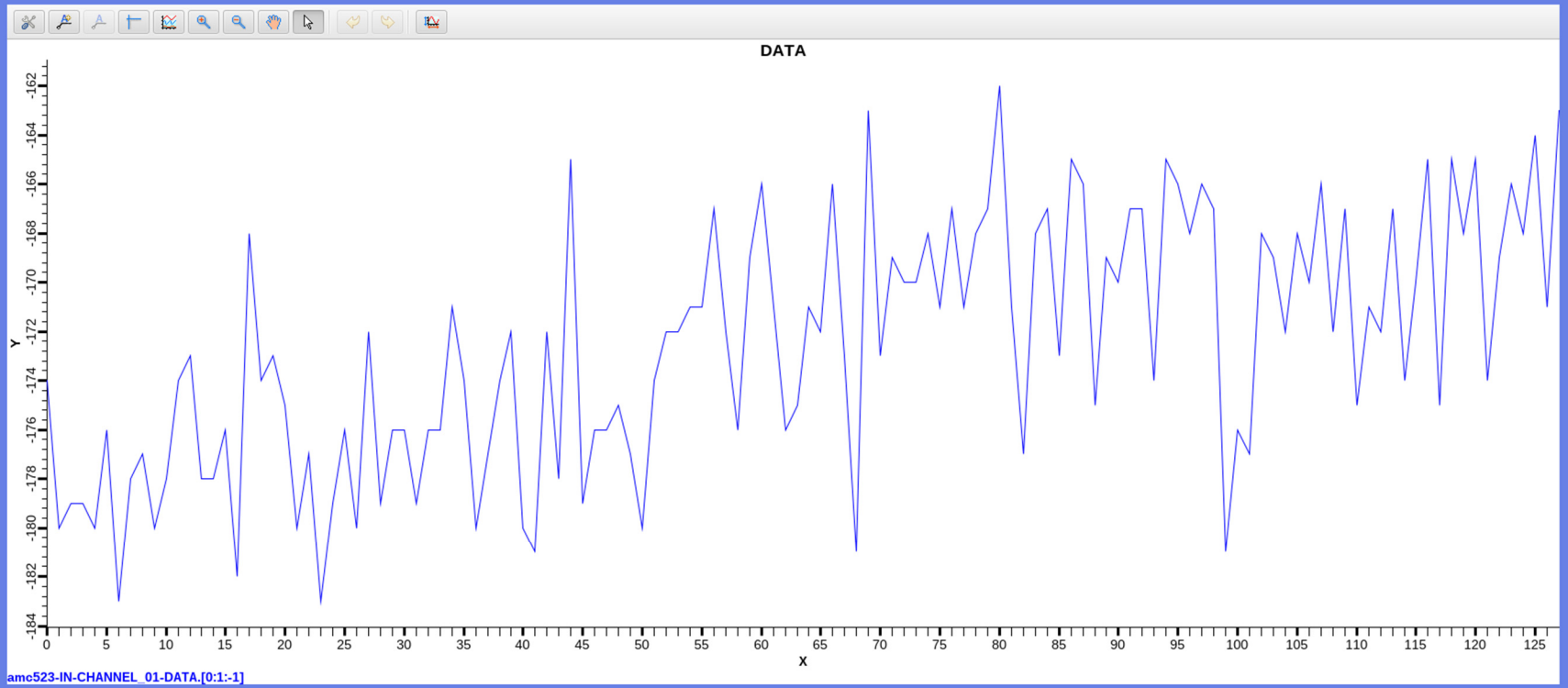
Ch index	Enable	Arm	Terminate	Soft trigger	Mode	Arm mode	Fpga state	Channel state	
00	EN	ARM	TERM	ST	triggered	auto-rearm	idle	enabled	Configure
01	EN	ARM	TERM	ST	triggered	auto-rearm	idle	enabled	Configure

Generic DAQ

CHANNELS | ADDITIONAL TRIGGERS | OVERVIEW | DATA BROWSER

Graph

Input channel 01



Conclusion

- Works as expected
- Tested but not yet used in production
- First use already on horizon

- Future
  - Adding support for MRF is possible
  - Adding support for continuous, lossless acquisition

- Contact me if you have any questions: jure.krasna@cosylab.com

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Thank you!

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