WEPV037

ICALEPCS 2021

Development of a Voltage Interlock System for Normal-Conducting Magnets in the Neutrino Experimental Facility at J-PARC

Kazuo Nakayoshi, Ken Sakashita, Yoshiaki Fujii (J-PARC/KEK, Japan) for J-PARC Neutrino facility group

1. Background/Motivation

Only one miss shot causes serious damage to the beamline equipment at J-PARC neutrino experimental facility.

To strengthen the interlock for beamline,
we are developing a voltage interlock system.

2. Preliminary study

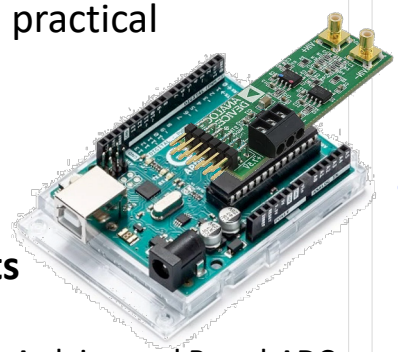
Before developing the interlock system, the following preliminary study was conducted.

- **Feasibility of magnet coil voltage measurement**
- **System and voltage divider design**
- **Validation of the use of Arduino + ADC**

3. Validation of the use of Arduino + ADC

We have verified Arduino + ADC are practical as key components of this system.

- **Sampling readout by SPI**
- **Read and compare data at 1kHz**
- **Threshold setting using interrupts**
- **Signal output for interlock**



Arduino and Pmod-ADC

4. Prototype development

We developed a prototype of voltage interlock system using Arduino and Pmod-ADC.

5. Summary and Future plans

We developed the prototype of voltage interlock system. Next step, the prototype will be attached to the power supply for testing and improvement.

Background/Motivation

We are producing high intensity neutrino beam for T2K experiment at J-PARC.

Only one miss shot (~1.27MJ) causes serious damage to the beamline equipment.

We develop a new interlock system to detect 1% voltage change of beam-transport magnets which may cause a dangerous beam orbit shift.

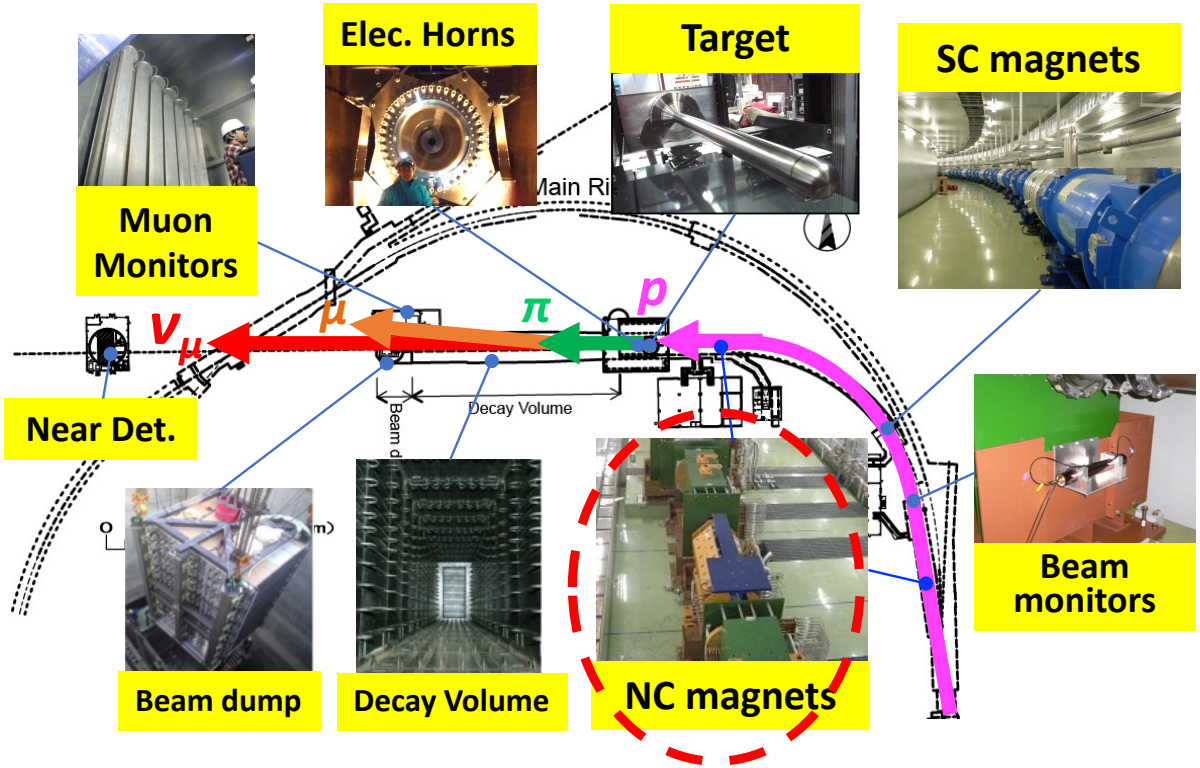


Figure 1: Neutrino experimental facility at J-PARC

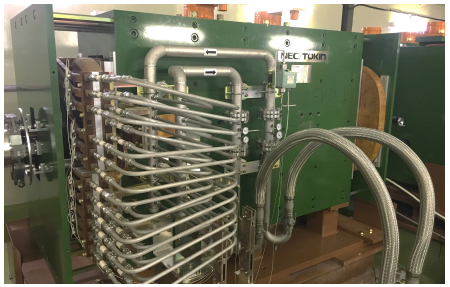


Figure 2: A dipole magnet at the primary beamline

Preliminary study

How can we measure the magnet coil voltage ?

We performed a preliminary study for measurements of the magnet coil voltage with a digital multimeter. It was found even the measurement of the voltage between the outputs of the ground PS during accelerator operation can obtain the accuracy we need.(Figure 3).

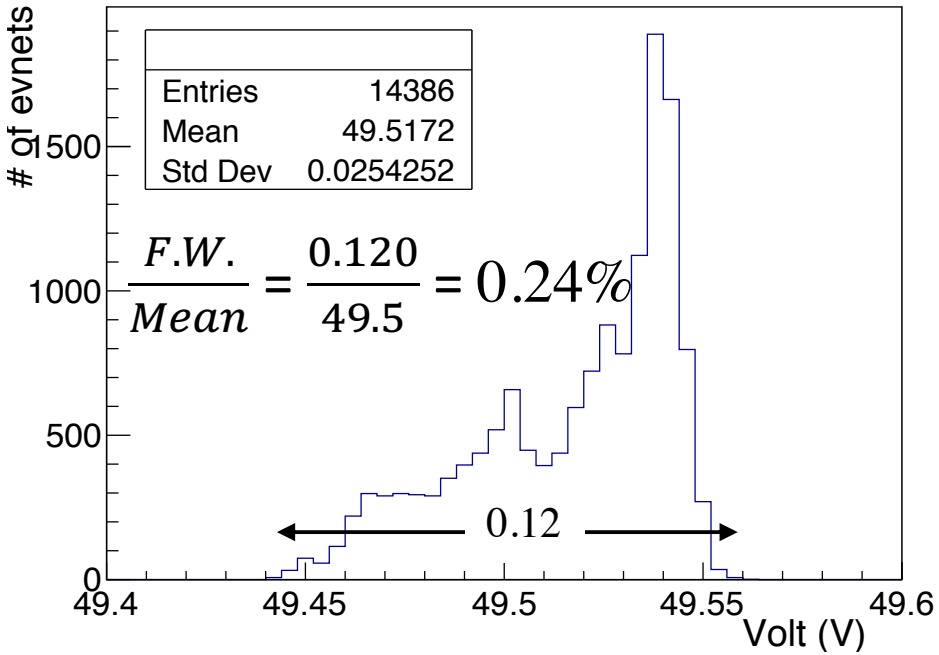


Figure 3: Results of preliminary study

What kind of system we will adopt

In order to realize a small latency and an intelligence function (future extension) , we are evaluating a sysmtem with Audiuno + ADC. Sufficient input impedance is ***10kOhm < R < 10MOhm***. We use a Pmod-ADC(AD7685) and modify its total input impedance to 200kOhm.

Figure 4: Arduino UNO

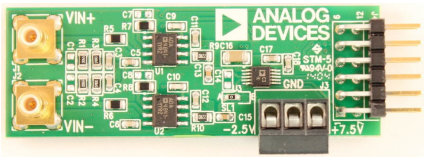


Figure 5: Pmod-ADC board (AD7685: 16bit, 250kSPS)

Validation of the use of Arduino + Pmod-ADC

We have verified the following validity of adopting Arduino + Pmod-ADC.

- **Check feasibility of ADC readout by Arduino with SPI[1]**
- **Checking the ability to compare read data with thresholds**
- **Implementation of threshold setting using interrupts**
- **Confirmation that the signal can be output as an interlock**

[1]: *Serial Peripheral Interface*

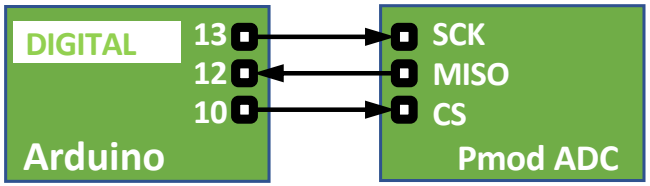


Figure 6: Arduino and Pmod ADC wiring for SPI

Voltage interlock system using Arduino and Pmod-ADC seems to be feasible.

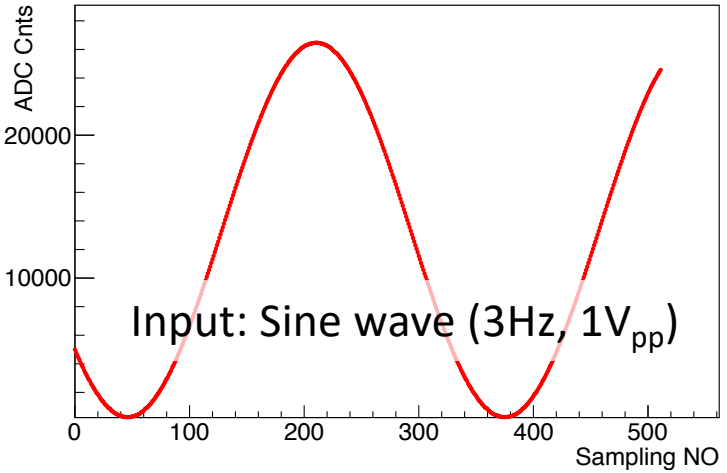


Figure 7: Sampling read results

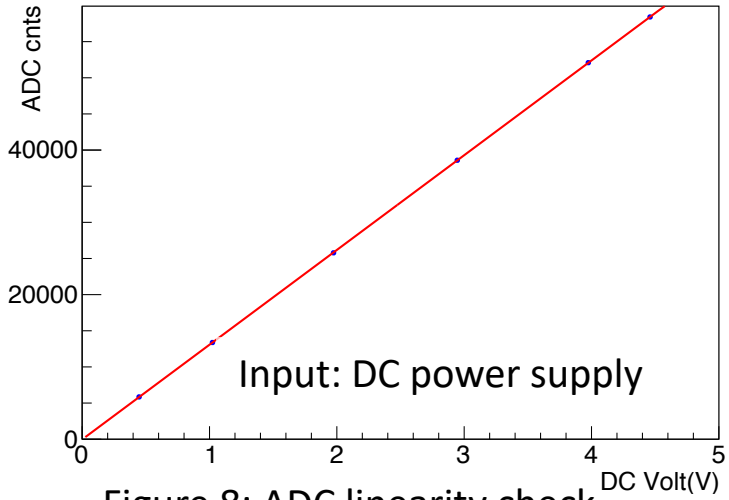


Figure 8: ADC linearity check

Prototype development

We performed long-term stability tests and interlock latency measurements using the prototype(Figure 9).

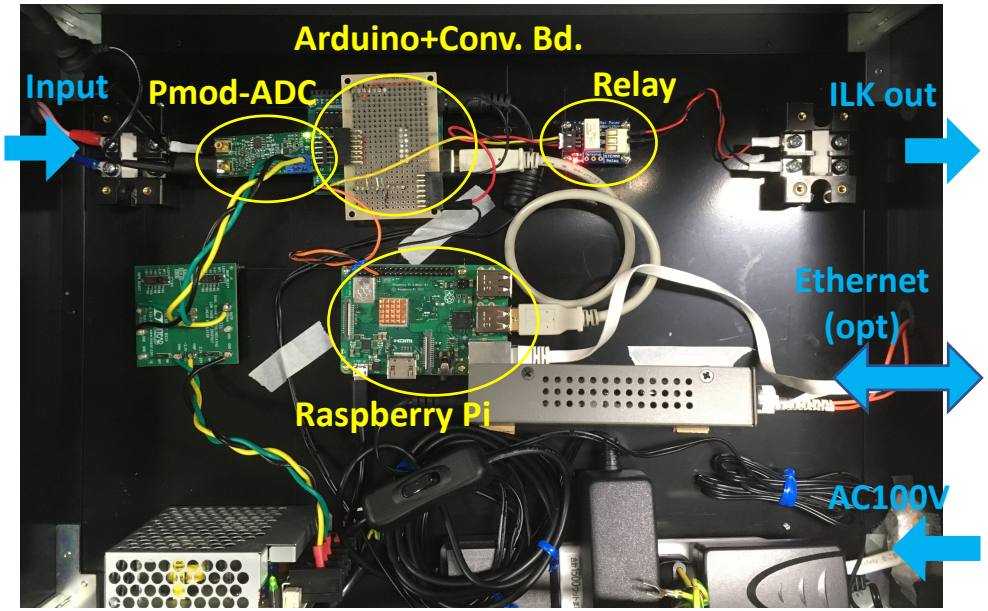


Figure 9: The prototype in a box

Summary and Future plans

We developed the prototype of voltage interlock system. Next step, the prototype will be attached to the power supply for further evaluation. We also plan to improve the performance before actual implementation.

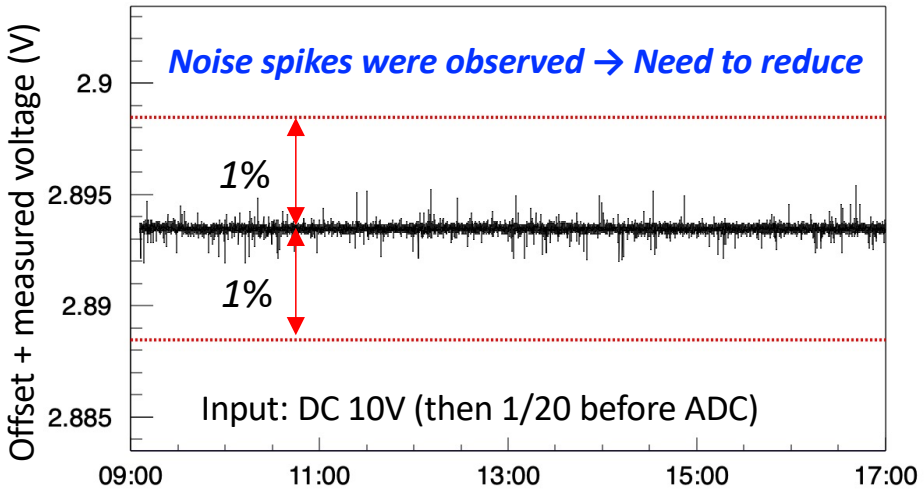


Figure 10: Result of long-term stability test

CH0: DC input
CH1: Relay input
We measured x10 using a oscilloscope.
Trigger: DC in 10->9V (by hand)

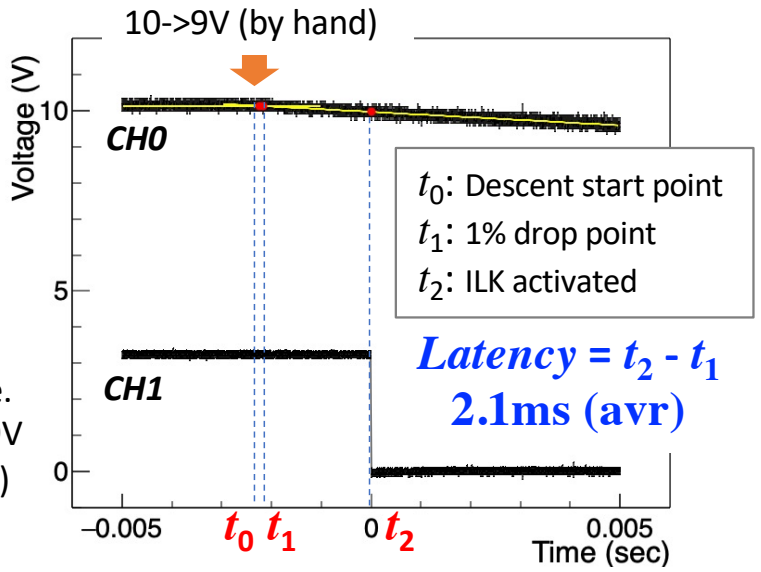


Figure 11: Interlock latency measurement