WEPV031

Status of the uTCA Digital LLRF design for SARAF Phase II

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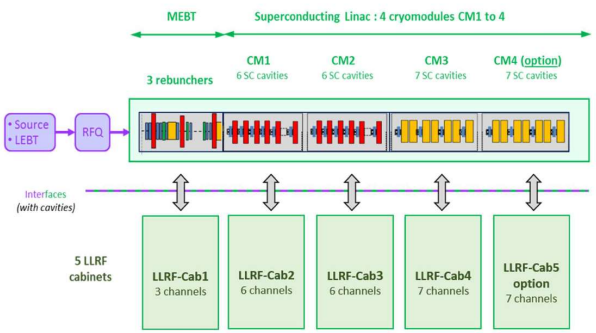
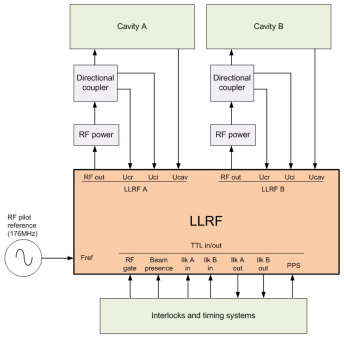
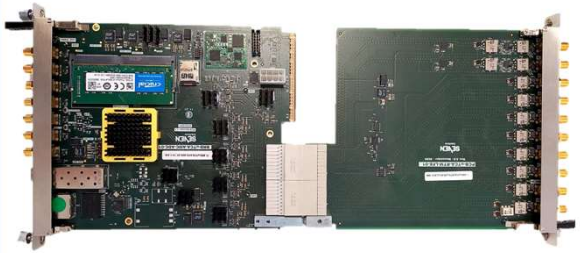
ICALEPCS 2021

LLRF for SARAF (Soreq Applied Research Accelerator Facility)

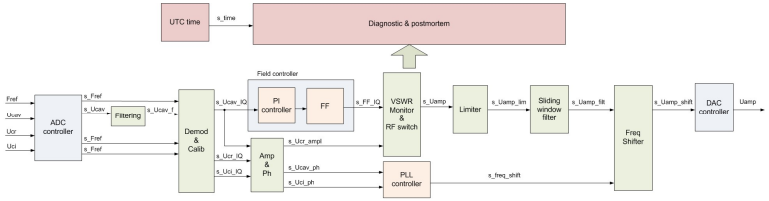




Hardware Architecture based on Analog Front End + Digitital Processing

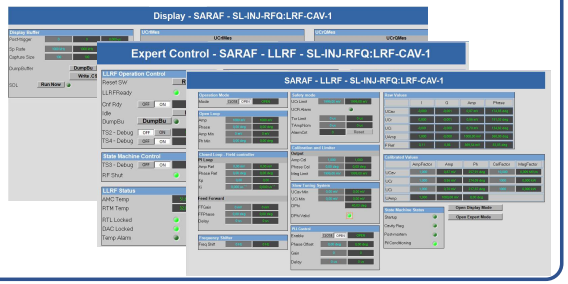


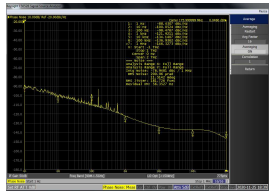
Rackeable uTCA.4 solution

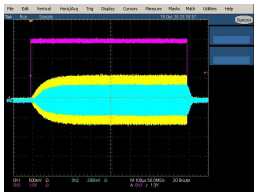


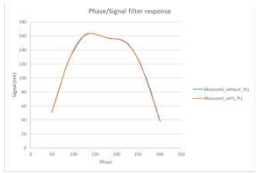
Intutitive operation and diagnostic GUI

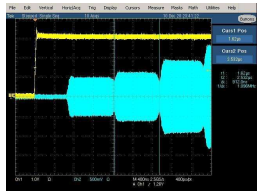
All the main functionalities to control the cavity field.

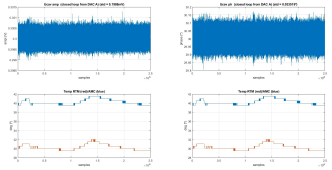












Great performance!

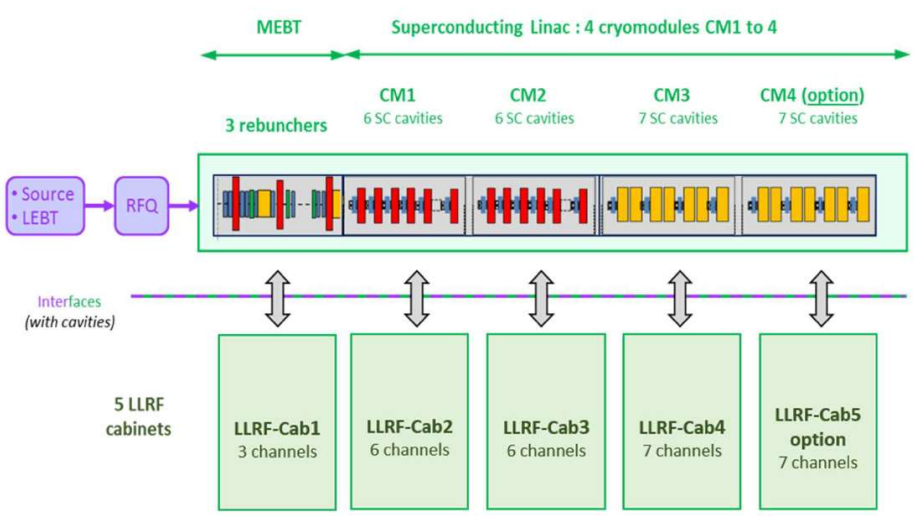
Abstract

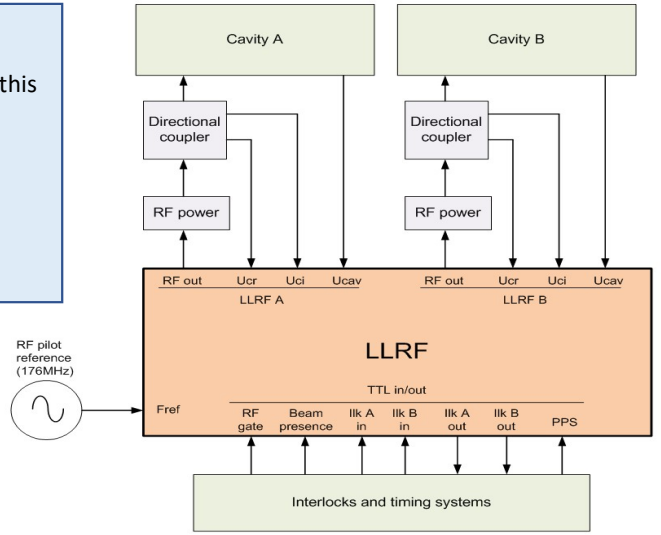
One of the crucial control systems of any particle accelerator is the Low Level Radio Frequency (LLRF). The purpose of a LLRF is to control the amplitude and phase of the field inside the accelerating cavity. The LLRF is a subsystem of the CEA control domain for the SARAF-LINAC instrumentation and Seven Solutions has designed, developed, manufactured and tested the system based on CEA technical specifications. The final version of this digital LLRF will be installed in the SARAF accelerator in Israel at the end of 2021. The architecture, design and development as well as the performance of the LLRF system will be presented in this poster. The benefits of the proposed architecture and the first results will be shown.

SARAF (Soreq Applied Research Accelerator Facility) in Israel

Constructed at Soreq Nuclear Research Center (SNRC). The main scientific objectives of this facility are:

- Search for Beyond Standard Model Physics
- Nuclear Astrophysics
- High Energy Neutron Induced Cross Sections
- Neutron Based Material Research/Neutron Based Therapy
- Development of New Radiopharmaceuticals
- Accelerator based neutron imaging





Superconduction Linear Accelerator	
Parameter	Value
Ion Species	Protons/Deuterons
Energy Range	1. 5 Me. V/u – 40 Me. V
Current Range	0. 04 – 5 m. A CW
Operation	6000 hours/year
Availability	> 90%

LLRF Requirements

The LLR is a key component to regulate RF filed inside the cavities. It operates in close loop maintaining the cavity gradient and phase stability when operating the cavity with beam.

Operating frequency range: 175-177 MHz

Delay: < 1us

Amplitude measurement RMS error: < 0.03%

Phase measurement RMS error: < 0.03 °

Output amplitude uncertainty: < 5%

Output phase uncertainty: < 5 °

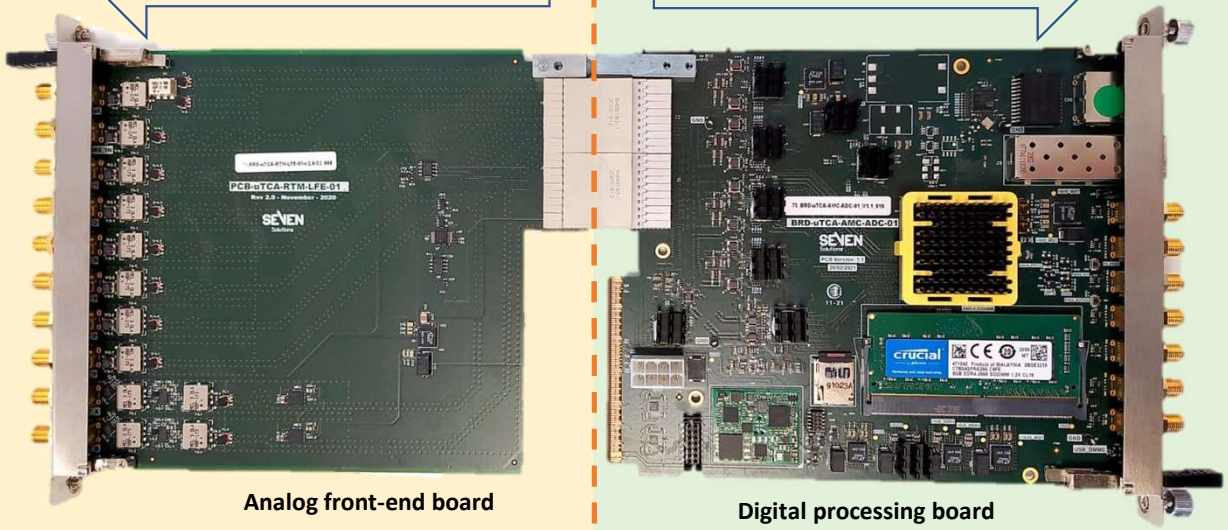
uTCA LLRF hardware architecture

LFE (LLRF Front-End) board

- uRTM with double height and mid-size form factor uTCA.4
- SMA connectors:
  - 1 RF input for Fref: 176 MHz sine wave for LLRF reference
  - 6 x RF input signals to condition two LLRF channels
  - 1 x RF input Spare for future functionality
  - 2 x RF output channels
- Band pass filters in all the RF paths.
- Temperature sensor
- EEPROM memory
- Output amplifier in both channels

Analog

Digital



Analog front-end board

Digital processing board

ADC board (AMC digitizer controller)

- AMC with double height and mid-size form factor uTCA.4
- 10 x Analog to digital converters (ADCs)
- 2 x Digital to analog converters (DACs)
- Zynq UltraScale+ FPGA from Xilinx as main processing element
- PLL to generate the different clock signals needed
- 8GB DDR4 memory for processor and data storage (postmortem analysis)
- uTCA MMC stamp
- Temperature sensor
- uSD socket
- uUSB port
- ETH port
- SFP port (White Rabbit compatible)

Front panel of LFE board

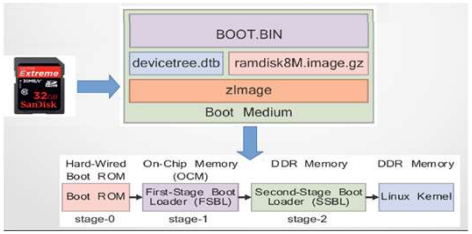
Front panel of ADC board

Empty	Empty	CU
Timing Board	MCH-PHYS80	
ADC Board 1		
ADC Board 2	Empty	

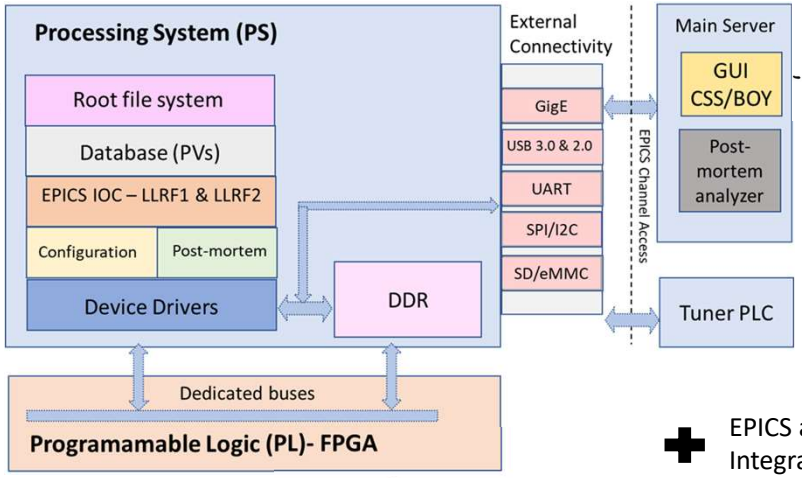
CU	Empty	Empty
	MCH-RTM-COMex-E3	Empty
	Power Unit	LFE Board 1
		LFE Board 2

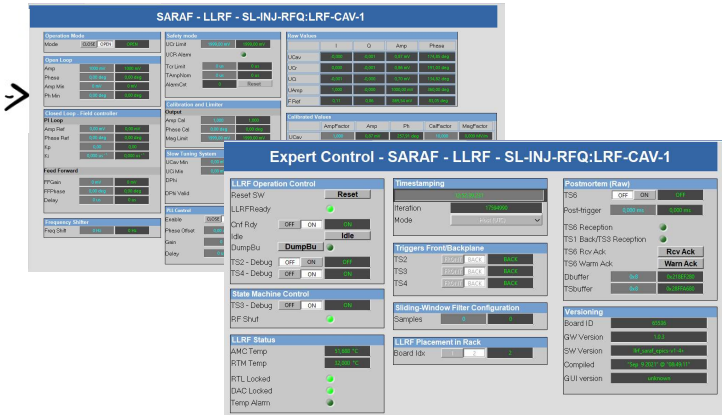
- NATIVE-R2 uTCA.4 from N.A.T. (up to 5 LLRF boards - AMC + RTM)
- NAT-MCH-PHYS80
- NAT-MCH-RTMCOMex-E3 for direct access to the facilities located on the NAT-MCH-PHYS80
- Timing gating and triggers:
  - 4 shared backplane lines
  - 4 point-to-point backplane lines

Gateware/Software architecture – 2 LLRF on 1 single board



- Buildroot for OS Image:
  - BOOT.bin: FPGA image
  - Uboot: instructions to boot the devices
  - Devicetree: mapping of devices of the system
  - zImage: linux kernel image



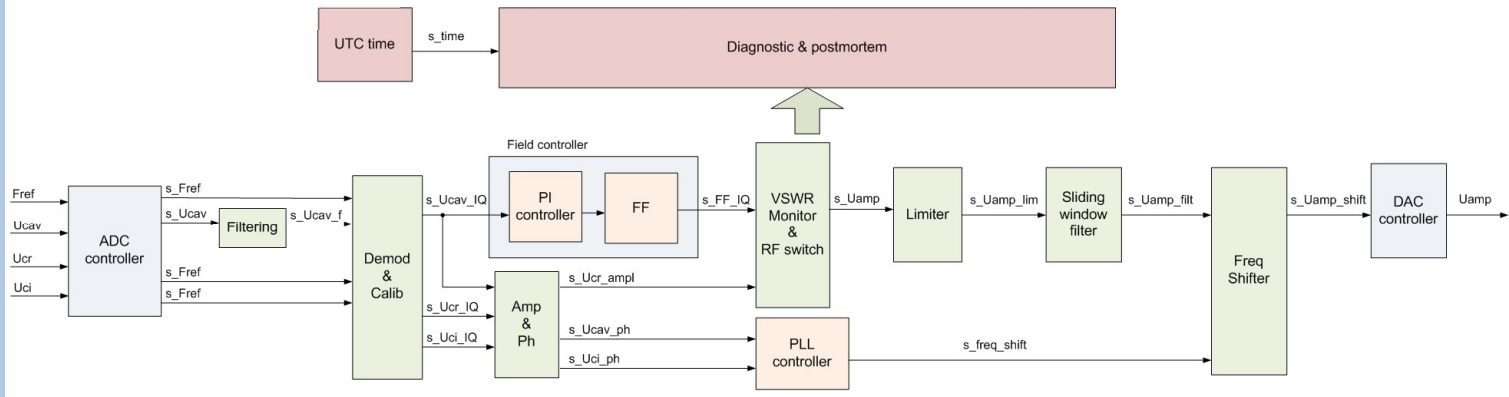


✚ EPICS as Control system (asynPortDriver, databases, PV, autosave…)
Integrated libraries for FPGA/ARM communication (AXI based)

2 LLRF IOCs with complete functionality

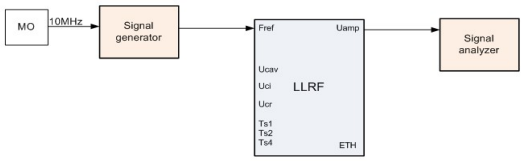
Main Gateware Controllers

- Continuous and pulsed amplitude and phase cavity field
- Opened loop or closed loop of amplitude and phase
- Pulse shaping feature for smoothing RF pulses
- Feedforward for beam loading compensation
- Real-time monitoring of RF signals (Incident, reflected, cavity field …)
- Provides information for step tuner motors VSWR (arcing/reflection) detection and handling events: when it receives a reflection signal above a user-defined threshold, it shuts off RF output for a time period also defined by the user
- Fast output interlock system (Machine protection)
- Postmortem analysis with selectable event triggers and configurable capture parameters
- Compatible with White-Rabbit and IEEE-1588 protocols



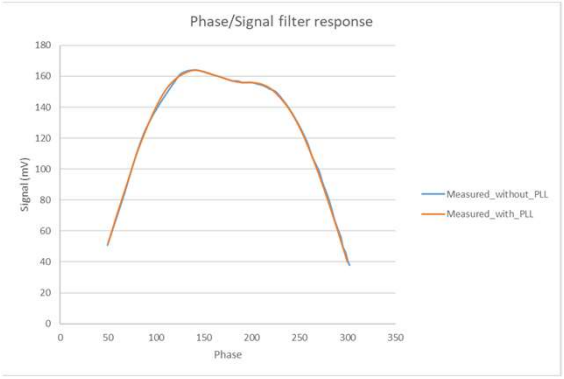
Measured Performance

Low jitter addition at the outputs



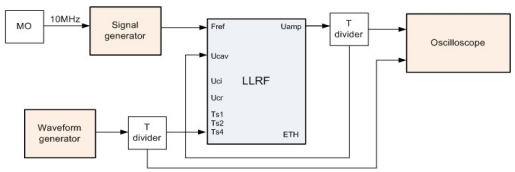
LLRF additive phase noise of only 182 fs

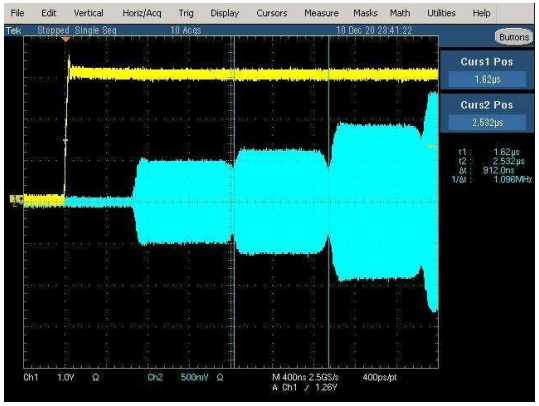
PLL Capability



Frequency closed loop for tracking the cavity resonant frequency in opened loop

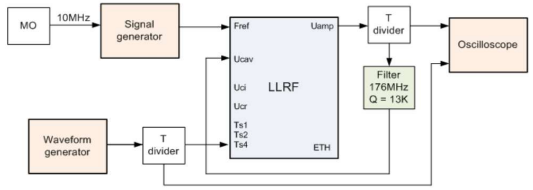
Low response time – PI delay

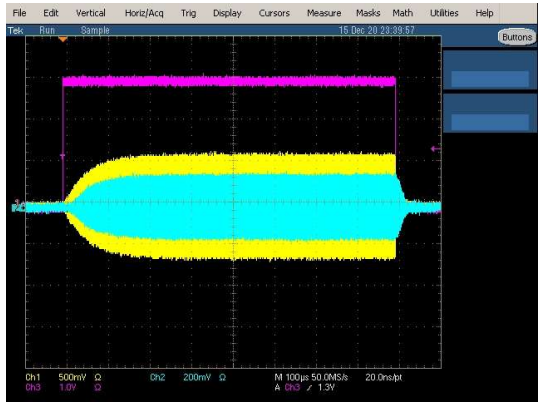




The duration of the steps produced by the effect of Kp determine the total loop delay of the system from Ucav to Uamp (delay < 1us)

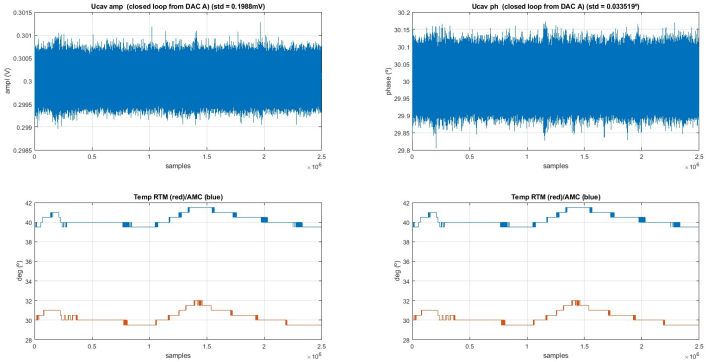
PI loop for amplitude & phase regulation





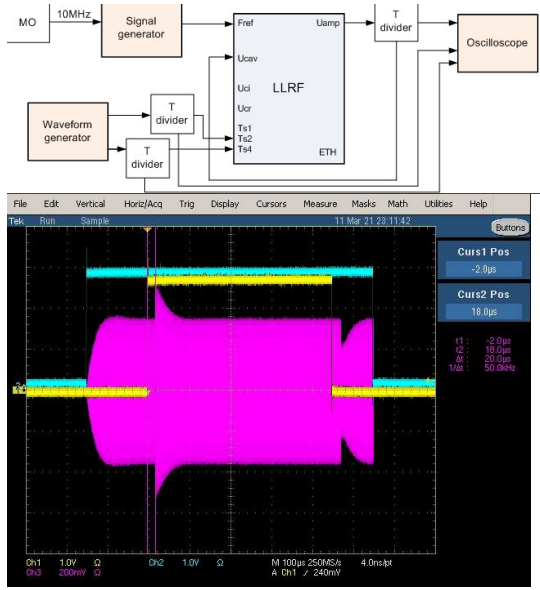
In pink, RF gate signal; in yellow RF output; in blue UCav. A high Q filter is used to emulate the cavity behaviour. The PI controller keep constant the cavity field

Long term temperature test



Great cavity regulation long-time stability with temperature changes

Feedforward feature



In blue RF gate signal; in yellow beam presence gate; in Pink RF output. Configurable gain and phase used to compensate the beam loading

Moreover…

- Amplitude stability: 0.02%
- Phase stability: 0.3 degree
- Amplitude precision: 0.03% Vpp
- Phase precision: 0.03 degrees