THPV033

Reusable Real-Time Software Components for the SPS Low Level RF Control System

M. Suminski*, K. Adrianek, B. Bielawski, A. C. Butterworth, J. Egli, G. Hagmann,
P. Kuzmanovic, S. Novel Gonzalez, A. Rey, A. Spierer, CERN, Geneva, Switzerland

ICALEPCS 2021

Introduction

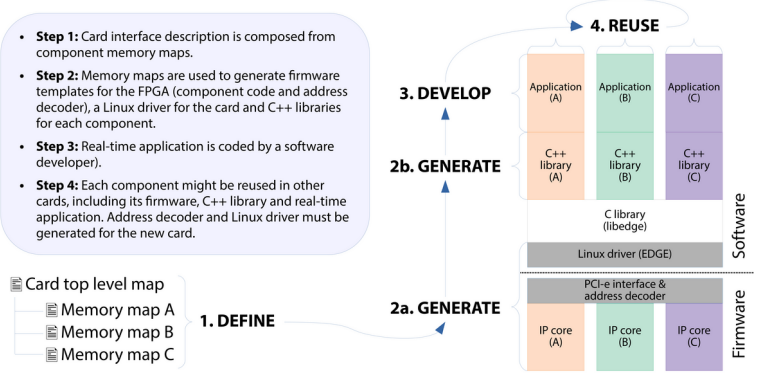
In 2021 the Super Proton Synchrotron has been recommissioned after a complete renovation of its Low Level RF system (LLRF). The new system has largely moved to digital signal processing, implemented as a set of functional blocks (IP cores) in Field Programmable Gate Arrays (FPGAs) with associated software to control them. Some of these IP cores provide generic functionalities such as timing, function generation and signal acquisition, and are reused in several components, with a potential application in other accelerators.

The update has brought many benefits, one of them being increased hardware density: what used to take an entire crate full of VME modules is now done by one or two microTCA cards. It has also affected the architecture of the LLRF control system: from the former approach of a single VME card performing a single function (with its own driver, user-space library and application), to fitting multiple IP cores with different functionalities in the same board.

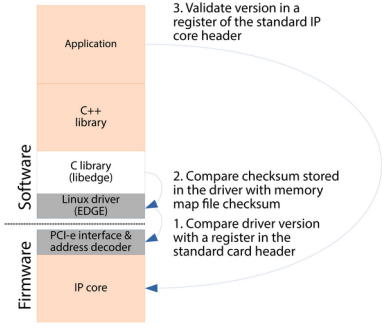
In order to match the requirements of the new IP/component model, a new solution for memory map management had to be defined.

Workflow

- **Step 1:** Card interface description is composed from component memory maps.
- **Step 2:** Memory maps are used to generate firmware templates for the FPGA (component code and address decoder), a Linux driver for the card and C++ libraries for each component.
- **Step 3:** Real-time application is coded by a software developer).
- **Step 4:** Each component might be reused in other cards, including its firmware, C++ library and real-time application. Address decoder and Linux driver must be generated for the new card.



Version validation



Components tend to change, but it is important to keep all layers compatible. Without it, it is very likely that the component will misbehave in an unpredictable way.

To prevent such problems, there are multiple checks to assure compatibility between different layers of a component stack. When at least one of the checks fails, the software will not start and indicate an incompatibility.

Results

- The concept has been successfully validated during the SPS LLRF renovation.
- Multiple components have been designed and reused in new Cavity Controller and Beam Control microTCA cards. No changes in the software or firmware were required to reuse the same IP on a different board.
- The new components can be ported to platforms other than microTCA.
- The new IP model improves the firmware and software development process by making it more decoupled from specialized hardware.

Introduction

In 2021 the Super Proton Synchrotron has been recommissioned after a complete renovation of its Low Level RF system (LLRF). The new system has largely moved to digital signal processing, implemented as a set of functional blocks (IP cores) in Field Programmable Gate Arrays (FPGAs) with associated software to control them. Some of these IP cores provide generic functionalities such as timing, function generation and signal acquisition, and are reused in several components, with a potential application in other accelerators.

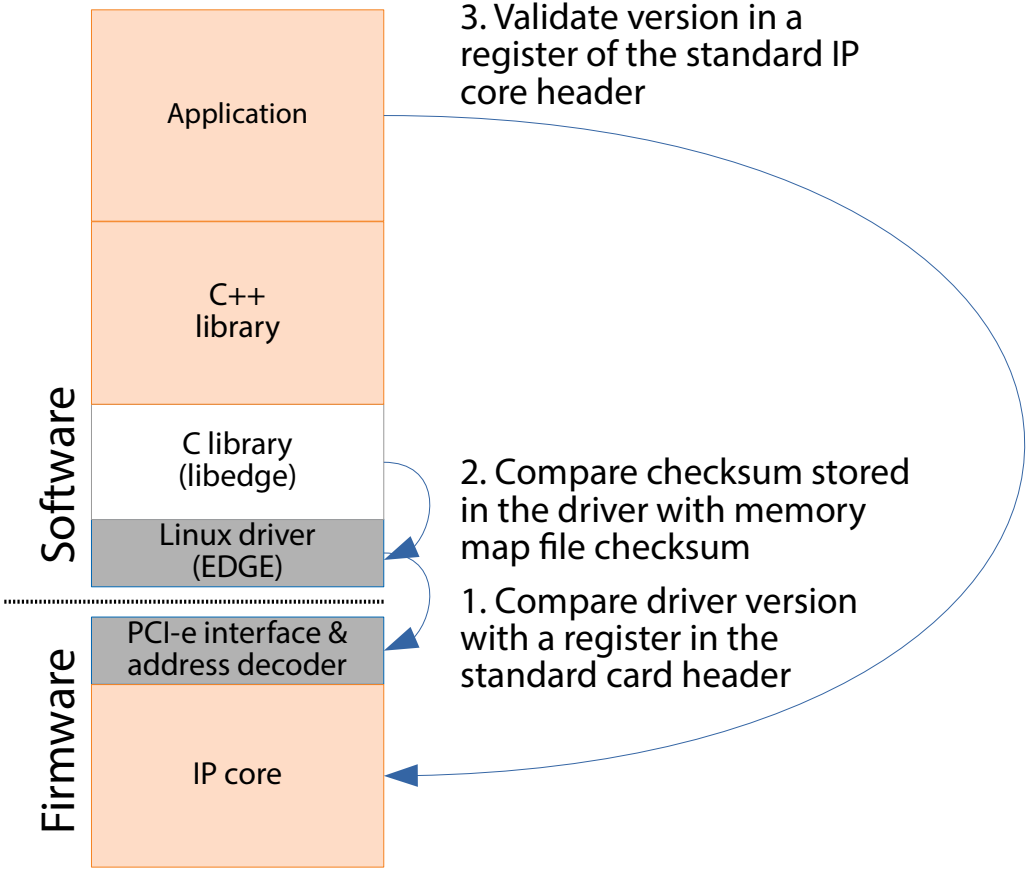
The update has brought many benefits, one of them being increased hardware density: what used to take an entire crate full of VME modules is now done by one or two microTCA cards. It has also affected the architecture of the LLRF control system: from the former approach of a single VME card performing a single function (with its own driver, user-space library and application), to fitting multiple IP cores with different functionalities in the same board.

In order to match the requirements of the new IP/component model, a new solution for memory map management had to be defined.

Workflow

- **Step 1:** Card interface description is composed from component memory maps.
- **Step 2:** Memory maps are used to generate firmware templates for the FPGA (component code and address decoder), a Linux driver for the card and C++ libraries for each component.
- **Step 3:** Real-time application is coded by a software developer).
- **Step 4:** Each component might be reused in other cards, including its firmware, C++ library and real-time application. Address decoder and Linux driver must be generated for the new card.

Version validation



Components tend to change, but it is important to keep all layers compatible. Without it, it is very likely that the component will misbehave in an unpredictable way.

To prevent such problems, there are multiple checks to assure compatibility between different layers of a component stack. When at least one of the checks fails, the software will not start and indicate an incompatibility.

Results

- The concept has been successfully validated during the SPS LLRF renovation.
- Multiple components have been designed and reused in new Cavity Controller and Beam Control microTCA cards. No changes in the software or firmware were required to reuse the same IP on a different board.
- The new components can be ported to platforms other than microTCA.
- The new IP model improves the firmware and software development process by making it more decoupled from specialized hardware.