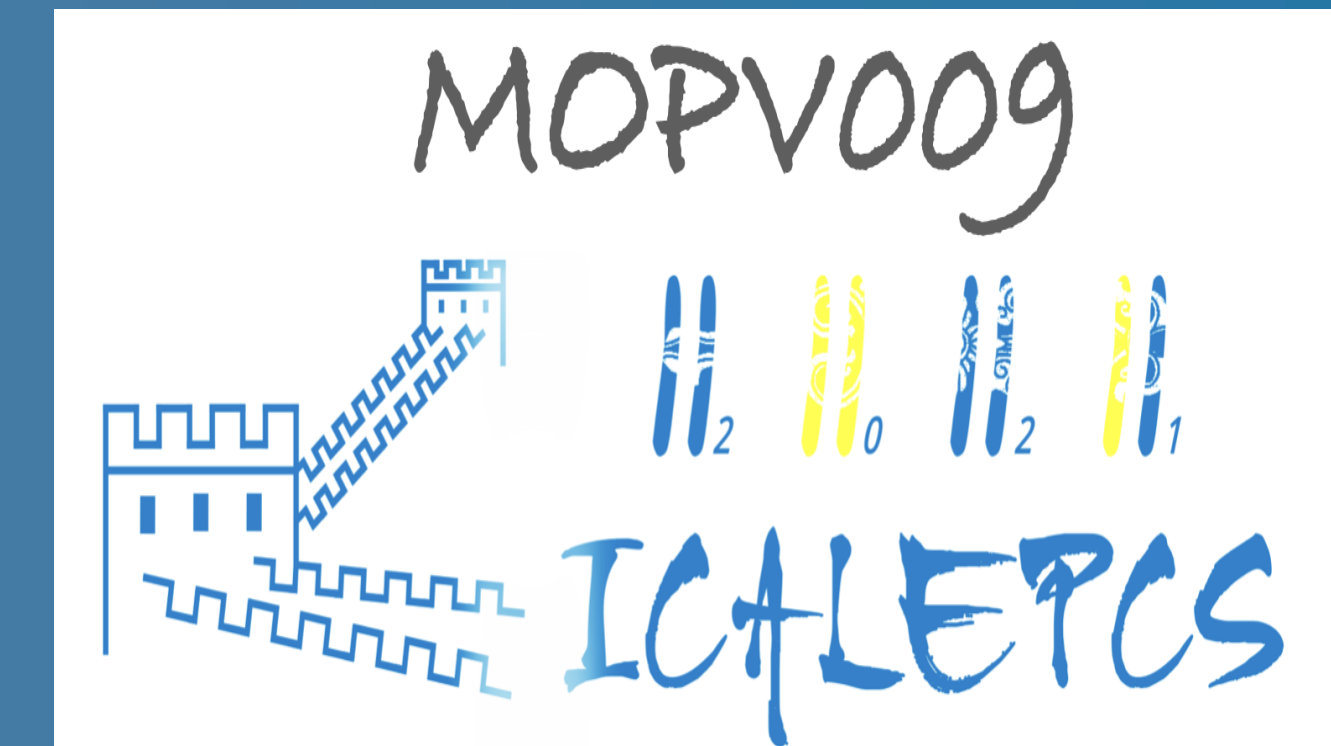




# THE HV DCS SYSTEM FOR THE NEW SMALL WHEEL UPGRADE OF THE ATLAS EXPERIMENT

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## INTRODUCTION

The ATLAS Muon Spectrometer will exceed its design capabilities in the high background radiation as expected towards the HL-LHC. In order to cope with the foreseen limitations, the collaboration decided to replace the Small Wheel (SW) with a New SW (NSW) by combining 2 detector technologies, namely small-strip Thin Gap Chambers (STG) & and resistive Micromegas (MMG). Both technologies are "aligned" to the ATLAS general baselines for the NSW upgrade project, maintaining in such way the excellent performance of the system beyond Run-3. Complementary to the R&D of these detectors, an intuitive control system was of vital importance. The principal task of the DCS is to enable the coherent and safe operation of the detector by continuously monitoring its operational parameters and its overall state.

## FSM HIERARCHY AND LOGIC

The control system is represented by an homonymous Finite State Machine (FSM) node, MMG & STG, defined as the main control unit (CU), from where commands are propagated downwards into the device (DU) or logical elements (LU). Such units, groups and geographical detector segments are represented by device-oriented (SMI) FSM objects. Figure 1 shows an instance of the MMG FSM tree along with each commands.

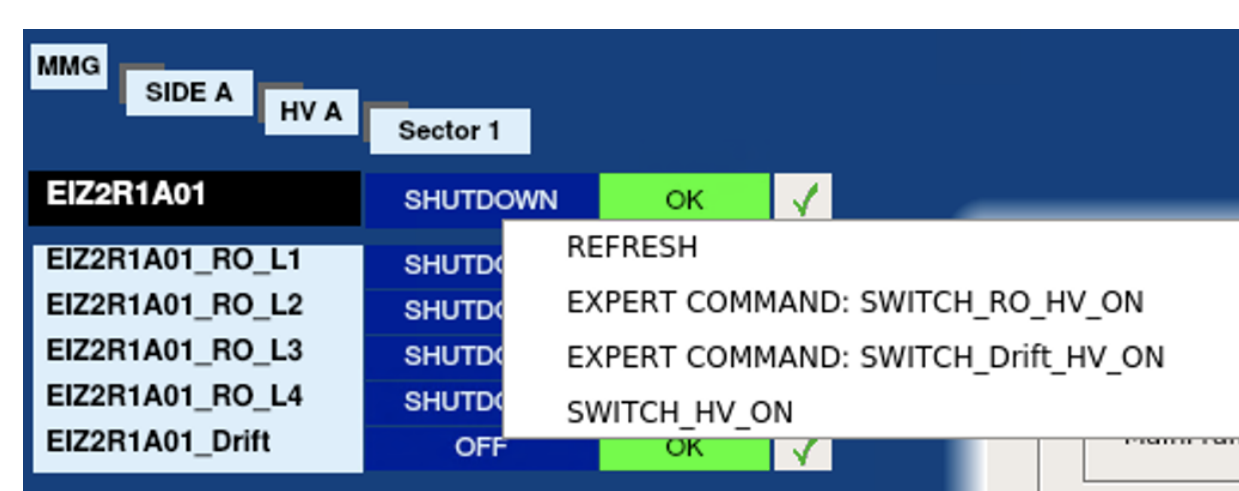


Figure 1: MMG FSM Tree instance at chamber level.

The current condition of each object is determined by a set of states alongside with their transitions. The actual state is determined by the states of the associated children (DU,LU,CU) via state rules implemented using SML and they propagate upwards (LU,CU). A state transition is triggered either by a condition change or by a dedicated action. Figure 2 depicts the device and logical state diagrams. It allows:

1. a DU to change from its ground state OFF to its operational state ON via optional stages.
2. a LU or CU to reflect conditions for which data taking is possible or not.
3. an UNKNOWN state when the condition cannot be verified.

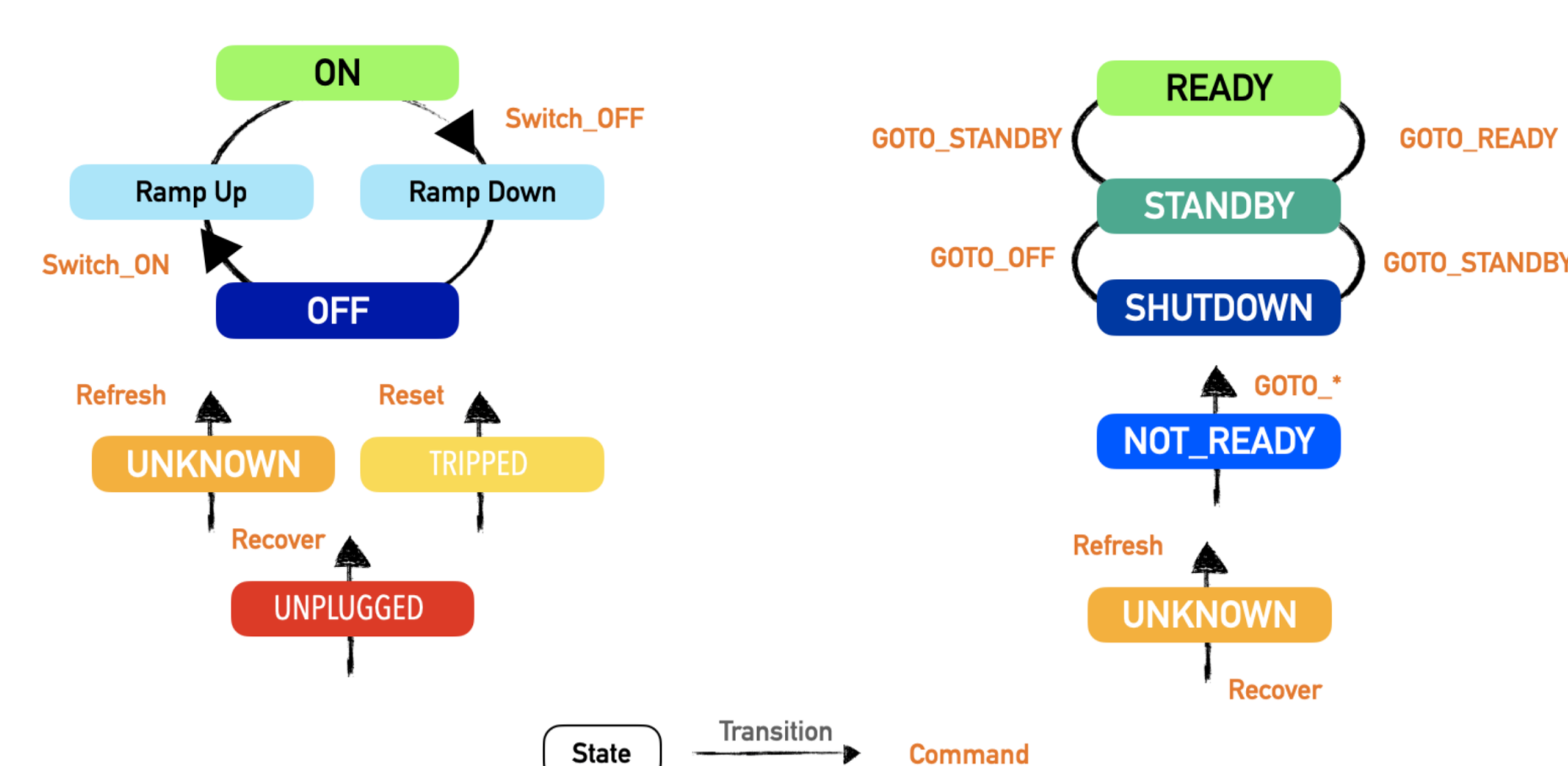


Figure 2: Device (left) and Logical (right) object state model.

## HARDWARE ARCHITECTURE AND REQUIREMENTS

The system architecture consists of several components based on the sub-detector needs. It is supplied by the Universal multichannel CAEN system, and depicted in Figure 3. Among its main requirements are:

- Remote control, monitoring and configuration of a wide variety of parameters, like voltage and current set/readback, state and status values along with error flags. Data can be exchanged with other sub-systems.
- Active archiving with smoothing and on-the-flight storage in the DCS database.
- Compatibility with operation under radiation and magnetic field as in the ATLAS cavern.

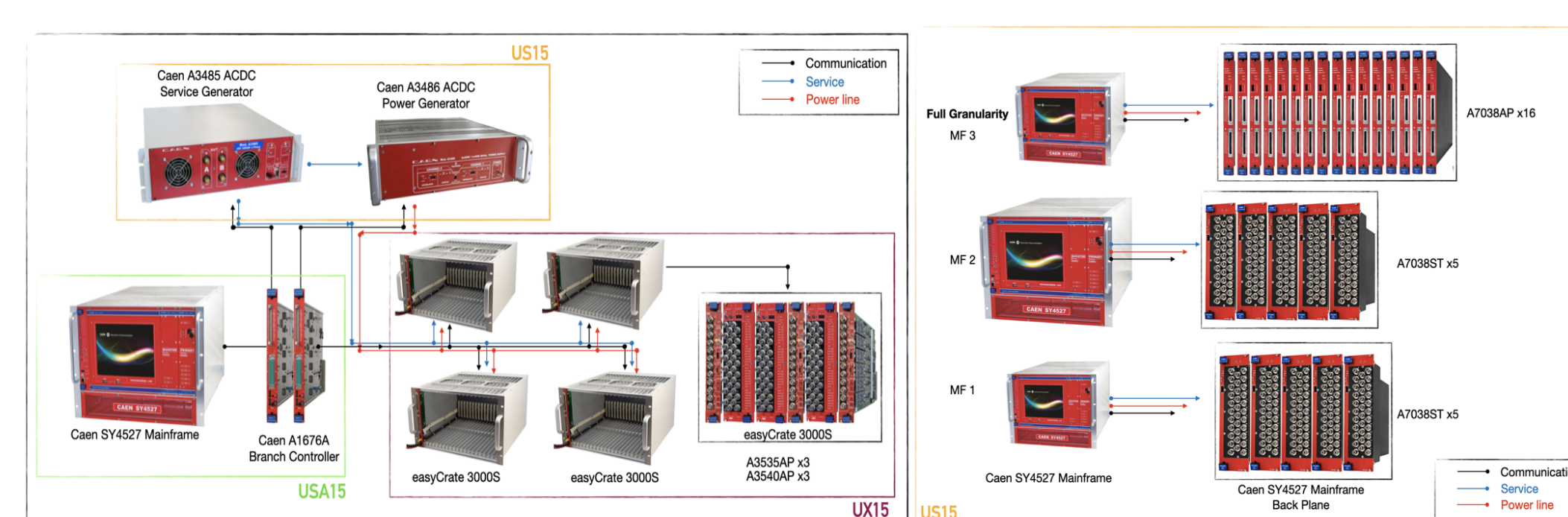


Figure 3: The hardware chain of the STG (left) and the MMG (right) as has been installed at ATLAS P1.

- Automated mechanisms, such as the safety Interlock, the Reset Trip, the HV transition when the Beam for Physics is expected or not, etc.
- Communication is established via the OPC UA server-client pairing.



Figure 4: The GUI of the 48V Generators (left) and the SY4527 mainframes (right).

## ALARM SCHEME

A powerful alert system provides:

1. dedicated status instances (OK, WARNING, ERROR, and FATAL) signaling a problem in the corresponding part of the detector, attributed to different severity levels (Warning, Error, Fatal).
2. notifications about detected anomalies/malfunctions of the system on the flight,
3. instructions required for recovery.

Figure 5: The Alarm Screen.

## OPERATION PANELS

1. follow the existing look, feel and command architecture of the other Muon sub-systems,
2. facilitate the shifter/expert operations,
3. holds the system's overall view,
4. provide the user with useful information, reflecting the state and status of the detector's constituents,
5. display the vitals of the system in table or trend-plot format.



Figure 6: Operational Panels for both MMG and STG sub-systems.



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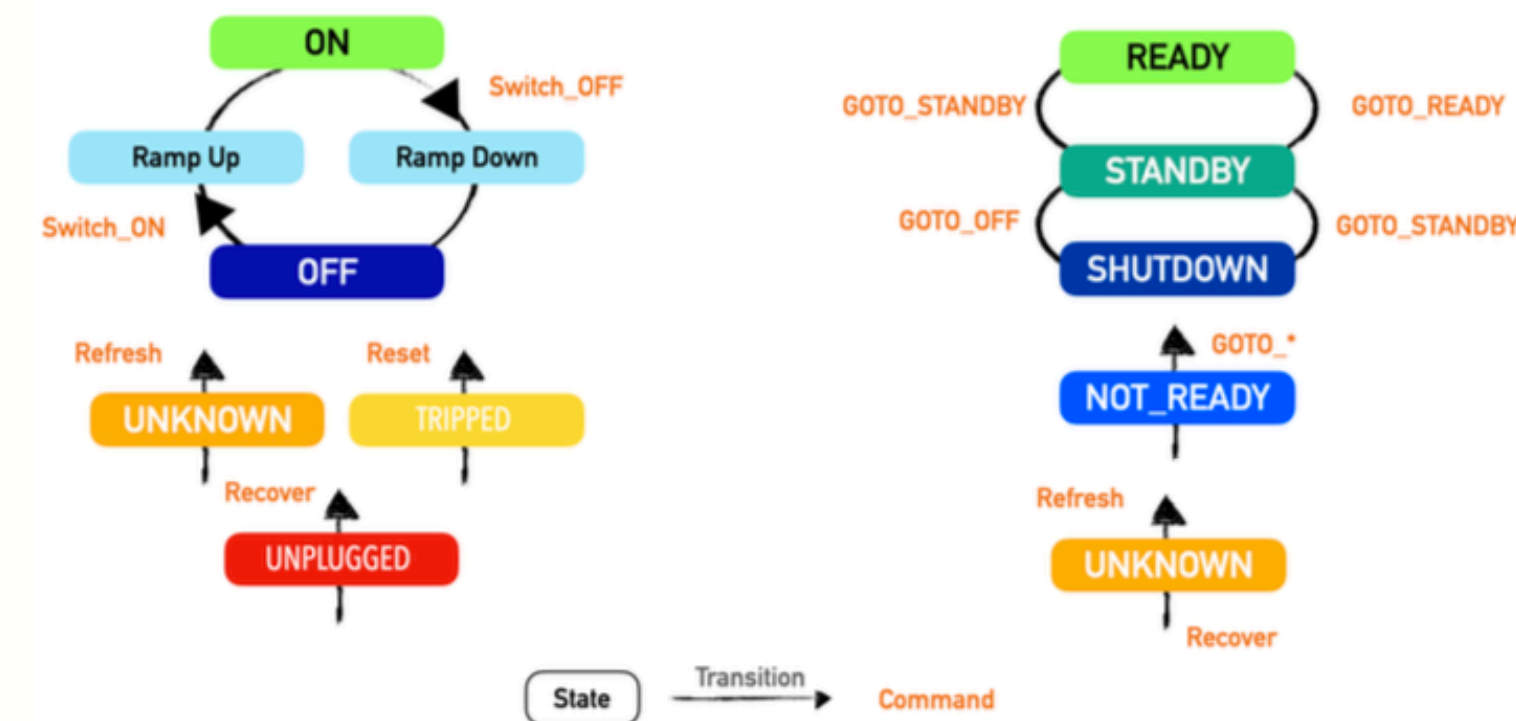


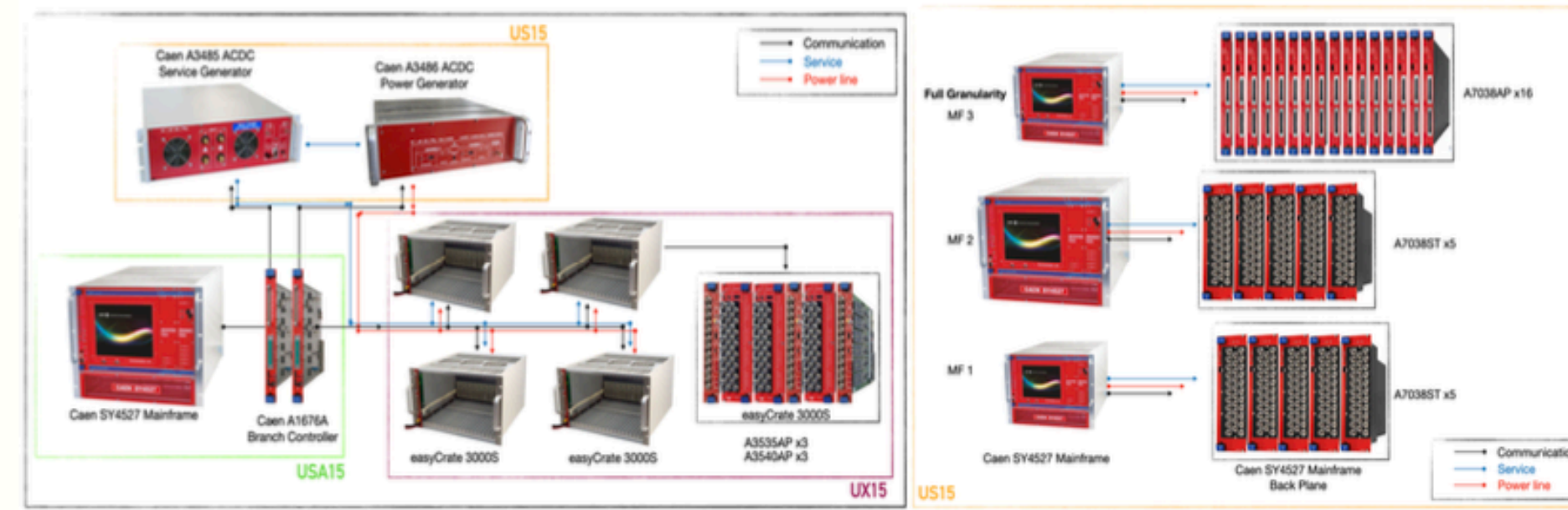
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# Architecture & Hardware Requirements

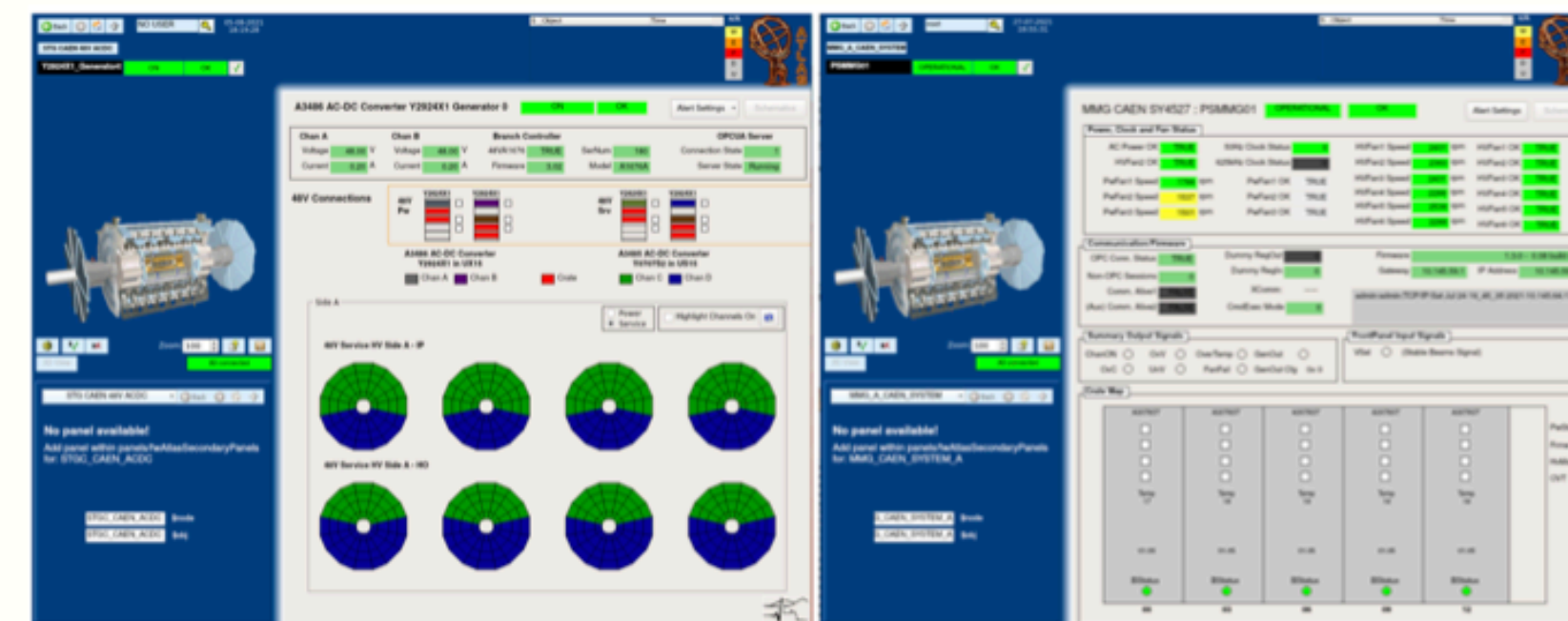
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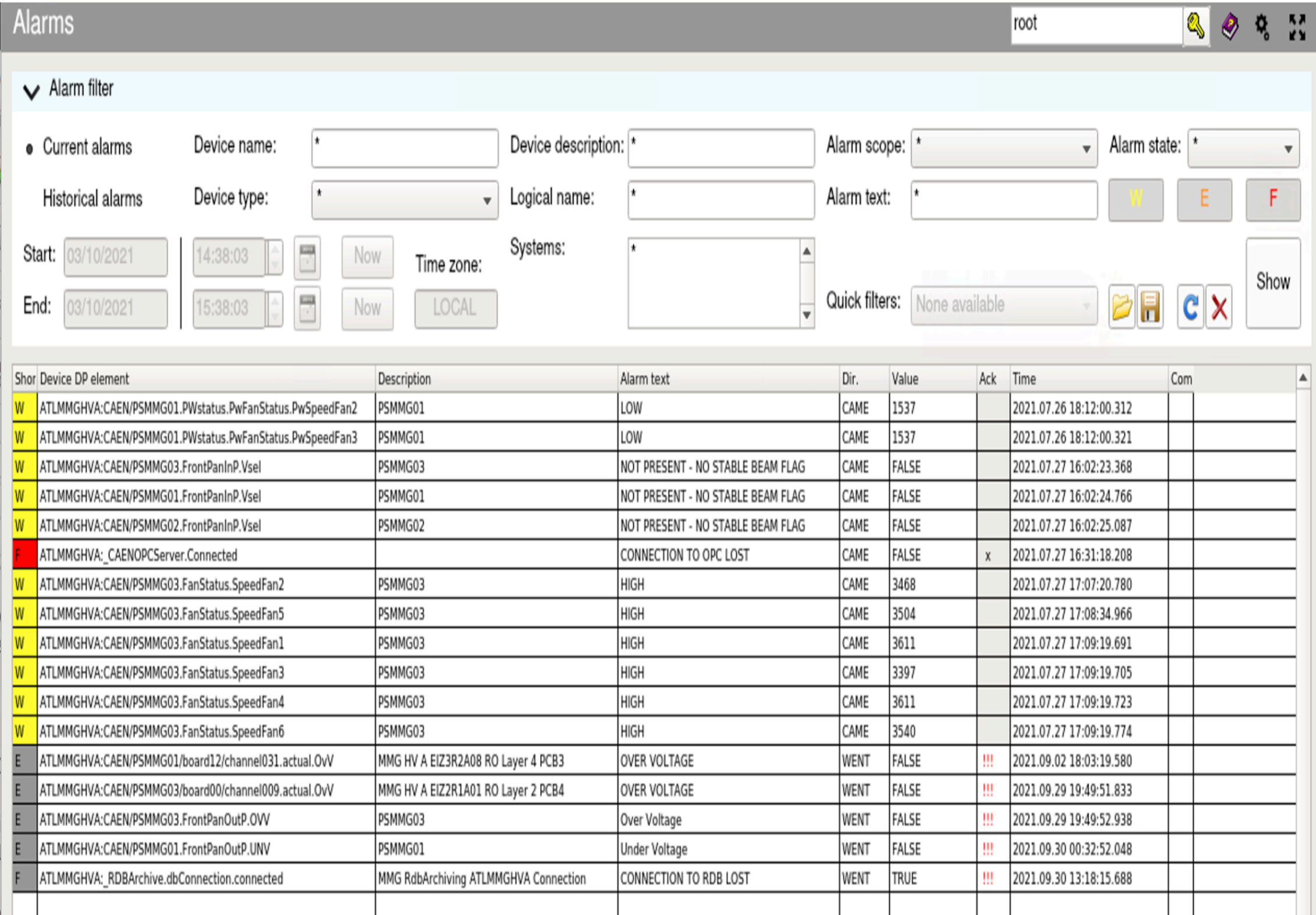


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