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# R&D STUDIES FOR THE ATLAS TILE CALORIMETER DAUGHTERBOARD * †

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*Abstract*

The ATLAS Hadronic Calorimeter DaughterBoard interfaces the on-detector with the off-detector electronics. The DaughterBoard features two 4.6 Gbps downlinks and two pairs of 9.6 Gbps uplinks powered by four SFP+ Optical transceivers. The downlinks receive configuration commands and LHC timing to be propagated to the front-end, and the uplinks transmit continuous high-speed readout of digitized PMT samples, detector control system and monitoring data. The design minimizes single points of failure and mitigates radiation damage by means of a double-redundant scheme. To mitigate Single Event Upset rates, Xilinx Soft Error Mitigation and Triple Mode Redundancy are used. Reliability in the high speed links is achieve by adopting Cyclic Redundancy Check in the uplinks and Forward Error Correction in the downlinks. The DaughterBoard features a dedicated Single Event Latch-up protection circuitry that power-cycles the board in the case of any over-current event avoiding any possible hardware damages.

We present a summary of the studies performed to verify the reliability if the performance of the DaughterBoard revision 6, and the radiation qualification tests of the components used for the design.

## INTRODUCTION

The instantaneous luminosity at HL-LHC will be increased by a factor of five compared to the LHC. Consequently, the read-out systems of the ATLAS detector [1] will be exposed to higher radiation levels and increased rates of pileup. The current electronics for the read-out system of the ATLAS Tile Calorimeter (TileCal) will not be able to handle the new requirements imposed by the HL-LHC. R&D work is ongoing to upgrade the TileCal electronics with a new design that will provide continuous digital read-out of all the calorimeter cells with better energy resolution, improved timing and less sensitivity to out-of-time pileup [2]. The upgrade R&D work requires Total Ionizing Dose (TID), Non Ionizing Energy Loss (NIEL) and Single Event Effects (SEE) tests to be performed on the upgraded on-detector electronics, to qualify the design as reliable for the HL-LHC radiation environment.

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## ATLAS TILE CALORIMETER

TileCal is a sampling calorimeter with plastic scintillator tiles and steel plates as active and absorber materials, respectively. TileCal is longitudinally divided into four cylindrical barrels (Fig. 1b) each comprising 64 wedge-shaped modules (Fig. 1c). Scintillator light is collected on each side of a pseudo-projective cell by wavelength shifting fibers and read out by a pair of PMTs.

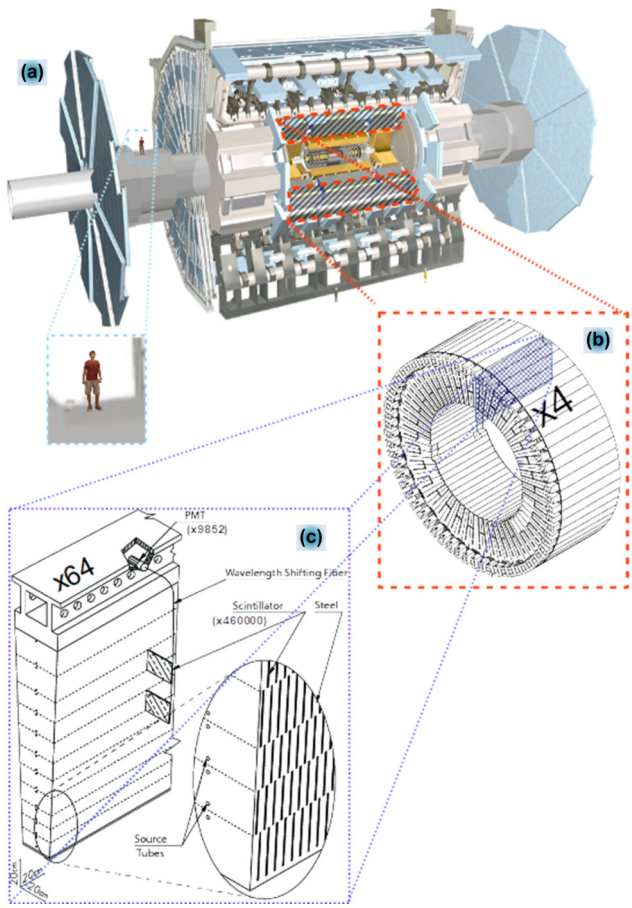


Figure 1: (a) The ATLAS detector. (b) A TileCal barrel. (c) Depiction of a TileCal wedge-shaped module.

## THE TILECAL HL-LHC UGPRADE SYSTEM

The TileCal HL-LHC upgrade on-detector electronics will continuously sample data from all TileCal PMTs at 40 MHz by means of 896 independent modules, so-called MiniDrawers (MD). Each MD servicing up to six pairs of

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PMT channels, each pair sampling the light coming from the same TileCal cell. Each PMT signal is conditioned, shaped and fed into amplifiers with low- and high-gain by a Front-end electronics (FENICS) card, before they are digitized by a MainBoard (MB, Fig. 2). A read-out link and control DaughterBoard (DB) receives and propagates LHC synchronized timing, control and configuration to the front-end, while transmitting continuous read-out of the MB channels to the off-detector systems. Each MD is independently powered by radiation tolerant Low Voltage Power Supplies (LVPS) sitting on-detector and designed to withstand the radiation requirements of the HL-LHC.

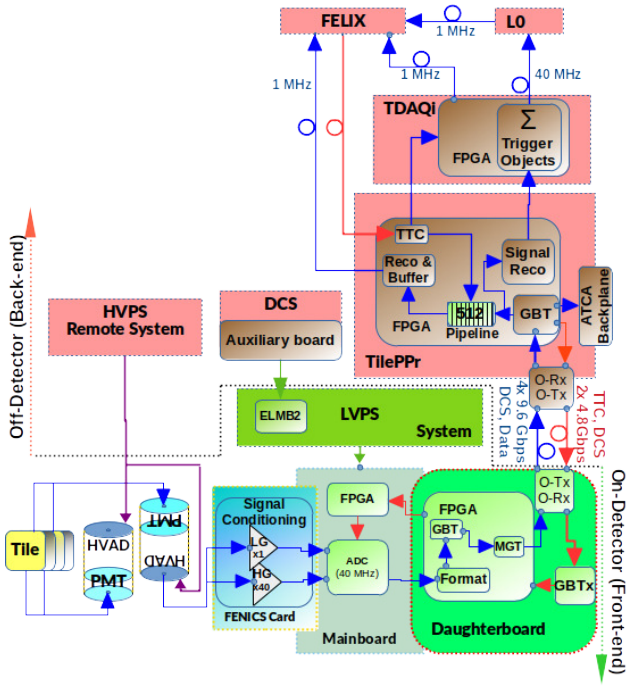


Figure 2: Block diagram for the On-Detector and Off-Detector electronics.

On the off-detector, Tile Processors (TilePPrs) receive the PMT digitized data and store it in pipelines (Fig. 2). The TilePPr will send all the digitized data to the Level 0 (L0) trigger system through the Trigger and DAQ interface (TDAQi) at 40 MHz, and the Front-End Link eXchange (FELIX) system will read-out data stored in the TilePPr pipelines at 1 MHz if a trigger decision is made. The power will be controlled, monitored and distributed to the on-detector electronics by the Detector Control System (DCS) interfaced LVPS, while the High Voltage Power Supply (HVPS) remote system will provide high voltage to the High Voltage Active Dividers (HVAD) sitting the PMTs.

The front-end electronics of TileCal include multiple, complementary test and calibration systems. These are the charge injection system (CIS), the laser calibration system and the Caesium (Cs) source calibration system. The CIS sends electronic pulses with configurable amplitude can be injected into the system in order to test the behaviour of the digitization and read-out chain of each channel over its full dynamic range. The LASER system distributes short, controlled light pulses over optical fibres to the light mixers of the PMT blocks to allow measurements of individual PMT gains of each PMT in the absence of collisions. The Cesium system uses radioactive $^{137}Cs$ $\gamma$ sources that are moved hydraulically through water-filled tubes that pass through each scintillating tile in the calorimeter, producing strong, slow signals read by a separate read-out path is implemented with a slow integrator circuit read-out by ADCs sitting in the FENICS cards.

## THE DAUGHTERBOARD REVISION 6

The DB Revision 6 (DB6, Fig. 3) design aims to solve the radiation tolerance issues found in the previous revision while incorporating a more robust timing design and extra features that will allow minimizing single points of failure one step further. The DB6 consists in a radiation tolerant and electrically redundant board that serves as a hub that interconnects the on-detector and off-detector electronics of the HL-LHC TileCal Upgrade System by means of four Small Form-Factor Pluggable+ (SFP+) modules and a 400 FPGA Mezzanine Card (FMC) connector. A block diagram for the design of the DB6 is shown in Fig. 4. The design consists in equal and electrically independent halves, each capable of servicing the six PMT channels that correspond to the half of the MD interfaced with the DB.

Two CERN radiation-hard GBTx ASICs will receive two GBT-FEC protected 4.8 Gbps downlinks with LHC synchronized clocks and configuration commands. Each GBTx recovers two 160 MHz good quality LHC synchronized clocks in order to drive the GTH transceivers of both FPGAs, two 40 MHz Trigger, Timing and Control (TTC) synchronous clocks to drive the relevant logic of the KU FPGAs, and four 40 MHz TTC phase configurable clocks to drive the digitizing blocks and calibration signals on each MD quadrant. Two Xilinx KU XCKU035 FPGAs powered by TMR capable firmware provide continuous GBT-CRC protected words to the four 9.6 Gbps uplinks with all the Detector Control System (DCS) and PMT digitized data. The DB6 design allows nominal running with at least one working downlink and two working uplinks. By means of the FMC connector interface, the KU FPGAs send all the front-end configuration commands and phase-configurable LHC synchronized clocks and receive MB power monitoring information, data from slow current integrator ADCs that sit in the FENICS cards, and samples of two-gains of the signals coming from each PMT digitized by fast ADCs sitting on the MB. Additionally, two buses will allow communication between FPGAs from both halves of the DB, a slow bus (CommBUS) powered by IDDR/ODDR IOs and a high speed 9.6 Gbps bus powered by interconnected GTH transceivers (GTHBUS), allowing signal monitoring, in addition to trigger commands and data interchange between both FPGAs. The DB6 features two Microsemi ProASIC FPGAs to control the remote KU FPGA resets, manage the

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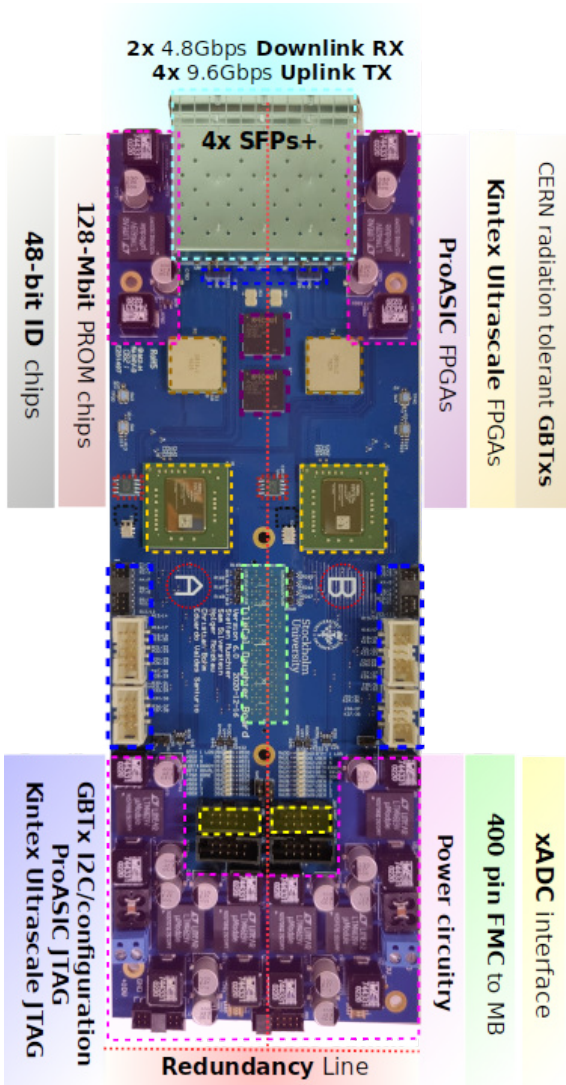


Figure 3: The DaughterBoard revision 6.

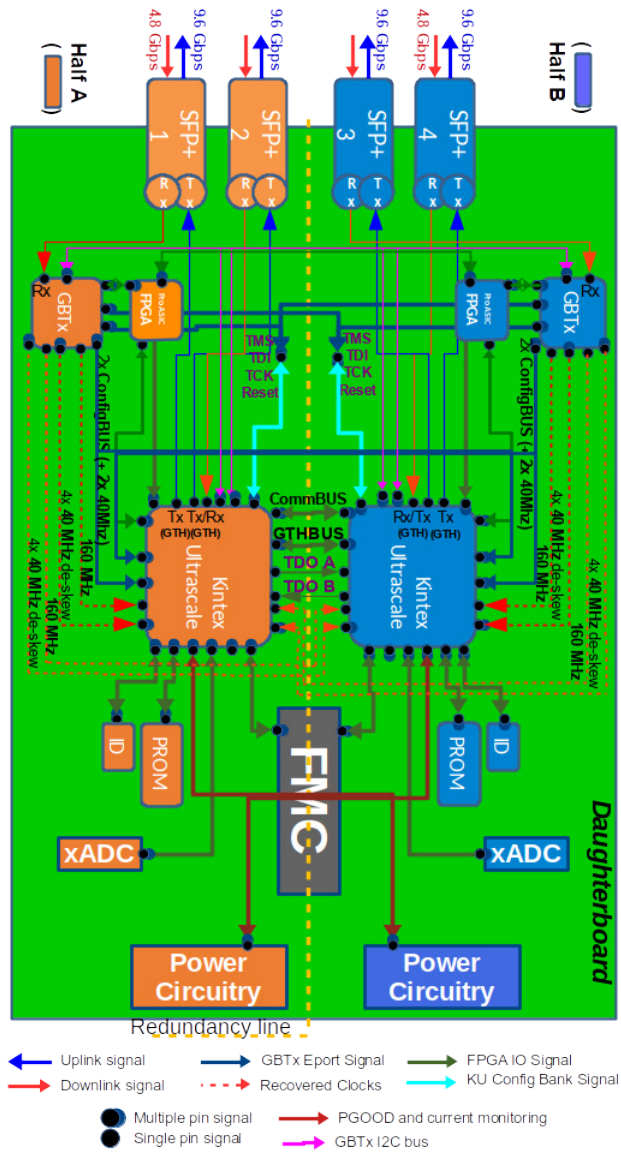


Figure 4: The DaughterBoard revision 6 block diagram.

initialization of the GBTxs and the KU FPGAs, and buffer the JTAG interface signals received from the off-detector by the GBTx that allow remote reconfiguration of the KU FPGAs and their attached FLASH memories. Additionally, the DB6 design includes an xADC header per FPGA for extra analogue sensor monitoring capabilities, and digital ID serial chips for unique MD half identification.

The firmware of the KU FPGAs are in charge of reading out the dual-gain PMT digitized data and formatting it into GBT-CRC protected words. The firmware has a complex clock and timing scheme with multiple clock inputs from various sources such as the two GBTxs, an oscillator and the six ADCs sitting on a MB half. Some of the these clocks are being asynchronously multiplexed depending on the availability of the GBTx links. The DB6 design routing was optimized to take advantage of the Ultrascale dedicated XYPHY BITSLICE byte groups architecture [3]. The bit and flame clocks, and high-gain and low-gain serial data signals coming from each ADC channel will be routed to the same byte XYPHY BITSLICE group. The byte groups used for each specific are 1 or 2, since they contain the dedicated Global Clock Capable IO pins (GCIO) that allow direct access to the Phase Locked Loops (PLLs) and the Mixed-Mode Clock Manager (MMCM) of the bank, and assures that there is no congestion with more than 6 clocks driving IO loads on any half bank. Figure 5 shows the scheme followed for the clock input distribution and the routing of signals of the ADCs and other relevant time-dependent data paths to the different banks. This scheme makes sure that successful timing-closure is easier to achieve during firmware implementation. The DB6 firmware has been under development and extensive testing has taken place in different testbenches and a test beam by interfacing DB6 prototypes to various prototype versions of the TileCal HL-LHC Upgrade system. The experience accumulated from the previous revisions and prototypes of

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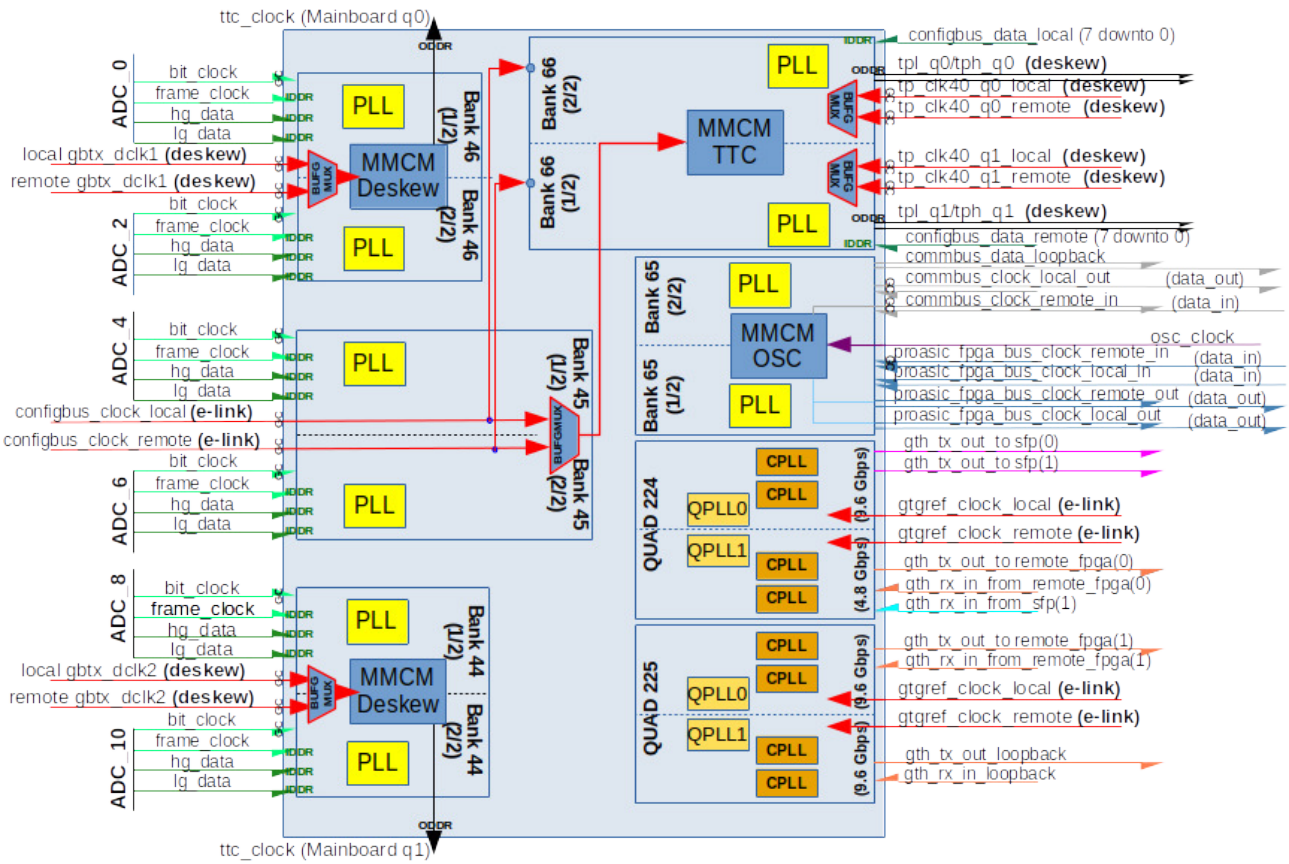


Figure 5: Distribution of clocks, ADC read-out pins (bit_clock, frame_clock, hg_data and lg_data), GTH transceiver signals, Configuration BUS (configbus) interface, TTC phase configurable clocks to drive the digitizing blocks and calibration signals on each MB quadrant (ttc_clock, tpl/tph) and other clock dependent modules for the DB6 Xilinx KU XCKU035 FPGA.

the DB was used as a baseline guide for the DB6 firmware that is currently in active development. Core functionalities have been successfully implemented in the firmware such as stable 4.6 Gbps downlinks and 9.6 Gbps uplinks interface with the TilePPr, ADC read-out, CIS signals, slow ADC Integrator system readout and front-end configurations.

## RADIATION TOLERANCE STUDIES FOR THE DAUGHTERBOARD 6 DESIGN

Previous revisions of the DB were tested for TID, NIEL and SEE to verify the radiation tolerance of each iteration for the HL-LHC era. The main driver for selecting the components to us in the board are the Xilinx FPGAs because of their importance in the functionalities of the design and weight in the end-price of the production of the boards. Three generations of the Xilinx Kintex family were studied. The forth revision of the DB (DB4) was powered by 28 nm planar Kintex 7 (K7) FPGAs, the fifth revision by 16 nm FinFET Kintex Ultrascale+ (KU+) FPGAs, and DB6 by 20 nm planar KU FPGAs. The strategy followed for Single Event Upset (SEU) appearances in Xilinx FPGAs rests in using the Xilinx Soft Error Mitigation (SEM) IP Core in the firmware implementation. The Xilinx SEM detects, classifies and corrects SEUs for the configuration memory. Not all the SEUs can be corrected, those classified by the SEM as uncorrectable are planned to be mitigated by using Triple Mode Redundancy (TMR) and partial reconfiguration whenever possible in the firmware, and where none of the previous solutions is possible an FPGA total re-configuration from the attached FLASH memory will be triggered. The K7 FPGAs were sufficient for the radiation requirements of the TileCal for the HL-LHC with manageable SEU rates where manageable with the fluences simulated at the time when the tests were performed [4]. However, there was a need to migrate to a different transceiver architecture because of the bandwidth gap present in the K7 GTX transceivers. It was expected that migrating to smaller feature size such as the ones of KU and KU+ would reduce the cross section for the Single Event Upsets (SEUs) of the FPGA chosen.

The KU+ FPGAs present in the DB5 feature GTY transceivers that allow 9.6 Gbps communication with full compatibility with the LHC timing [5]. The DB5 design proved to withstand up to 20 kRad of TID, being enough to qualify it for the HL-LHC lifetime within the radiation doses simulated as reported in the ATLAS Tile Calorimeter Phase-II Upgrade Technical Design Report [2]. However,

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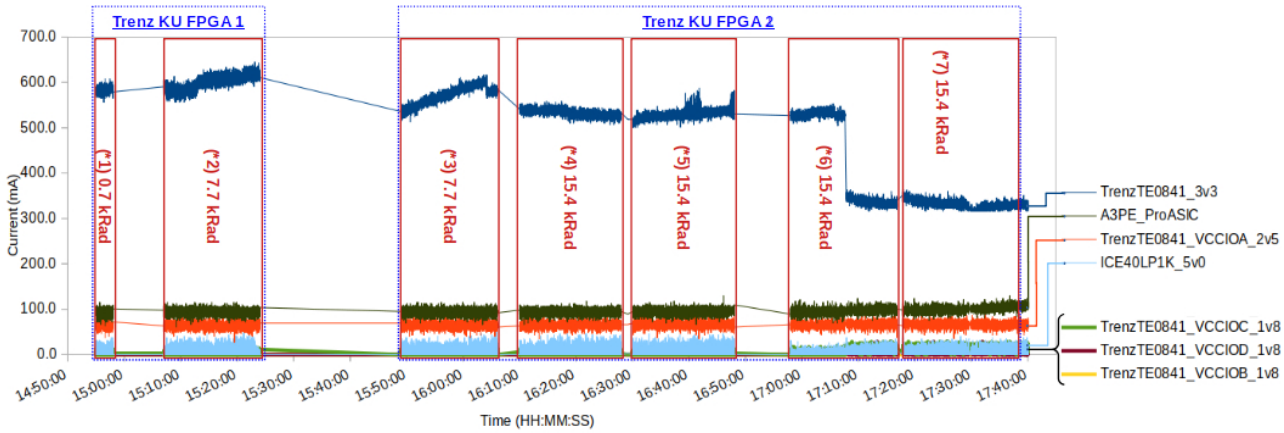


Figure 6: Current monitoring data corresponding to SEL tests with protons at 226 MeV performed on two Trenz TE0841 micromodules (marked as Trenz KU FPGA 1 and Trenz KU FPGA 2), a Microsemi A3PE starter kit, and a Lattice ICEBLINK LP1K evaluation board. The irradiation took place over seven runs, each signalized in the red boxes with (*x) followed the corresponding deposited TID dose. Note that values for the measured currents for TrenzTE0841_VCCIOB, TrenzTE0841_VCCIOC, and TrenzTE0841_VCCIOD are quite close to the current values for the ICE40LP1K_5V0. Therefore, the aforementioned channels are not visible in the plot [6]

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new dose estimates were obtained by new simulation runs performed with updated geometry. The new values established that to qualify the DB5 design, new TID tests had to performed up to either 72 kRad or to 14.4 kRad if the test included annealing. The SEU tests resulted in 4934 SEUs over a fluence of $2.05 \times 10^{11}$ protons cm$^{-2}$, of which only 11 SEUs could not be corrected by the Xilinx SEM. The uncorrectable SEU rates predict that 1.4 $\pm$0.4 uncorrectable errors are expected per DB per year. Between the Xilinx SEM and the TMR it is expected that correctable SEUs will not affect nominal runs. The DB5 SEE tests showed that the KU+ 16 nm FinFET technology is susceptible to Single Event Latch-ups (SEL) with SEL-fluence rate increased from $2 \times 10^{-11}$ SEL-fluence rate at 58 MeV to $2.36 \times 10^{-10}$ rate at 226 MeV protons [6]. The over-currents due to the latch-ups did not cause any noticeable damage, however SELs are highly undesirable. Hence, the solutions to mitigate SELs are to add an over-current protection to the design and migration to an SEL-resistant FPGA. Xilinx FPGAs require a specific power-on sequence and the implementation in DB5 was done by means of an RC circuit.

The KU FPGAs present in the DB6 design are powered by GTH transceivers, which are compatible with the 9.6 Gbps communication required by the TileCal HL-LHC Upgrade system. According to the published studies during the time, no SELs were seen in the 20 nm planar Xilinx FPGAs. Two Trenz TE0841 boards (each with the same KU FPGA used in the DB6 design), a Lattice ICE40LP FPGA and a ProASIC3E A3P31500 FPGA were irradiated with 226 MeV protons to verify for SEL sensitivity up to a target fluence of 1.11 $10^{12}$ p/cm$^2$, covering eight times the fluence simulated for 10-years of HL-LHC. During the test, all the currents of the FPGAs were monitored (Fig. 6) and no SELs were detected. The LCMXO2 CPLDs present in the TE0841 boards for buffering the JTAG chain used to configure the KU FPGAs failed due to TID effects. As a consequence only rough estimates of the SEUs could be obtained through the Xilinx SEM over two runs: 2 uncorrectable errors and 2 333 correctable errors for a rate of 166 soft errors per $10^9 \times$ p/cm$^2$.

In the case of the ProASIC3E A3P31500, the firmware started failing at around 57 kRad of TID or 75% of the total fluence with no recovery after power cycling. As reported by Actel, the firmware functionality was fully recovered after a long process of annealing and the VPUMP of the FPGA was permanently damaged making the reconfiguration of the chip permanently unavailable [7]. The Lattice ICE40LP FPGA firmware failed after approximately $10^9$p/cm$^2$ of the delivered fluence. The firmware functionality was recovered on-site by reconfiguring the FPGA from the attached FLASH memory after power-cycle.

Even though no SEL occurrences are expected in KU FPGAS, it was decided to integrate an SEL current limiting circuitry in the chain of DC-DC converters used in the power sequence scheme of DB6. This circuitry will power off the whole DC-DC converter chain of the half of the DB where one of the voltages gets a high current drain. This solution will increment the robustness of the board by avoiding potential damages to the FPGAs and other components on the presence of isolated unexpected SELs or overcurrents originated by any power failures. Additional radiation induced problems potentially caused by the use of large electrolytic capacitors at the DC-DC regulators used in previous revisions of the DB are being mitigated by the use of conductive polymer capacitors, which have been observed to be radiation tolerant with no impact to performance after 200 kRad at 500 rad per hour [8].

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The KU FPGA offered a good compromise in SEU rates ranging between K7 and KU+ and no SEL sensitivity up to the HL-LHC simulated fluences. Therefore, two DB6 prototyped were produced to do TID tests to the full design. The two DB6s (DB6-1 and DB6-2) were irradiated by means of a $^{60}$Co source at the CERN CC60 facilities. Each of the DBs was exposed to different dose rates and different dose targets. DB6-1 was irradiated to 220 Gy at a "fast" rate of 3.37 Gy/h and DB6-2 was irradiated to 52.6 Gy at a "slow" rate of 0.33 Gy/h. The KU FPGAs and all the board currents were monitored for each of the voltages, putting special interest in detecting any failures on the eight Coretek SFP+, the four KU FPGAs, the four Microsemi ProaSIC3 FPGAs and the reconfiguration FLASH memories. A baseline firmware was programmed in the ProASIC FPGAs and in the KU FPGA attached FLASH memories. After the irradiation period, both DBs were extensively tested in testbenches and none of the aforementioned components were damaged by the deposited TID.

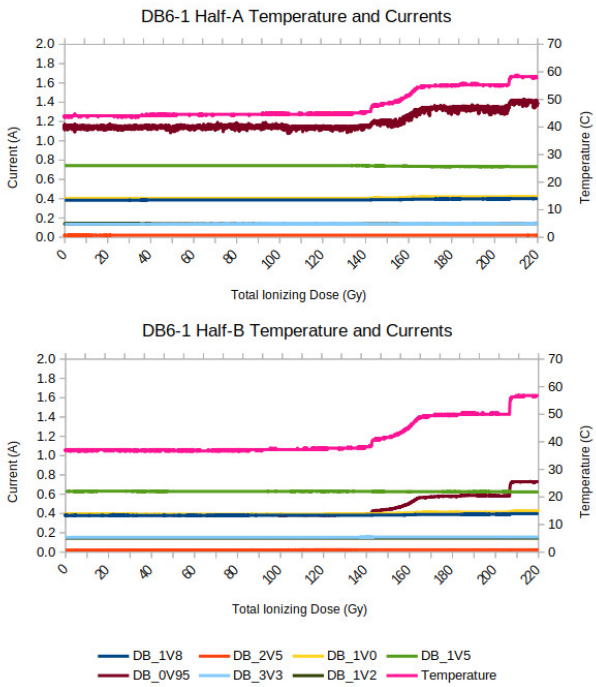


Figure 7: DB6-1 Current monitoring during 220 Gy (22 kRad) of TID exposure at 3.37 Gy/h (0.337 kRad/h).

During the DB6-1 TID exposure (Fig. 7), it was discovered a strong correlations between temperature and current in 0.95 V. An increase in current was measured in the 0.95 V of both sides at around 140 Gy. During the setup a fan was situated to keep the temperatures of the FPGAs steady during the irradiation period. The fan active components started to fail at around 140 Gy, leading to the increase of temperature on the FPGA during the rest of the irradiation period. The 0.95 V supplies the VCCRAM and the VCCINT for the core of the KU FPGA, making the currents drawn

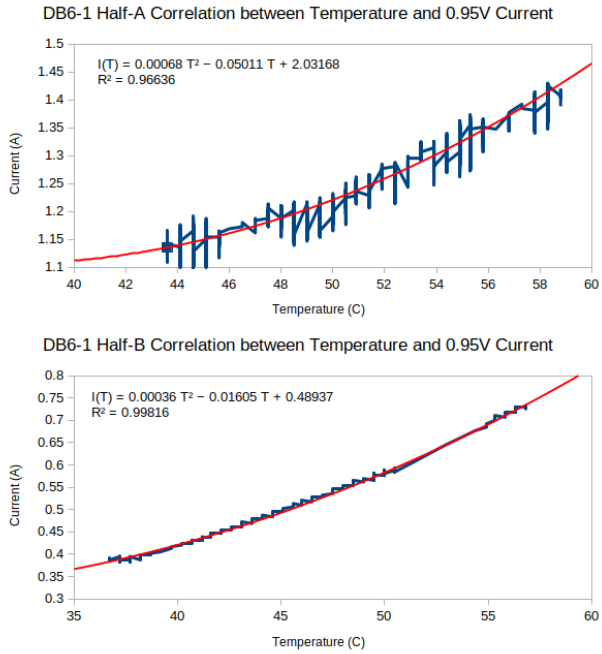


Figure 8: DB6-1 correlation between current and temperature for the 0.95 V channel of both DB halves fixed to a second polynomial degree regression.

from this voltage more sensitive to any temperature change in the FPGA.

A correlation between the 0.95 V current and the FPGA temperature was found by fitting the data to a second degree polynomial regression (Fig. 8). A convolution to the original data was done then to find the expected 0.95 V current behaviour for an exposure with constant temperature (Fig. 9). In each half the temperature value chosen for the convolution was the temperature measured on each FPGA when the test started.

In the case of DB6-2 (Fig. 10), all the currents and the temperatures were stable during the full run.

## CONCLUSIONS

The DaughterBoard is the read-out link and control board that interfaces a TileCal MD and the off-detector electronics. The current revision of the DaughterBoard (DB6) fulfills the radiation requirements for TID and SEE imposed by the HL-LHC. The DB6 improved the radiation tolerance of the previous designs that includes the SEL sensitivity issues of DB5, by migrating the design to the non-SEL sensitive 20 nm planar KU FPGA, adding extra protection to mitigate any overcurrent appearances and using conductive polymer capacitors. The studies performed on SEUs showed that even though the KU+ FPGAs offer a better SEU rates, the preliminary rates measured in the KU FPGAs are a good compromise for a design where SELs are unacceptable. To fully qualify the DB6 for the HL-LHC radiation requirements a dedicated SEU test and NIEL tests need to be conducted. Around 930 of the

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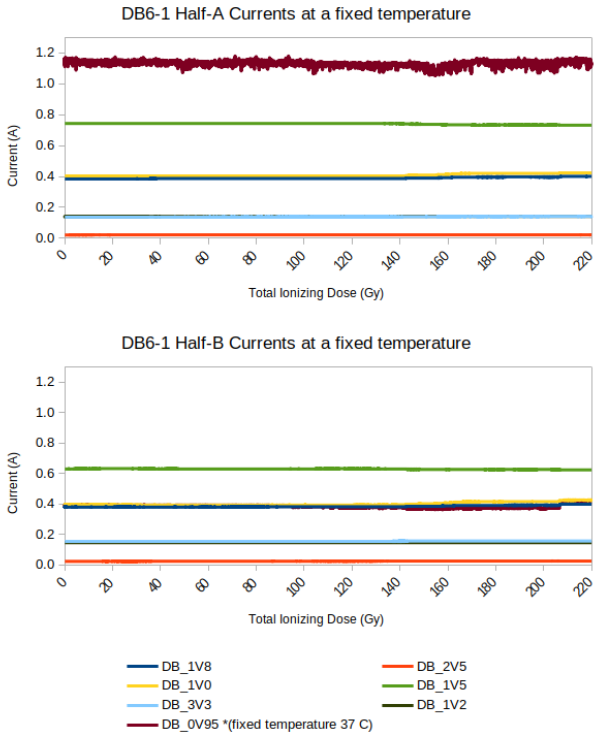


Figure 9: Expected DB6-1 Current monitoring during 220 Gy (22 kRad) of TID exposure at 3.37 Gy/h (0.337 kRad/h) with constant temperature. Only the current measurements for the 0.95 V voltages were corrected for temperature, the correction was done following the initial temperature value measured at the start of the test.

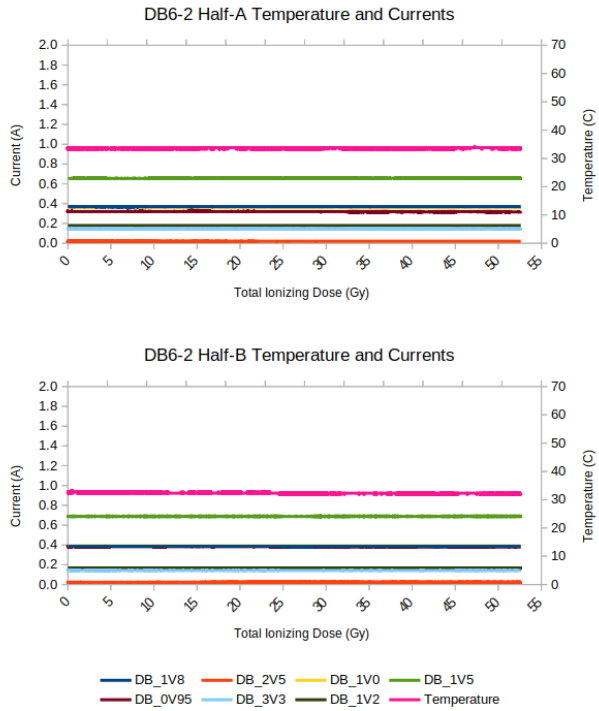


Figure 10: DB6-2 Current monitoring during 52.6 Gy (5.26 kRad) of TID exposure at 0.33 Gy/h (0.033 kRad/h).

redesigned DaughterBoards will be produced for Phase-II as the contribution of Stockholm University to the the ATLAS Upgrade for the HL-LHC era.

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