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THE DEMONSTRATOR OF THE HL-LHC ATLAS TILE CALORIMETER

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Abstract

The High Luminosity Large Hadron Collider (HL-LHC) has motivated R&D to upgrade the ATLAS Tile Calorimeter. The new system consists on an optimized analogue design engineered with selected radiation-tolerant COTS and redundancy layers to avoid single points of failure. The design will provide better timing, improved energy resolution, lower noise and less sensitivity to out-of-time pileup. Multiple types of FPGAs, CERN custom rad-hard ASICs (GBTx), and multi-Gbps optical links are used to distribute LHC timing, read out fully digital data of the whole TileCal, transmit timing and calibrated energy per cell to the Trigger system at 40 MHz, and provide triggered data at 1 MHz. To test the upgraded electronics in real ATLAS conditions, a hybrid demonstrator prototype module containing the new calorimeter module electronics, but still compatible with TileCal legacy system was tested in ATLAS during 2019-2021. An upgraded version of the demonstrator with finalized HL-LHC electronics is being assembled to be tested in testbeam campaigns at the Super Proton Syncrotron (SPS) at CERN. We present current status and results for the different tests done with the upgraded demonstrator system.

Introduction

The upgrade of the Large Hadronic Collider (LHC) to the High-Luminosity Large Hadronic Collider (HL-LHC) is aimed to deliver up to ten times peak luminosity [1]. HL-LHC is designed to deliver collisions at the luminosity of 7.5×10^{34} cm^{-2} s^{-1} and up to 200 simultaneous proton-proton interactions per bunch crossing. This environment necessitated a Phase-II upgrade of the ATLAS detector [2]. The Tile Calorimeter (TileCal) is the central section of the hadronic calorimeter of ATLAS. It plays an important role in the measurements of jet and missing transverse momentum, jet substructure, electron isolation, energy reconstruction and triggering, including muon information. To meet the requirements of HL-LHC, upgraded electronics were tested by using The Hybrid Demonstrator in real conditions. The Hybrid Demonstrator combining fully functional upgraded Phase-II electronics with analog trigger signals to be compatible with present and legacy ATLAS interface. Demonstrator comprises four prototype mini-drawers, each equipped with 12 Photo-Multiplier Tubes (PMT) with 3-in-1 cards, Mainboard, Daughterboard and high voltage regulation board. Finger Low Voltage Power supply (fLVPS) is powering all four mini-drawers with 10V. The Hybrid Demonstrator is connected to an off-detector Pre-Processor module with a patch panel. PreProcessor modules provide data and control interfaces between on-detector electronics and both legacy and Phase-II Trigger and Data AcQuisitions interface (TDAQi) [3].

Photo-Multiplier Tubes

At every bunch crossing light produced by scintillator plates is transmitted by wavelength shifting fibres. PMTs are responsible for converting this light coming from TileCal cells into analog signal and transfer it to the next stage of a signal chain. Every PMT is equipped with a High Voltage Active Divider (HVAD). The function of HVAD is to divide high voltage coming from high voltage system to 8 PMT dynodes. The high voltage for PMTs is in the range of 600-900 Volts. HVAD is also responsible for linear PMT response. PMT Block consists of PMT, HVAD and 3-in-1 card. For individual PMTs and PMT Blocks, there are two different test benches to ensure their performance and correct functionality. Before PMT Blocks are assembled each PMT is tested to ensure their physical properties. After this PMT Blocks are tested with Portable Readout Module for Tile Electronics (PROMETEO) system which ensures the correct functionality of PMT blocks alongside other demonstrator modules [3].

3-in-1 Card

The 3-in-1 card is part of the PMT Blocks, see Figure 1. They are responsible for shaping, amplification and integration of signal coming from PMT. 3-in-1 cards feature a 16-bit dynamic range, 50ns full width at half maximum (FWHM) time constant, fast readout with two gains (low gain and high gain), integrated slow readout, charge injection for continuous calibration over full dynamic range. Low-gain signals are summed into trigger towers (adder cards) and sent to off-detector electronics. It also consists of an analog trigger to be compatible with the current ATLAS architecture. Data from 3-in-1 cards are read by FPGAs from The Mainboard.

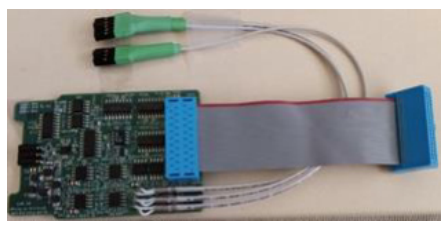

Figure 1: 3-in-1 Card [3].

Mainboard

The Demonstrator consists of four mainboards. The picture of The Mainboard is shown in Figure 2. Currently, Mainboard went through four revisions. The Mainboard is responsible for data transfer between PMT Blocks and Daughterboard. Each of them is connected to 12 PMT Blocks using Field Programmable Gate Arrays (FPGA).

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Each FPGA reads out 3 PMT Blocks. For The PMT Block readout, The Mainboard uses 12-bit ADC at 40 Msps and 16-bit ADC for slow integration. The Mainboard is designed to be reliable and redundant, therefore it is divided into two sections called A- and B- Side. Each section is completely independent with each side having +10V LVPS supply bricks. In ordered to prevent failure caused by LVPS or total failure each side is connected with a "Diode-Or" connection to make the power supply more redundant. Other functions of The Mainboard are to provide timing signals for low- and high-gain Charge Injection (CIS) calibrations. Mainboard V4 is the final revision that will be used in HL-LHC.

Figure 2: Mainboard [3].

Daughterboard

The Daughterboard is an on-detector communication board that interfaces between front-end electronics and back-end Tile Pre-Processor (TilePPr) module, The Daughterboard is shown in Figure 3. This is 4th version of The Daughterboard. It sends PMT data and Detector Control System (DCS) and detector readout data to TilePPr over multi-gigabit links. Like The Mainboard, The Daughterboard is also divided into two sections for reliability and redundancy. Redundant optical fibres are also used for protection against single link failure. CERN-developed GBTx protocol chip is used for FPGA configuration, LHC clock distribution and to receive DCS and run commands from off detector PreProcessor module. The Daughterboard version 6 is available and is being tested at CERN test beam facilities. Replacement with the latest version on The Demonstrator is under consideration.

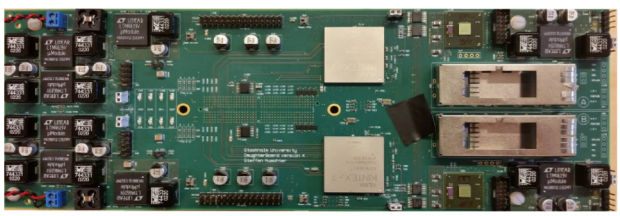

Figure 3: Daughterboard [3].

PreProcessor

The PreProcessor (PPr) is a core module of off-detector electronics. PMT Digital samples are transferred to The PPr every bunch crossing, A picture of the PPr is shown in Figure 4. The PPr has bi-directional communication with front-end electronics. It provides DCS commands, Timing, Trigger and Control information and the LHC Clock to the front-end electronics. From front-end electronics, The PPr receives PMT data which is stored in pipeline buffers waiting for trigger decision. In parallel, The PPr provides reconstructed energy information to the trigger system at 40MHz. After the trigger decision, The PPr sends buffered data to legacy Read-Out Driver (ROD) and processes in the same way as for current modules (backward compatibility).

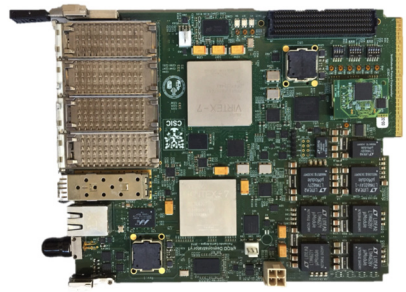

Figure 4: Tile PreProcessor [3].

Trigger and Data AcQuisition interface

Trigger and Data AcQuisition interface (TDAQi) communicates with off-detector electronics. It is responsible for constructing the trigger primitives and interfaces with trigger systems. The Trigger FPGA calculates trigger objects such as jets, muons, electrons with different granularity and energy resolution and results are transmitted through low latency optical links to the first level of the trigger. TDAQi is designed for HL-LHC and currently is not used for Demonstrator.

Low Voltage Power Supply

The Tile Calorimeter Low Voltage Power Supply (LVPS) provides power to all front-end electronics and provides control and feedback to the monitoring system and can be seen in Figure 5. Previous LVPS modules were generating eight different voltages for various sub-circuits of front-end electronics. In Phase-II upgrade each super-drawer is powered by one LVPS module which now provides 10V supply to all the front-end. As the result, TileCal has 256 LVPS boxes. Each LVPS box consists of eight bricks which coverts 200V input voltage to 10V output. For redundancy eight bricks are grouped into four sets of two. Diode-Or design is also implemented for improved reliability.

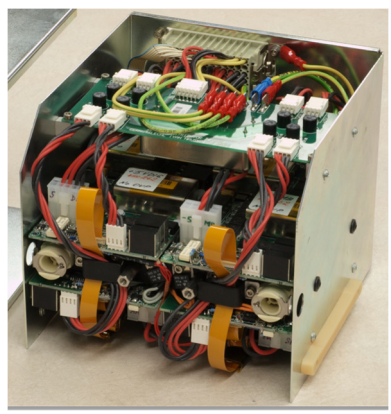

Figure 5: Low Voltage Power Supply [3].

High Voltage Power Supply

High Voltage Power Supply (HVPS) must supply high voltage to all PMTs in the system. it also needs to monitor, control and report values to DCS System, as shown in Figure 6. There is a total of 256 high voltage regulation boards each equipped with an ethernet interface.

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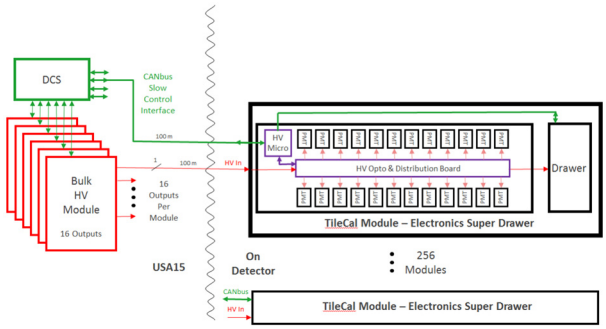

Figure 6: High Voltage Power Supply System [3].

Test Beam Results

The TileCal modules equipped with The Hybrid Demonstrator, with Phase-II upgrade electronics together with modules equipped with the old electronics, were exposed to different particles and energies in 7 test beam campaigns at CERN SPS North Area, during 2015-2018 [3].

The uniformity of the test module, which is segmented into three longitudinal layers (A - Figure 7 BC - Figure 8 and D - Figure 9), was evaluated using muon beams.

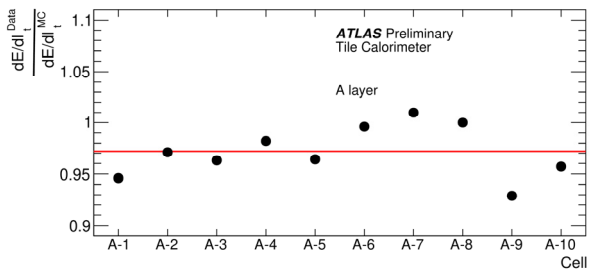

Figure 7: Longitudinal layer A [4].

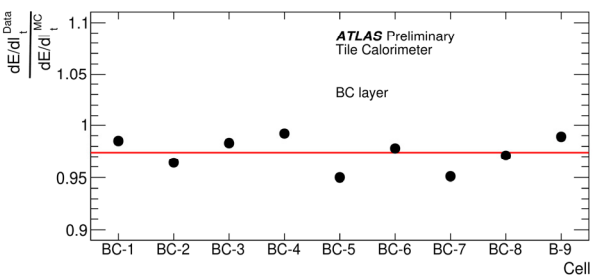

Figure 8: Longitudinal layer BC [4].

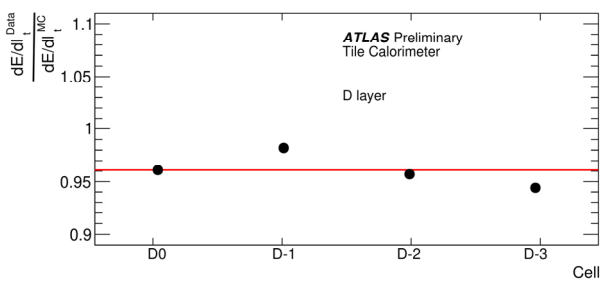

Figure 9: Longitudinal layer D [4].

Figure 10 shows the distribution of the total energy deposited in the calorimeter obtained using experimental and simulated electron data.

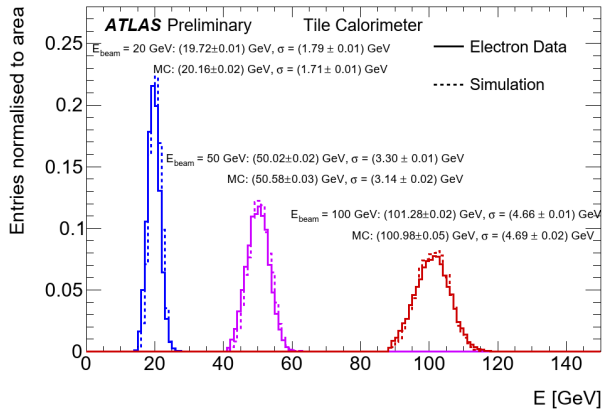

Figure 10: Total energy deposited in the calorimeter obtained using electron beams was also studied [4].

Detector energy response and resolution were studied using the hadron beams with different energies. The results obtained using muons, electrons and hadrons are in agreement with the calibration settings, as shown in Figure 11.

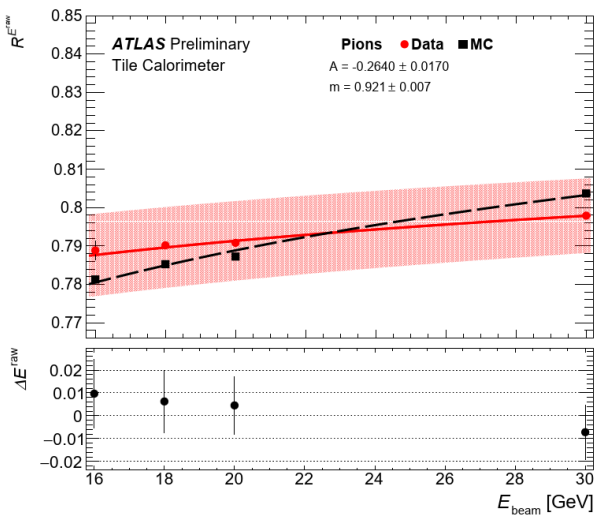

Figure 11: Energy response ratios, measured experimentally (red circles) and predicted by simulation (black squares) as a function of beam energy obtained using pions [4].

Figure 12 shows the stability of the laser over time with low and high gains.

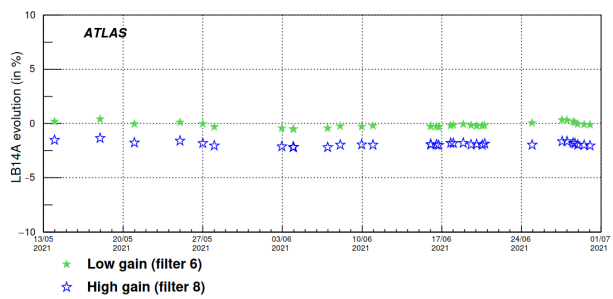

Figure 12: Stability of Laser over time.

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Figure 13 and Figure 14 show a comparison of noise between The Demonstrator and Legacy Module.

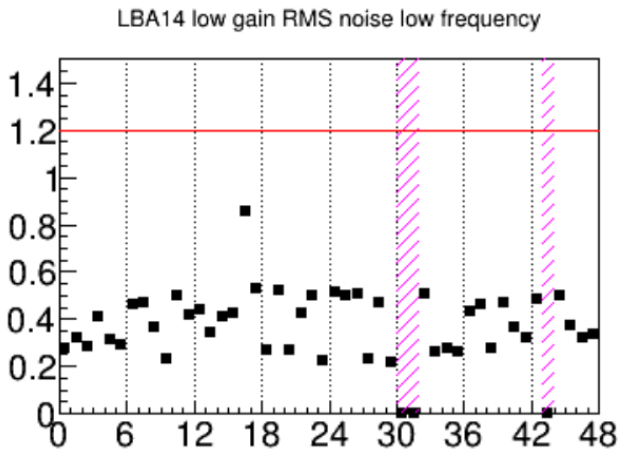

Figure 13: The Demonstrator low gain RMS noise.

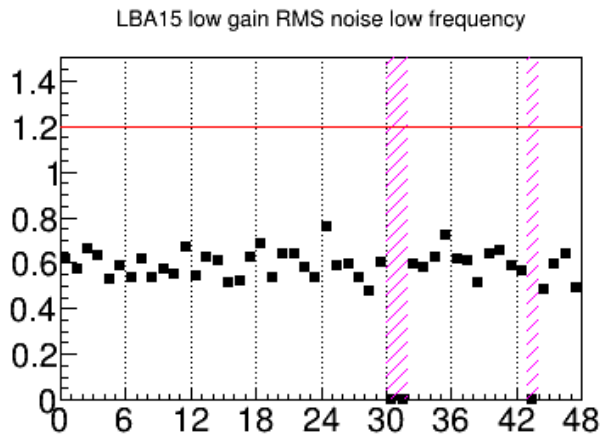

Figure 14: Legacy Module low gain RMS noise.

The above test beam results indicate that The Demonstrator Module performs at least as good as Legacy Module.

SUMMARY

The Tile Demonstrator Module is a prototype for an upgraded readout system and is compatible with current and legacy systems. The Tile Demonstrator is fully integrated into upgraded in the ATLAS Trigger and Data Acquisition and Detector Control systems. It was extensively tested during 2015, 2016 and 2017 test beams and demonstrated good performance. New tests will take place in November 2021 in order to validate new on-detector electronics in the radiation environment and associated off-detector electronics. The Tile Demonstrator module will also be present in Tile Calorimeter during the Run-3 period.

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