ISBN: 978-3-95450-221-9 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2021-THPV029

DEVELOPMENT OF TIMING READ-BACK SYSTEM FOR STABLE OPERATION OF J-PARC

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Abstract

Since 2006, the Japan Proton Accelerator Research Complex (J-PARC) timing system has been operated successfully. However, there were some unexpected trigger-failure events, typically missing trigger events, during the operation over 15 years. When a trigger-failure event occurred, it was often tough to find the one with the fault among many suspected modules. To solve the problem more easily, a unique device, triggered scaler, was developed for reading back accelerator signals.

The performance of the module has been evaluated in 2018. In 2021, we measured and observed an LLRF signal as the first signal of the read-back system for beam operation. After firmware upgrades of the module, some customized timing read-back systems were developed, and successfully demonstrated as coping strategies for past trigger-failure events. In addition, a future plan to apply the read-back system to other facilities is discussed. More details are given in the paper.

INTRODUCTION

J-PARC (Japan Proton Accelerator Research Complex) is a high-intensity proton accelerator complex. It consists of three accelerators: a 400-MeV H- Linac (LI), a 3-GeV Rapid Cycling Synchrotron (RCS), and a 30-GeV slow cycling Main Ring Synchrotron (MR) [1-2]. Since the initial beam in 2006, J-PARC has been improving beam power. Concerning MR, recent beam power is about 500-kW (50-kW) by fast (slow) extraction, respectively [3].

There are two time cycles used in J-PARC: A 25-Hz rapid cycle is used at LI and RCS, a slow cycle is used at MR. When MR delivers proton beams to the NU and HD facilities, 2.48-s (fast extraction mode (FX)) and 5.20-s (slow extraction mode (SX)) cycles are used, respectively. Because the slow cycle determines the overall time behavior of the accelerators, it is also called a "machine cycle."

The control system for J-PARC accelerators was developed using the Experimental Physics and Industrial Control System (EPICS) framework [4]. In addition, a dedicated timing system has been developed [5-6]. The J-PARC timing system consists of one transmitter module and approximately 200 receiver modules. Both types of modules were developed as in-house VME modules. Event-codes, which have information on beam destination and beam parameters, are distributed from the transmitter module to the receiver modules. A fiber-optic cable network is used for event-code distribution using several optical-to-electrical (O/E) or electrical-to-optical (E/O) modules. According to the received event-code, each receiver module generates eight independent delayed trigger signals.

Since the first beam use began in 2006, the J-PARC timing system has contributed to a stable operation of the accelerator beam [6]. Nevertheless, some timing trigger-failure events have occurred during beam operation. During each recovery process against a failure, it was often difficult to find a definite module among the many modules suspected. Such experiences have prompted us to develop a new module that can read back signals generated by the J-PARC timing system. We developed a new module, called a triggered scaler module, for this purpose [7-8].

In this paper, using one of trigger-failure events occurred in J-PARC MR as a case, the working principle, a usage in beam operation, and firmware upgrades of the triggered scaler module, are described. Moreover, a customized read-back system is introduced, followed by a discussion on the plan for future.

PAST TRIGGER-FAILURE EVENTS

Since 2006, we experienced some unexpected trigger-failure events during beam operation [8-9]. Herein, one case is given as an example, a 25-Hz irregular trigger event.

From November to December 2016, an O/E module, which was used to send a 25-Hz trigger signal from RCS to MR, started to produce irregular triggers (Fig. 1). Because the irregular triggers affected a critical beam diagnostic system, the accelerator operation was suspended several times per day [7]. It took 2 weeks to identify the troublesome O/E module.

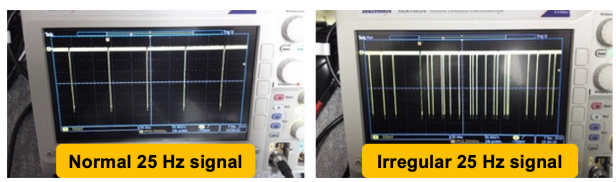

Figure 1: The normal and irregular 25-Hz trigger signals monitored by an oscilloscope during beam operation.

TRIGGERED SCALER MODULE

Introduction

A unique device, triggered scaler (hereafter TS), was designed by J-PARC control group for reading back timing signals. It is a scaler to count number of pulses in a specified accelerator cycle, and it stores the counts in a momentary array [7-8]. The differences between a TS module, a digitizer, and a simple scaler are shown in Fig. 2. Contrast to the simple scaler, the uniqueness of the triggered scaler

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module is that it has an external trigger input and an output data as a digitizer, and its output is a data buffer with 192 elements. It was designed as a Yokogawa (FA-M3/e-RT3) PLC-type, which can fit the standard I/O form in J-PARC MR.

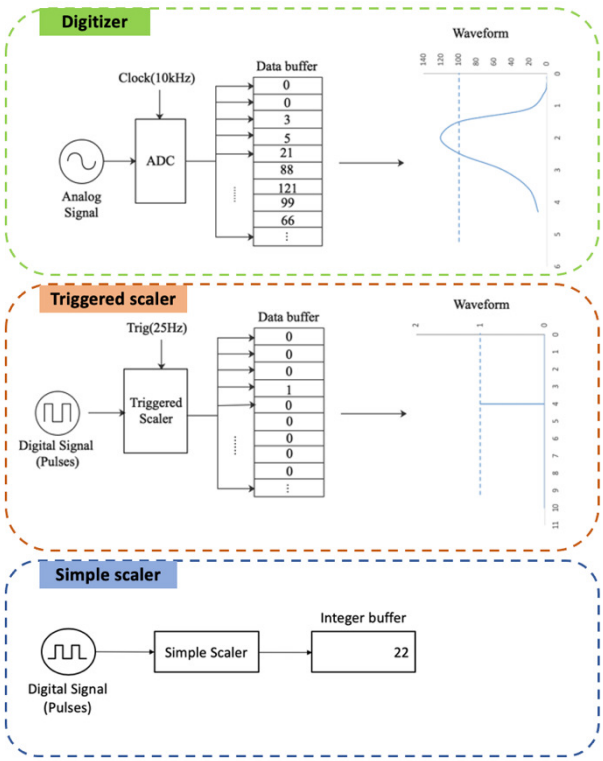

Figure 2: The comparison of digitizer, triggered scaler, and simple scaler.

There are two types of the module: the MR-type and the LI-type. The hardware appearances of the two types are shown in Fig. 3. The LI-type TS module was designed to find a missing trigger event of the LI accelerator. The module checks the pulse count in the rapid cycle (25-Hz), and outputs an error signal when an error is detected. In turn, the MR-type checks the pulse counts in the last slow cycle (2.48-s or 5.20-s) and raises an error flag. Both require the start signals of the slow cycle ("S") and the rapid cycle ("Trig"), provided by the J-PARC timing system. The MR-type has four input channels and no output channel, while the LI-type has two input channels and two error-output channels. There is a dual ring buffer (192 cells × 2 for MR-type, 448 cells × 2 for LI-type, 16 bit/cell) for each channel.

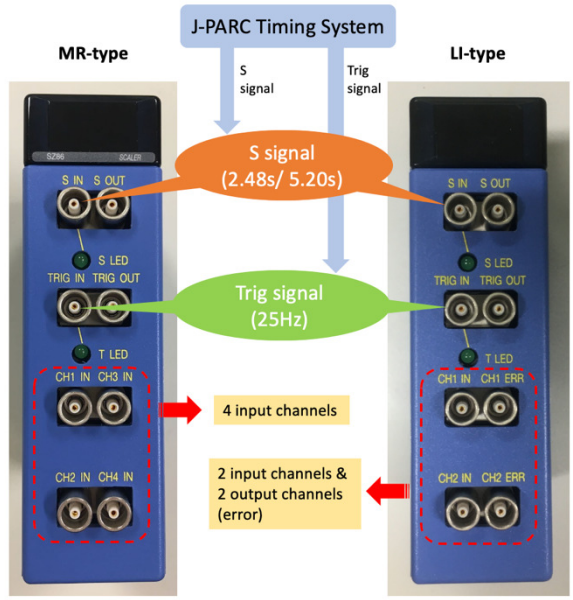

Figure 3: The hardware appearances of two types of the triggered scaler module.

Working Principle

In principle, each channel of the TS module works as a scaler. Two internal FPGA logics are shown in Fig. 4. The first logic (FPGA_1) counts the input pulses. When the "S" signal arrives, FPGA_1 starts to increase the count in the first cell of the first memory buffer. Each time the "Trig" signal arrives, FPGA_1 shifts the pointer to the next cell. When the following "S" signal arrives, the pointer is moved to the first cell of the second memory buffer. In other words, each cell keeps several trigger pulses received in a 40-ms bin (as the "Trig" signal is 25-Hz). This scheme enables retrieval of the numbers of counts during the last machine cycle. The second logic (FPGA_2) reads the memory buffers, checks whether trigger faults exist or not, and outputs an error signal for LI-type or sets an error flag for the MR-type, if necessary. The LI-type module can output an error signal directly through the output channels.

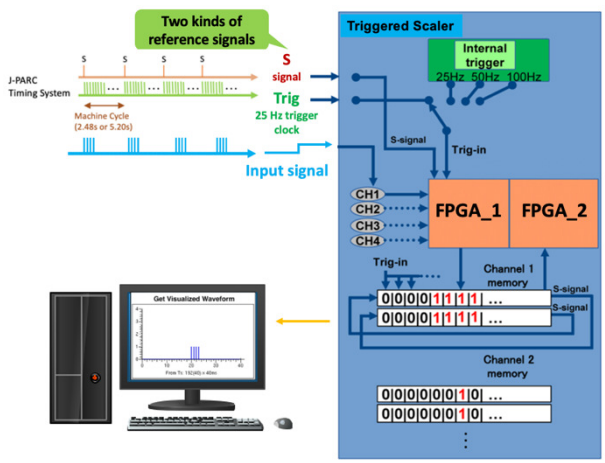

Figure 4: The conceptual design of the triggered scaler module.

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For Beam Operation

The performance of the module was confirmed and reported in 2018 [7]. Early in 2021, a setup for beam operation was prepared as shown in Fig. 5. It consists of a CPU module, a TS module, and a power supply module. All of them are standard Yokogawa PLC modules. Linux and EPICS IOC are running on the CPU module.

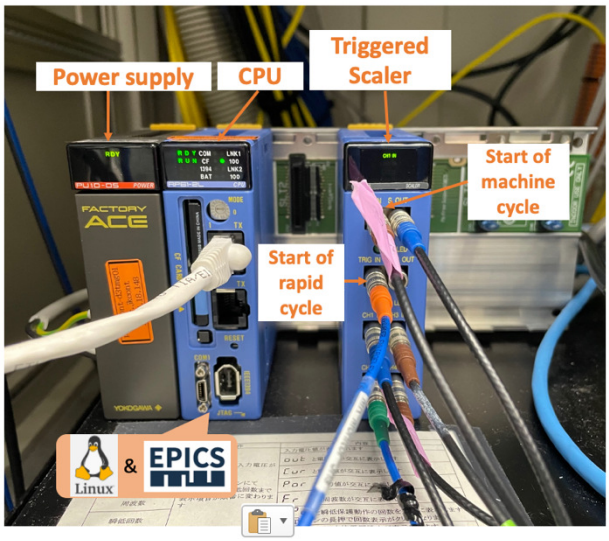

Figure 5: Test setup of triggered scaler module.

In May 2021, we started to observe an LLRF signal (MR circulation signal) by the setup, as one of the first operational surveillance to read-back signals. LLRF patterns in 30-GeV and in 8-GeV are visualized as shown in Fig. 6 (a). An EPICS PV (Process Variable) for the MR energy, which is deduced from the observed LLRF patterns, was developed and has been recorded by an archiver (as shown in Fig. 6 (b)).

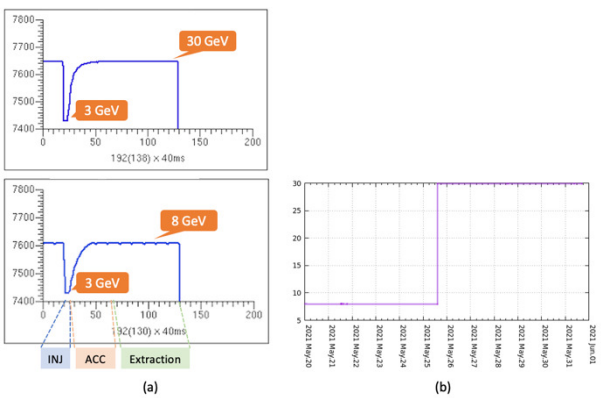

Figure 6: (a) Measurement of an LLRF signal, (b) MR energy from an archiver.

Firmware Upgrades

Based on experiences of module measurements, we identified small problems in the TS module. In 2020 and 2021, we upgraded the firmware of the MR-type module as follows (details are given in [9]).

1. Synchronize the internal trigger with the "S" signal. In the old firmware, the cell position of the received signal sometimes shifted to the next position.
2. Add preset-delay function for "Trig" signal. This function is to adjust the arrival time of the "S" signal relative to the external "Trig" signal.
3. Add 30-Hz, 60-Hz, and 120-Hz internal triggers to use in western Japan and other countries.
4. Clear data buffer each time when "S" signal comes.
5. A bug in counting the last cell of the data buffer was fixed. This bug has caused zero count in the last cells (62nd or 130th) when we had measured the RF signal.
6. Enlarge the LED flushing duration up to 10-ms, for better visibility in field works.

The issues 1 and 5 were caused by unsynchronized internal trigger. With the new firmware, the internal trigger is synchronized with the "S" signal. The issues 2 and 3 are essential upgrades to use the module in other facilities. The issues 4 and 6 were updated for user's conveniences.

This firmware upgrade was significant to shift the module status from a test to an operational phase. The firmware upgrade of the LI-type module is planned.

CUSTOMIZED TIMING READ-BACK SYSTEM

It has been demonstrated that the TS module can measure and visualize accelerator signals with the relationship of accelerator cycle. Several customized timing read-back systems were developed based on the module, as the countermeasures against the past trigger-failure events [9]. Here shows one example: a read-back system of 25-Hz trigger.

The 25-Hz trigger from RCS is important for the beam diagnostic system of a fast-current transformer (FCT), which observes the in-coming protons into MR. The past trigger-failure event in 2016, as shown in Fig. 1, caused a critical problem.

The read-back system of 25-Hz trigger observes the signal at the MR side since May 2021.The system realizes remote monitoring of the signal as shown in Fig. 7. Thus, we can find the same failure event immediately.

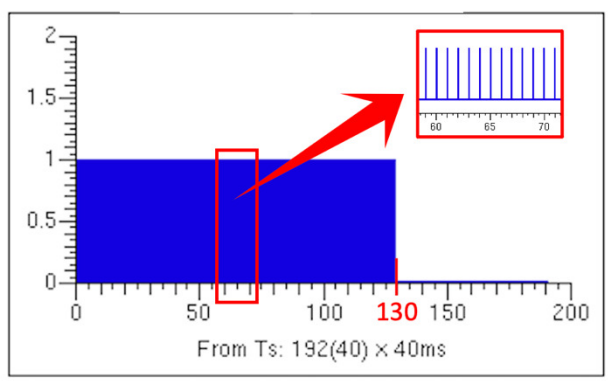

Figure 7: The observed 25-Hz trigger signal from RCS in a machine cycle (5.20-s) by the read-back system.

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FUTURE PLAN

The current read-back system assumes the use of the computer resources of the J-PARC control system. Thus, it is unavailable elsewhere, but on the J-PARC site. We would like to develop a standalone read-back system, which is available for other accelerators.

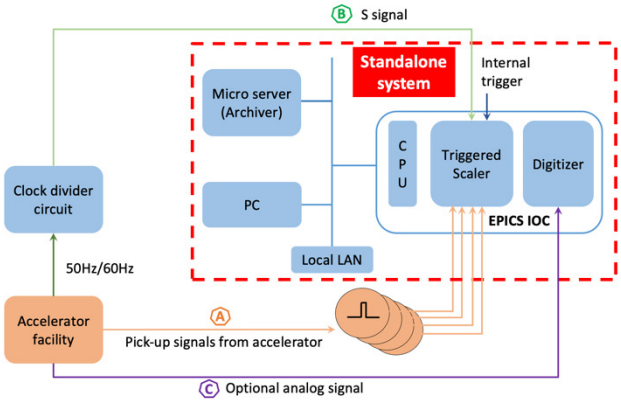

Figure 8: A standalone read-back system for other accelerators.

Fig. 8 shows a planned design of standalone read-back system. The system requires the start signal "S" from the target facility, which is needed to start the TS module. If there is no "S" (or similar) signal, a clock divider circuit would be used to simulate the signal from 50-Hz/60-Hz. The internal trigger of the TS module is to be used. Thus, no external trigger clock is needed. With additional I/O modules like a digitizer, the system can meet to various cases in other accelerator facilities. The unexpected trigger-failure detection of the target timing signal could be customized by updating the EPICS IOC software upon request. A portable micro-server is expected to work as an archiver to analyse faulty events.

If the portable standalone read-back system is successfully developed, it can be exported to other facilities.

CONCLUSION

A triggered scaler module was developed to read back the signals of the J-PARC timing system. The module is capable of detecting accelerator signals as well as visualizing beam based on the relationship with the accelerator cycle. The first read-back system by the TS setup started operational surveillance for an LLRF signal. Then, a customized read-back system for the 25-Hz trigger is introduced. It is demonstrated as a countermeasure against the trigger-failure event in 2016.

An idea to develop a standalone read-back system has been discussed. We expect the development of the standalone system will contribute to the accelerator timing fields in the future.

ACKNOWLEDGEMENTS

We express our best thanks to Noboru Yamamoto and other J-PARC accelerator staff members for their encouragement and suggestions during system development.

REFERENCES

[1] J-PARC website, http://j-parc.jp/index-e.html

[2] S. Nagamiya, "Introduction to J-PARC", *Prog. Theor. Exp. Phys*., vol. 2012, no. 1, p. 02B001, Oct. 2012. doi:10.1093/ptep/pts025

[3] S. Igarashi *et al.*, "Challenging to higher beam power in J-PARC: achieved performance and future prospects", in *Proc. 10th Int. Particle Accelerator Conf. (IPAC'19)*, Melbourne, Australia, May 2019, pp. 6-11. doi: 10.18429/JACoW-IPAC2019-MOYPLM1

[4] N. Kamikubota, *et al.*, "J-PARC control toward future reliable operation", in *Proc. ICALEPCS2011*, Grenoble, France, 2011, paper MOPMS026, pp. 378-381.

[5] F. Tamura, *et al.*, "J-PARC timing system", in *Proc. ICALEPCS2003*, Gyeongju, Korea, 2003, pp. 247-249.

[6] N. Kamikubota, *et al.*, "Operation status of J-PARC timing system and future plan", in *Proc. ICALEPCS2015*, Melbourne, Australia, Oct. 2015, pp. 988-991. doi:10.18429/JA-CoW-ICALEPCS2015-WEPGF121

[7] N. Kamikubota, *et al.*, "Development of triggered scaler to detect miss-trigger", in *Proc. PCaPAC2018*, Hsinchu, Taiwan, 2018, pp. 213-215. doi:10.18429/JACoW-PCaPAC2018-THP21

[8] M. Yang, *et al.*, "Applications of triggered scaler module for accelerator timing", in *Proc. 22nd Virtual IEEE Real Time Conference*, 2020. arXiv:2010.14716v2 [physics.acc-ph]

[9] M. Yang, "Development of Timing Read-Back System toward Stable Accelerator Operation", Ph.D. thesis, The Graduate University for Advanced Studies, SOKENDAI, Japan, 2021.