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A NEW TIMING SYSTEM FOR PETRA IV

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Abstract

The currently ongoing PETRA IV project at DESY proposes an upgrade of the PETRA III synchrotron light source towards a fourth-generation, low emittance machine. The goal is to provide X-ray energies in the regime of 10 keV bringing the electron beam production to its physical limits with respect to the smallest achievable source size, and thus approaching the diffraction limit.

The realization of this new, challenging machine implies a new design of the timing and synchronization system because requirements on beam quality and controls will become significantly more demanding with respect to the existing implementation at PETRA III. Furthermore, the PETRA IV baseline for the fast front-end electronics readout will be based on the MTCA.4 standard. Given the success of the at DESY developed MicroTCA.4-based timing system for the European XFEL accelerator, it has been chosen to utilize the MTCA.4 technology for the PETRA IV timing system as well.

We present in this paper general concepts of the timing and synchronization system, its integration into the control system as well as first design ideas and evaluations of the major timing system hardware component, a MicroTCA.4-based AMC.

THE PETRA IV PROJECT

The PETRA IV project [1] comprises the replacement of the existing 3rd generation synchrotron radiation source PETRA III with a state-of-the-art ultra-low emittance storage ring. This includes the upgrade of the storage ring infrastructure with a circumference of 2304 m as well as the redesign of the current pre-accelerator chain and construction of new beamlines. The 6 GeV storage ring will be operated at an RF frequency of 500 MHz as PETRA III. Currently, the PETRA III facility can run in either the timing mode with 40 equally distributed electron bunches at 100 mA stored beam or in brightness mode with 480 equally distributed bunches and 120 mA of beam current. The bunch pattern options are being under discussion since recent modifications of the lattice design allow now for patterns more similar to the PETRA III ones rather than what was proposed in the PETRA IV CDR.

The present booster synchrotron DESY II will be replaced by a new one, DESY IV, to meet the requirements of a low emittance beam injected into PETRA IV. While the LINAC section will be kept, the gun will be upgraded as well as the transfer section with the PIA accumulator has to be revised. The option of keeping DESY II for test beam production has to be taken into account when designing the timing and synchronization system even if this is not considered to be part of the baseline layout of the PETRA IV project. The entire facility is shown in Fig. 1.

Furthermore, the front-end electronics for diagnostics and instrumentation will be completely overhauled and based on the MTCA.4 standard. At the same time, it has been decided to change over the existing PETRA III control system using the TINE framework to a DOOCS-based one as used at the DESY FEL accelerators. This effectively leads to the necessity to redesign the entire timing and synchronization system and its controls for the storage ring as well as for the pre-accelerator chain.

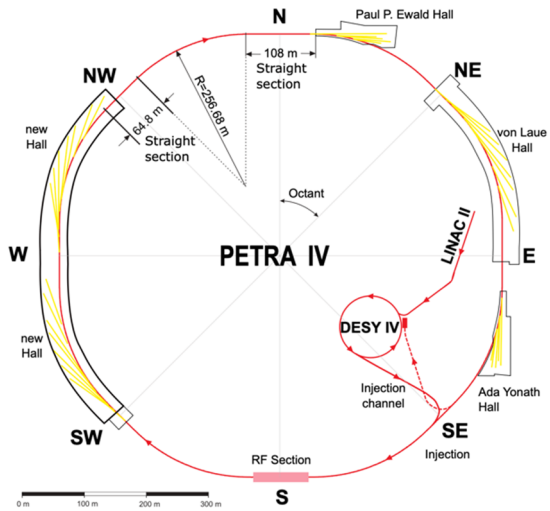

Figure 1: The PETRA IV facility layout with its existing, its new experimental halls and its pre-accelerators.

THE TIMING SYSTEM DESIGN

The overall concept of the new timing and synchronization system has to provide services to at minimum four individual synchrotron, booster, accumulator or LINAC facilities. Namely, the new PETRA IV storage ring, the new DESY IV booster ring, potentially a PIA II accumulator and a LINAC. If it is desired to continue to provide test beam services through DESY II fed by the same new LINAC and PIA II, one has to make sure, these are well enough synchronized with respect to the RF, timing and controls with the pre-accelerator chain for PETRA IV. The idea being pursued at the moment is to provide individual main oscillators and main timing system components for each of the major installations PETRA IV, DESY IV, DESY II and LINAC with PIA together. This would allow for a most flexible way of providing the different required RF frequencies and synchronization signals. Beamlines and experiments would be served by the timing system of PETRA IV, test beams by the DESY II one. The challenge

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here will be to synchronize not just the RF reference signals but also the timing information itself, i.e. cycle numbers and such to uniquely tag the data across facilities for later analysis.

THE TIMING SYSTEM HARDWARE

Baseline

The hardware for the new timing and synchronization system will follow this baseline:

- MTCA.4 [2] will be used as the standard for the timing system electronics specifically for the transmitter and receiver module.
- Since MTCA.4 has been successfully introduced and established when constructing and commissioning the European XFEL accelerator timing system, the design of its transmitter and receiver Advanced Mezzanine Card (AMC) [3] will be used as a basis for the new PETRA IV MTCA.4 timing module.
- The design will be kept such that adaptions and modifications of the overall functionality can be implemented easily during the life-cycle of the accelerator.
- Essential to a successful realization is the expertise from both the machine beam controls and machine controls system groups, being the developers of the timing and synchronization systems for the FEL and synchrotrons at DESY.

Key Requirements

The key requirements for the timing and synchronization system of which the latter is crucial for the proper RF reference and signal distribution are given as follows:

- Distribution of a continuous RF reference signal
- Provision of low-jitter clocks for ADC sampling
- Distribution of timing signals, clocks and trigger events
- Provision of beam-synchronous data such as:
    - High-resolution timestamp
    - Revolution counter(s)
    - Beam modes i.e. timing or brilliance mode
    - Bunch pattern
    - Bunch current (PETRA IV)

Further, it has been proven at the EuXFEL that a common MTCA.4 module acting as a transmitter and/or as a receiver is a quite flexible and convenient concept.

A dedicated optical fiber network with drift compensation along the lines will be used. The topology follows the storage ring layout to make use of temperature-controlled media shafts and facilities. The storage ring, the booster and the LINAC with its gun will have its own timing system, however, being synchronized across the overall facility. Beamline experiments will have the possibility to connect to the PETRA IV timing system via the same MTCA.4-based AMC module.

Integration into The Control System

An important part of the PETRA IV control system will be to provide all relevant data not only to control and monitor the entire accelerator but also to analyze its performance and proper functioning. This requires the timing system to provide the corresponding functionality. Beam-synchronous information like a high-resolution timestamp, revolution counters and a bunch pattern might be utilized by:

- Post-mortem analysis
- Transient recorder
- Event archives
- Bunch-resolved data acquisition (for detailed analysis)
- Experiment controls and its beamline data acquisitions

PROJECT STATUS

Organization

The timing and synchronization system project is well embedded into the overall PETRA IV project management. A work-breakdown structure as well as a product-breakdown structure with all of its deliverables have been set up. The PBS represents a hierarchical view of all PETRA IV components:

- Define the scope “What will be built?”
- Organization of design and specification data
- Integration of the subsystem into the overall project

Requirements are derived for each PBS item and classified:

- Design, Interface, Functional
- Design can be validated against requirements
- Requirements are linked to PBS items

As of now requirements from accelerator subsystems, accelerator work packages as a well as beamline experiments are being collected, discussed and evaluated. This is an iterative process and will continue throughout the TDR stage. Eventually reviews will lead to a final design for the TDR documents.

MTCA.4 Hardware Design

Currently an evaluation phase is ongoing and accompanied by lab pre-tests. This is done with the existing x2timer AMC hardware as installed at the DESY FEL machines and shown in Fig. 2 but also with a potentially new hardware based on the MPSoC-enabled Xilinx Zynq technology. For this, a Xilinx Zynq evaluation board as shown in Fig. 3 is being evaluated.

The primary goal here is to test the clock and trigger generation function, as used in PETRA III, and to measure the jitter quality of generated clock and trigger signals at the output. Using a dual loop PLL clock cleaner is being investigated as an improvement to the output jitter.

At the same time components for the distribution of the incoming and outgoing clock and trigger signals on the AMC-Card are being researched and tested. Those components must have a very low additive jitter as well. Therefore, a test stand for measuring its signal jitter has been set up in the lab.

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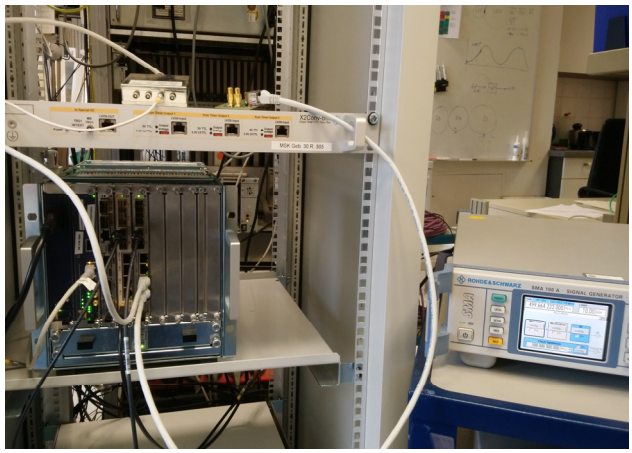

Figure 2: This figure represents the setup of the MTCA system with an x2timer AMC for tests and evaluation.

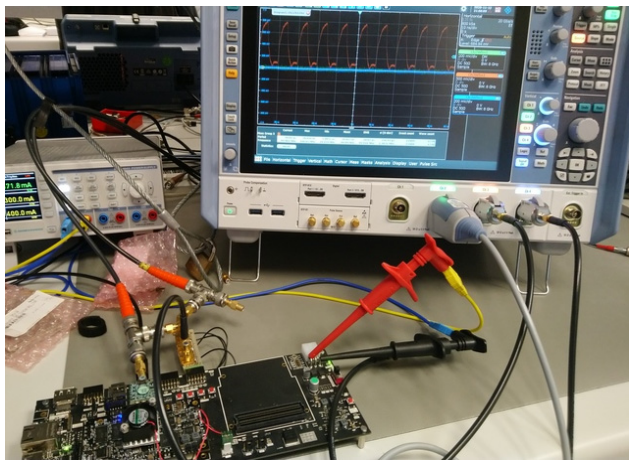

Figure 3: Shown in this picture is the measurement and FPGA evaluation board setup.

New concepts for the advance delay calculation which is required to target individual buckets inside the PETRA ring have to be developed as well as different kinds for the FPGA control system interface.

The next major step will be the integration of the aforementioned functionality into the existing DAMC-FMC1Z7IO AMC-Card. This MTCA.4 component is being developed by the DESY MSK group and the DESY MTCA Technology lab.

Since the overall distribution of the timing system information is using a distributed optical fiber topology, the clock recovery mechanism as well as drift compensation mechanisms have to be tested, too.

Eventually, the development has to yield in a design of a Zynq architecture-based successor AMC of the x2timer, currently being called x3timer. The design of this card is already in the specification phase and will be based on results of the requirements engineering in progress.

OUTLOOK AND ROADMAP

The next milestones within the TDR phase until mid of 2023 are:

- Collect requirements and derive specifications
- Develop MTCA AMC- and RTM-Card architecture and interfaces according to the specifications
- Adapt AMC- Design for x3timer demonstrator
- Hardware development and production
- Firmware development for the x3timer AMC
- Front-end controls development, i.e. server applications for controls

CONCLUSION

The renewal of the timing system for PETRA IV is without any choice however challenging. Given the excellent experience made with MTCA.4-based solutions specifically for the timing system hardware at the DESY FEL accelerators FLASH and the European XFEL, we are confident that this technology choice will serve the PETRA IV project quite well, too.

Our goal within the TDR phase is to fully specify the requirements of the PETRA IV timing and synchronization system and produce a fully functional demonstrator of the x3timer AMC hardware until 2023.

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